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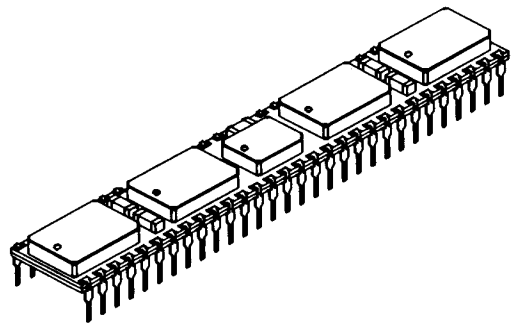
DESCRIPTION:

The DPS6434 is a fully asyncronous Static Random Access Memory (SRAM) and may be organized as 64K X 32, 128 X 16 or 256K X 8.

The module is built with eight low-power CMOS 32K X 8 SRAM's and two high speed 139 decoders. The DPS6434 is ideally suited for those computer systems having a 32-bit architecture.

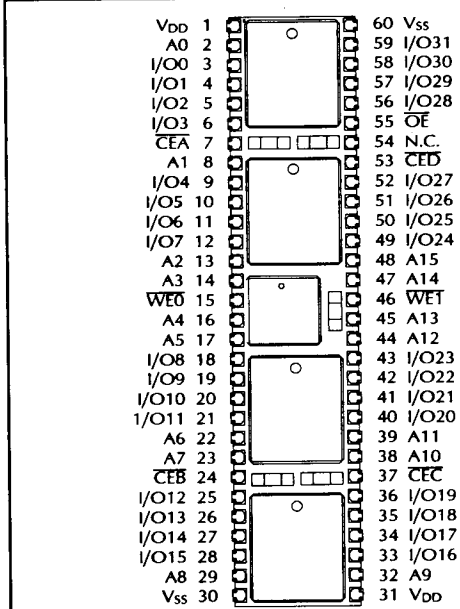


FEATURES:

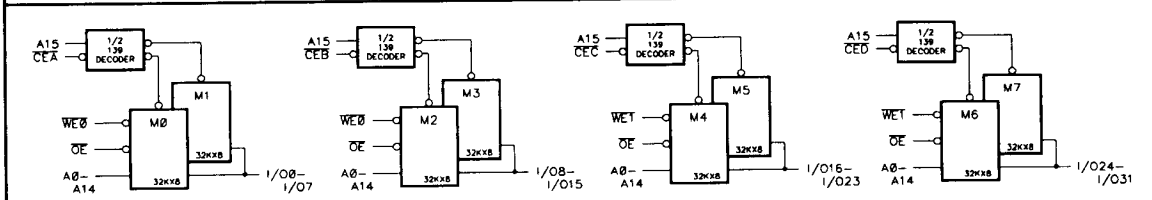
- Organization Available:
  64K X 32, 128 X 16 or 256K X 8
- Access Times: 35, 45, 55, 70, 85
  100, 120, 150ns (max.)
- Byte, Word, and Double Word Selectable
- Separate $\overline{OE}$ Pin
- Low-Power CMOS Design
- Single +5V Operation (± 10% Tolerance)
- TTL-compatible Inputs and Outputs
- 60-Pin, 600-Mil Wide Ceramic DIP Package

PIN NAMES	
A0 - A15	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{CEA}$	Chip Enable for I/O0 - I/O7
$\overline{CEB}$	Chip Enable for I/O8 - I/O15
$\overline{CEC}$	Chip Enable for I/O16 - I/O23
$\overline{CED}$	Chip Enable for I/O24 - I/O31
$\overline{WE0}$	Write Enable for I/O0 - I/O15
$\overline{WE1}$	Write Enable for I/O16 - I/O31
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



DPS6434-35, -45, -55, -70, -85, -100 DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions		C Min.	C Max.	I Min.	I Max.	M/B Min.	M/B Max.	Unit
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-20	+20	-20	+20	-20	+20	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}		-20	+20	-20	+20	-20	+20	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	X32		530		610		630	mA
			X16		390		450		560	
			X8		320		370		375	
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA	X32		690		790		790	mA
			X16		470		540		540	
			X8		360		415		415	
I_{SB1}	Full Standby Supply Current (CMOS)	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ + 0.2V, $\overline{CE} \geq V_{DD}$ -0.2V			16		16		16	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}			280		280		280	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA			0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA		2.4		2.4		2.4		V

DPS6434-35, -45, -55, -70, -85, 100 DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	TYP.	Max.	Unit
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V, $\overline{CE} \geq V_{DD}$ -0.2V		0.2	0.6	mA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V, $\overline{CE} \geq V_{DD}$ -0.2V		0.5	1.2	mA
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	5			ms

DPS6434–120, -150 DC OPERATING CHARACTERISTICS: Over operating ranges

Symbol	Characteristics	Test Conditions		C Min.	C Max.	I Min.	I Max.	M/B Min.	M/B Max.	Unit
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-16	+16	-16	+16	-16	+16	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}		-16	+16	-16	+16	-16	+16	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	X32		195		195		195	mA
			X16		105		105		105	
			X8		60		60		60	
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA	X32		255		275		295	mA
			X16		135		145		155	
			X8		75		80		85	
I_{SB1}	Full Standby Supply Current (CMOS)	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ + 0.2V, $\overline{CE} \geq V_{DD}$ -0.2V			1		1.8		2.6	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}			20		20		20	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA			0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA		2.4		2.4		2.4		V

DPS6434-120, -150 DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	TYP.	Max.	Unit
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V, $\overline{CE} \geq V_{DD}$ -0.2V		6	200	µA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V, $\overline{CE} \geq V_{DD}$ -0.2V		8	220	µA
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	5			ms

RECOMMENDED OPERATING RANGE[1]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	

ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} +0.5	V

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TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	H*	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

* If $\overline{OE}$ is LOW during Write, t_{WHZ} must be observed before data is presented to the device.

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	80	pF	V_{IN} = 0V
C_{CE}	Chip Enable	20		
C_{WE}	Write Enable	50		
C_{OE}	Output Enable	80		
$C_{I/O}$	Data Input/Output	20		

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

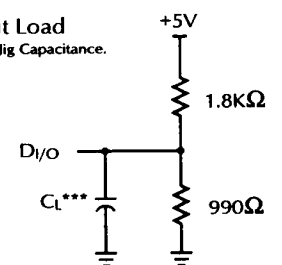
** Transition between 0.8V and 2.2V.

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 2.1mA	-	0.4	V

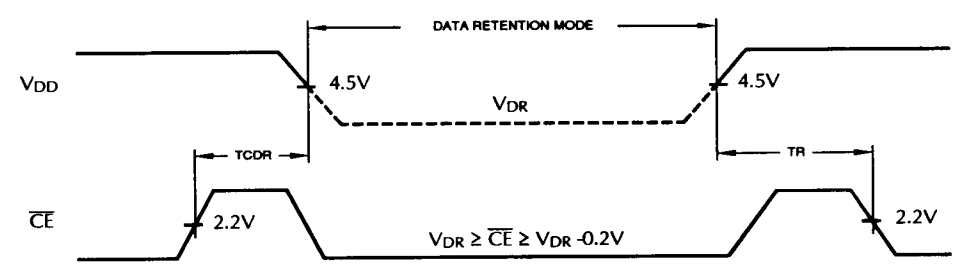
OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{WLZ}
2	5 pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{WLZ}

Figure 1. Output Load

*** Including Probe and Jig Capacitance.



DATA RETENTION WAVEFORM



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

No.	Symbol	Parameter	-35		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	35		45		55		70		ns
2	t_{AA}	Address Access Time		35		45		55		70	ns
3	t_{CO}	Chip Enable to Output Valid		35		45		55		70	ns
4	t_{OV}	Output Enable to Output Valid		25		25		35		40	ns
5	t_{OH}	Output Hold from Address Change	3		3		3		3		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	0		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		15		20		25		30	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		15		20		25		30	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]

No.	Symbol	Parameter	-35		-45		-55		-70		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	35		45		55		70		ns
11	t_{AW}	Address Valid to End of Write	30		40		50		65		ns
12	t_{CW}	Chip Enable to End of Write	30		40		50		65		ns
13	t_{DW}	Data Valid to End of Write	20		25		25		30		ns
14	t_{DH}	Data Hold Time	3		3		3		3		ns
15	t_{WP}	Write Pulse Width	30		40		50		60		ns
16	t_{AS}	Address Set-up Time*	0		0		0		0		ns
17	t_{AH}	Address Hold Time	0		0		0		0		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		15		20		25		30	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

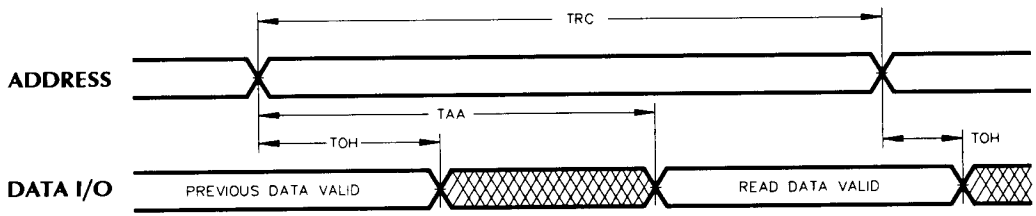
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	85		100		120		150		ns
2	t_{AA}	Address Access Time		85		100		120		150	ns
3	t_{CO}	Chip Enable to Output Valid		85		100		120		150	ns
4	t_{OV}	Output Enable to Output Valid		60		60		60		70	ns
5	t_{OH}	Output Hold from Address Change	5		10		10		10		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 6]	10		10		10		10		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 6]		30		35		40		50	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 6]		30		35		40		50	ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [7]

No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	85		100		120		150		ns
11	t_{AW}	Address Valid to End of Write	75		90		100		120		ns
12	t_{CW}	Chip Enable to End of Write	75		90		100		120		ns
13	t_{DW}	Data Valid to End of Write	35		40		50		60		ns
14	t_{DH}	Data Hold Time	0		0		0		0		ns
15	t_{WP}	Write Pulse Width	75		80		90		100		ns
16	t_{AS}	Address Set-up Time*	0		0		0		0		ns
17	t_{AH}	Address Hold Time	0		0		0		0		ns
18	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 6]		25		35		40		50	ns
19	t_{WLZ}	Write Enable to Output in LOW-Z [4, 6]	5		5		5		5		ns

* Valid for both Read and Write Cycles.

READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



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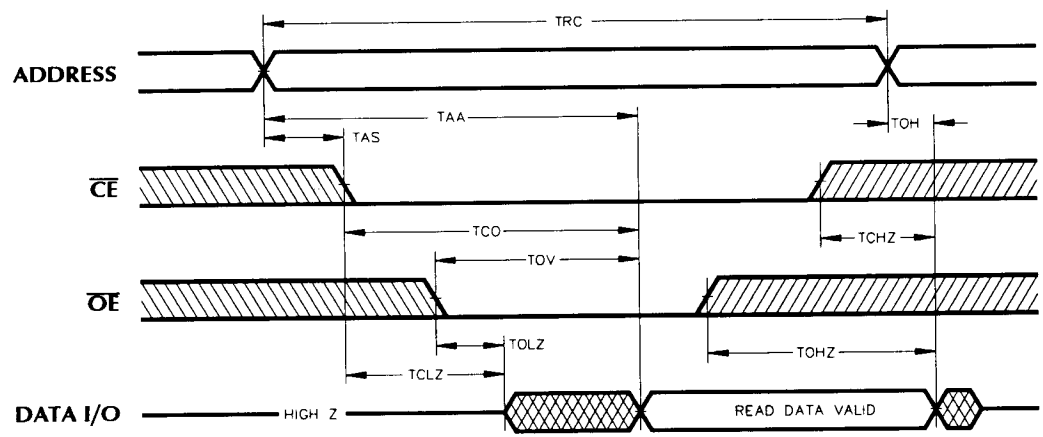
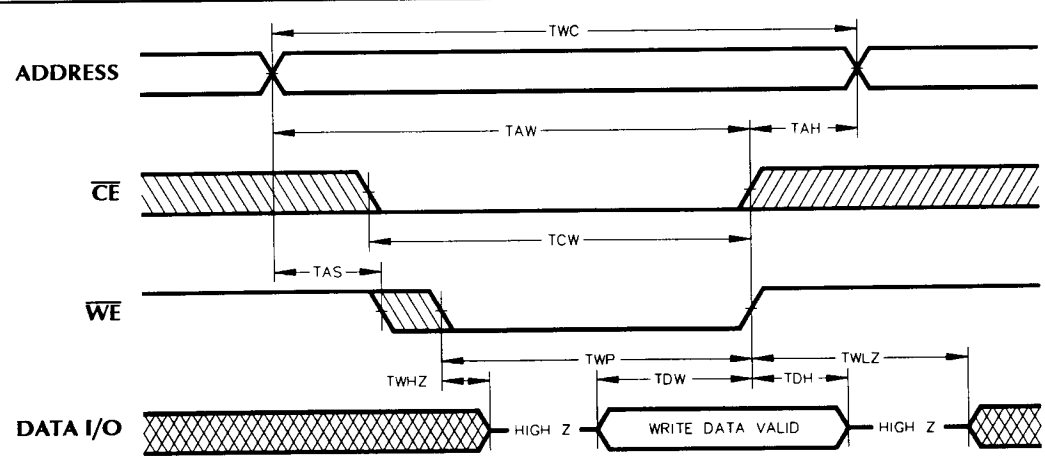
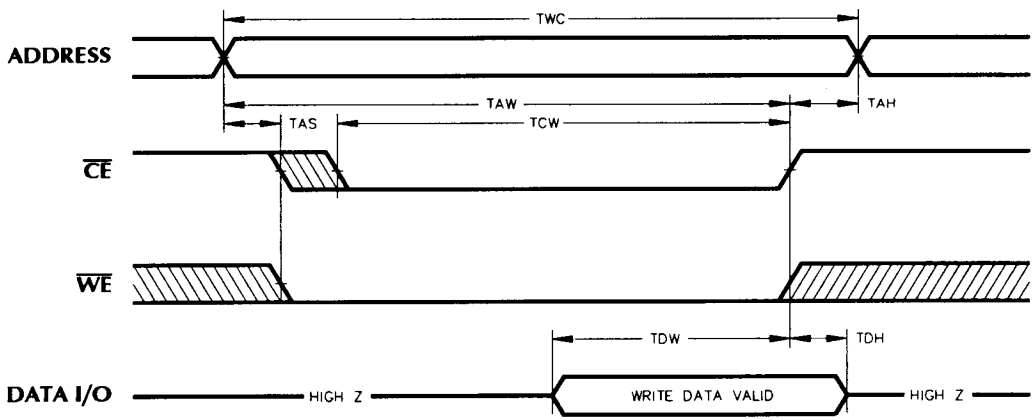
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



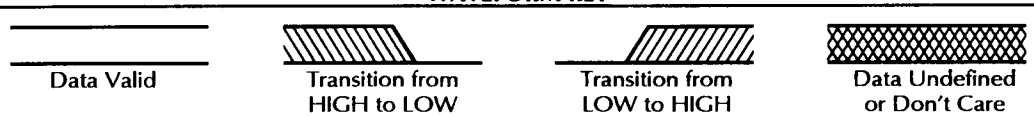
WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min.= -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WAVEFORM KEY



ORDERING INFORMATION

DP — PREFIX
S6434 — DEVICE TYPE
XXX — SPEED
X — GRADE

GRADE		
C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	−40°C to +85°C
M	MILITARY	−55°C to +125°C
B*	MIL−PROCESSED	−55°C to +125°C

SPEED	
35	35ns
45	45ns
55	55ns
70	70ns
85	85ns
100	100ns
120	120ns
150	150ns

S6434 — CMOS SRAM 64KX32, 128KX16 or 256KX8

* B grade modules can be constructed with 883 devices.

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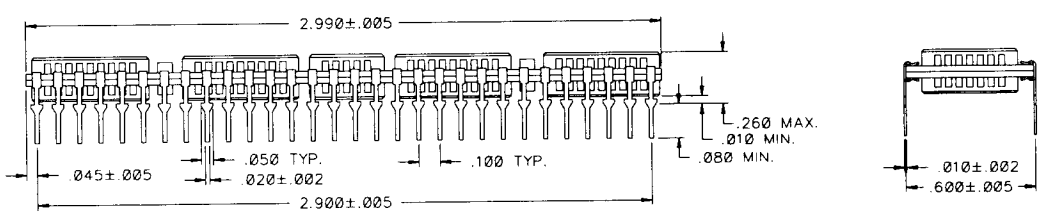
MECHANICAL DRAWING



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