NEC

MOS INTEGRATED CIRCUIT

μPD444001

4M-BIT CMOS FAST SRAM
4M-WORD BY 1-BIT

Description

The μPD444001 is a high speed, low power, 4,194,304 bits (4,194,304 words by 1 bit) CMOS static RAM.

Operating supply voltage is 5.0 V ± 0.5 V.

★ The μPD444001 is packaged in 32-pin PLASTIC SOJ.

Features

- 4,194,304 words by 1 bit organization
- Fast access time : 10, 11, 12 ns (MAX.)
- Output Enable input for easy application
- Single +5.0 V power supply

★ Ordering Information

Part number	Package	Access time	Supply current mA (MAX.)	
		ns (MAX.)	At operating	At standby
μPD444001LE-10	32-pin PLASTIC SOJ (10.16 mm (400))	10	170	10
μPD444001LE-11		11	160	
μPD444001LE-12		12	150	

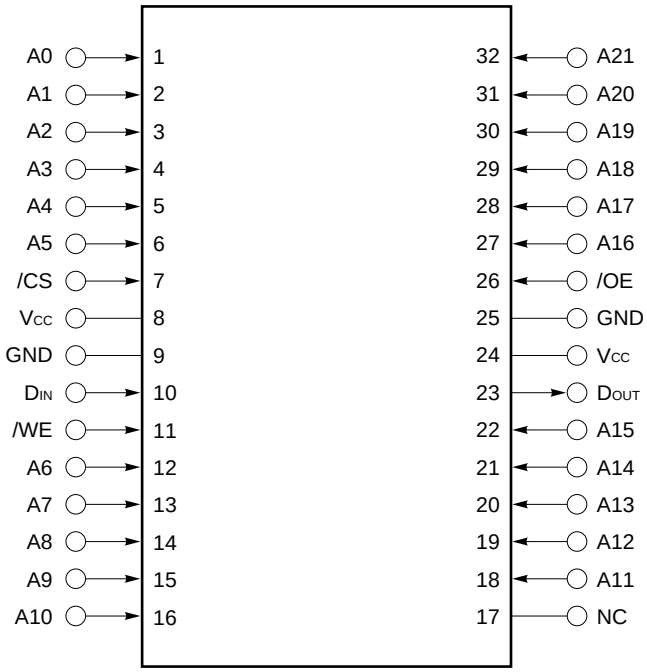
Document No. M14947EJ4V0DS00 (4th edition)
Date Published May 2002 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

★ Pin Configuration (Marking Side)

/xxx indicates active low signal.

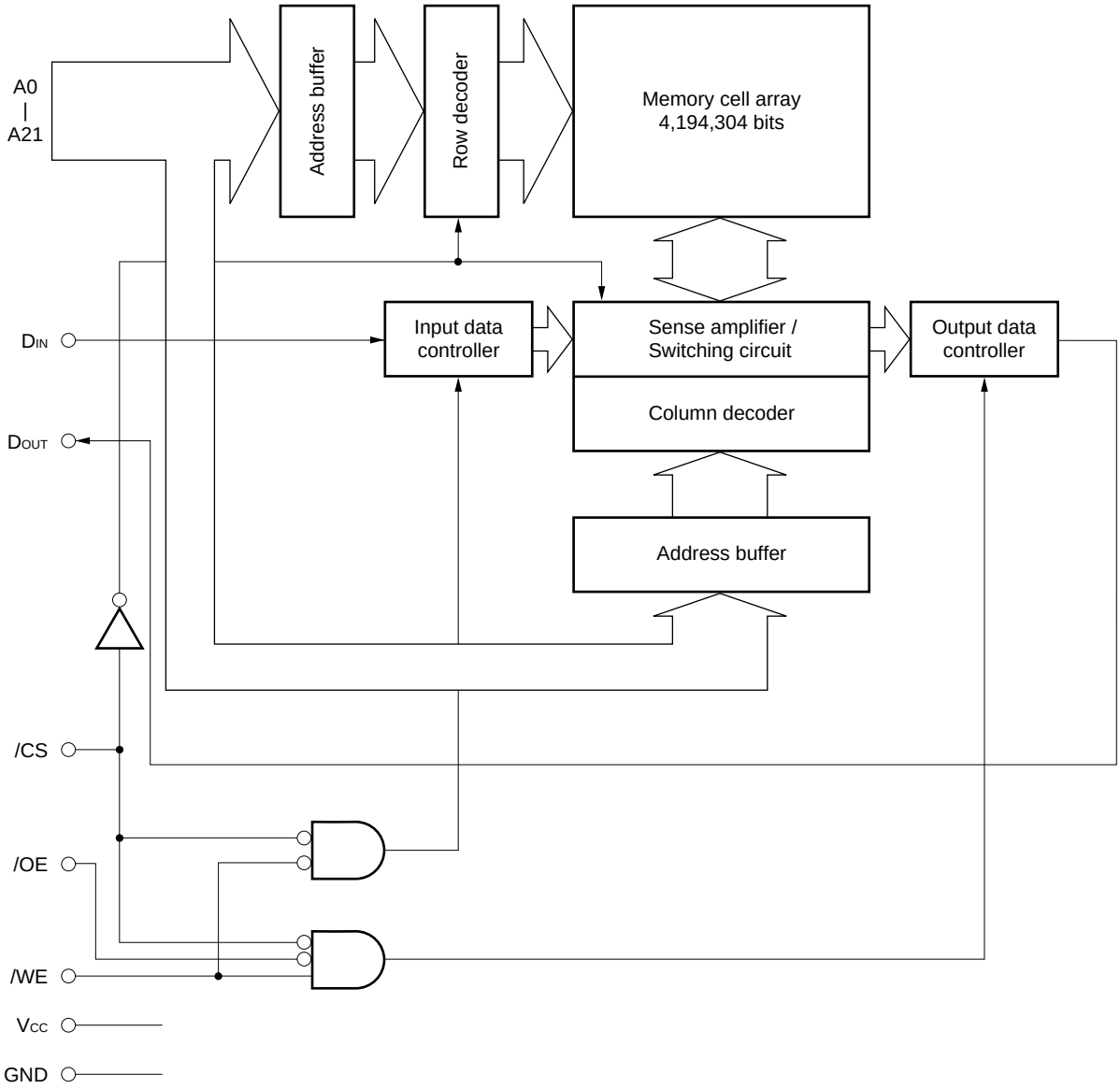
32-pin PLASTIC SOJ (10.16 mm (400))



A0 - A21	:	Address Inputs
D_{IN}	:	Data Input
D_{OUT}	:	Data Output
/CS	:	Chip Select
/WE	:	Write Enable
/OE	:	Output Enable
V_{CC}	:	Power supply
GND	:	Ground
NC	:	No connection

Remark Refer to **Package Drawing** for the 1-pin index mark.

Block Diagram



Truth Table

/CS	/OE	/WE	Mode	I/O	Supply current
H	×	×	Not selected	High impedance	I_{SB}
L	L	H	Read	D_{OUT}	I_{CC}
L	×	L	Write	D_{IN}	
L	H	H	Output disable	High impedance	

Remark × : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 Note to +7.0	V
Input / Output voltage	V_T		–0.5 Note to V_{CC}+0.5	V
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –2.0 V (MIN.) (pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.2		V_{CC} + 0.5	V
Low level input voltage	V_{IL}		–0.5 Note		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Note –2.0 V (MIN.) (pulse width : 2 ns)

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–2		+2	μA
Output leakage current	I_{LO}	V_{OUT} = 0 V to V_{CC}, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL}		–2		+2	μA
Operating supply current	I_{CC}	/CS = V_{IL},	Cycle time : 10 ns			170	mA
		I_{OUT} = 0 mA,	Cycle time : 11 ns			160	
		Minimum cycle time	Cycle time : 12 ns			150	
Standby supply current	I_{SB}	/CS = V_{IH}, V_{IN} = V_{IH} or V_{IL}				40	mA
	I_{SB1}	/CS ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V				10	
High level output voltage	V_{OH}	I_{OH} = –4.0 mA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = +8.0 mA				0.4	V

★ **Remark** V_{IN} : Input voltage

V_{OUT} : Output voltage

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V			8	pF

Remarks 1. V_{IN} : Input voltage

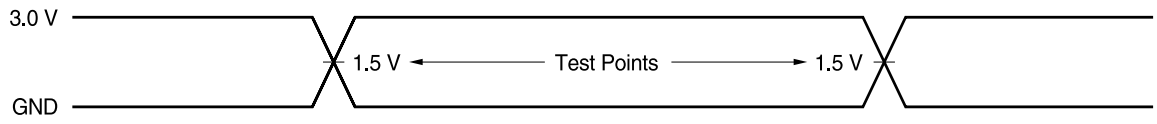
V_{OUT} : Output voltage

★ **2.** These parameters are periodically sampled and not 100% tested.

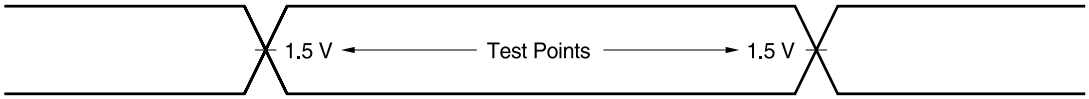
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 3 ns)



Output Waveform



Output Load

AC characteristics directed with the note should be measured with the output load shown in **Figure 1** or **Figure 2**.

Figure 1

(for t_{AA}, t_{ACS}, t_{OE}, t_{OH})

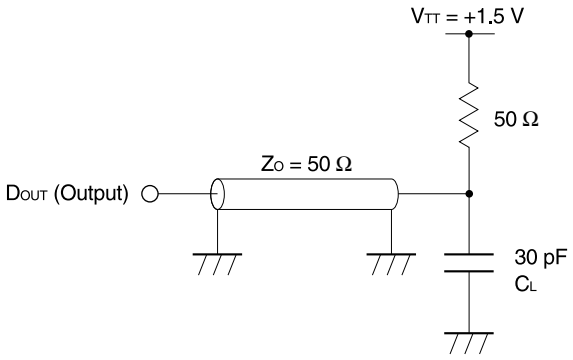
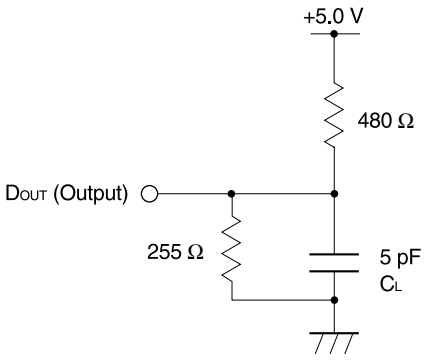


Figure 2

(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW})



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

★ **Read Cycle**

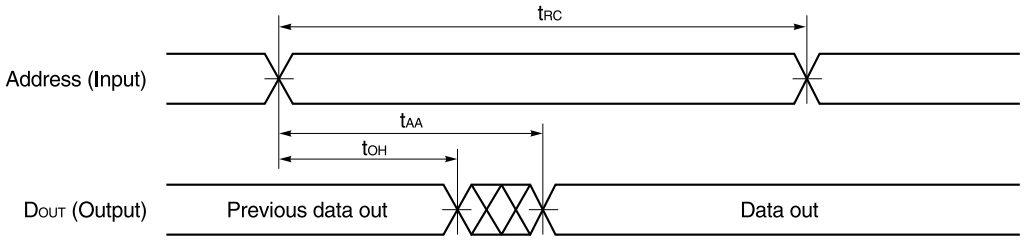
Parameter	Symbol	-10		-11		-12		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	10		11		12		ns	
Address access time	t_{AA}		10		11		12	ns	1
/CS access time	t_{ACS}		10		11		12	ns	
/OE access time	t_{OE}		5		5		6	ns	
Output hold from address change	t_{OH}	3		3		3		ns	
/CS to output in low impedance	t_{CLZ}	3		3		3		ns	2, 3
/OE to output in low impedance	t_{OLZ}	0		0		0		ns	
/CS to output in high impedance	t_{CHZ}		5		6		6	ns	
/OE to output hold in high impedance	t_{OHZ}		5		5		6	ns	

Notes 1. See the output load shown in **Figure 1**.

2. Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.

3. These parameters are periodically sampled and not 100% tested.

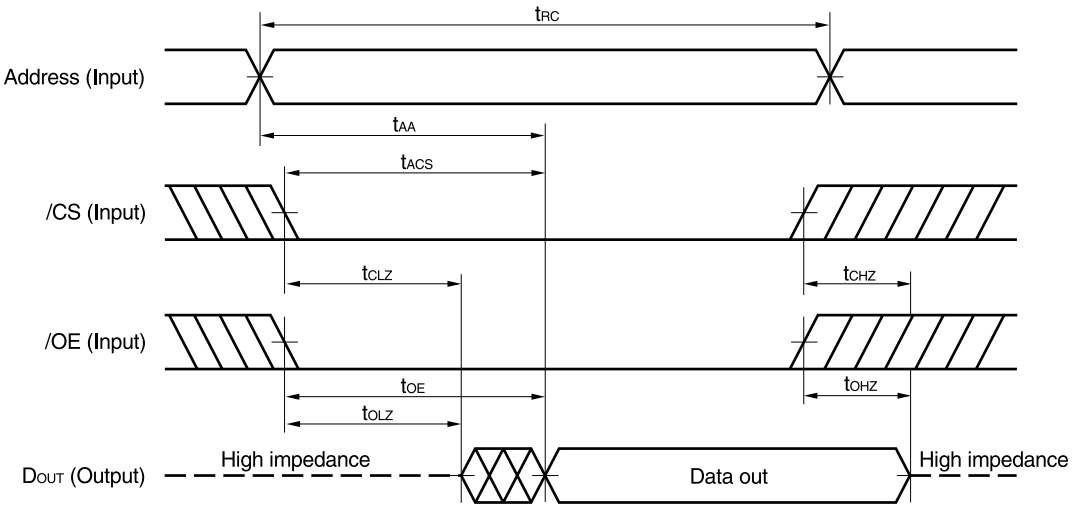
Read Cycle Timing Chart 1 (Address Access)



Remarks 1. In read cycle, /WE should be fixed to high level.

2. /CS = /OE = V_{IL}

Read Cycle Timing Chart 2 (/CS Access)



Caution Address valid prior to or coincident with /CS low level input.

Remark In read cycle, /WE should be fixed to high level.

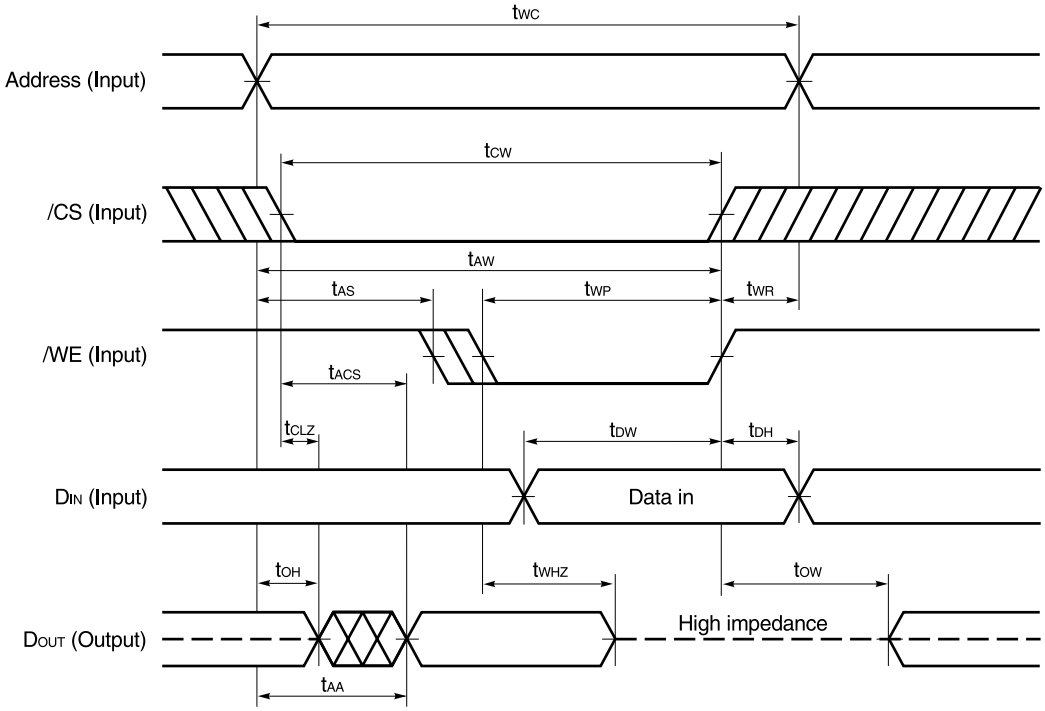
★ **Write Cycle**

Parameter	Symbol	-10		-11		-12		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	10		11		12		ns	
/CS to end of write	t_{CW}	7		7.5		8		ns	
Address valid to end of write	t_{AW}	7		7.5		8		ns	
Write pulse width	t_{WP}	7		8		8		ns	
Data valid to end of write	t_{DW}	5		5		6		ns	
Data hold time	t_{DH}	0		0		0		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write recovery time	t_{WR}	1		1		1		ns	
/WE to output in high impedance	t_{WHZ}		5		5		6	ns	1, 2
Output active from end of write	t_{OW}	3		3		3		ns	

Notes 1. Transition is measured at ± 200 mV from steady-state voltage with the output load shown in **Figure 2**.

2. These parameters are periodically sampled and not 100% tested.

Write Cycle Timing Chart 1 (/WE Controlled)



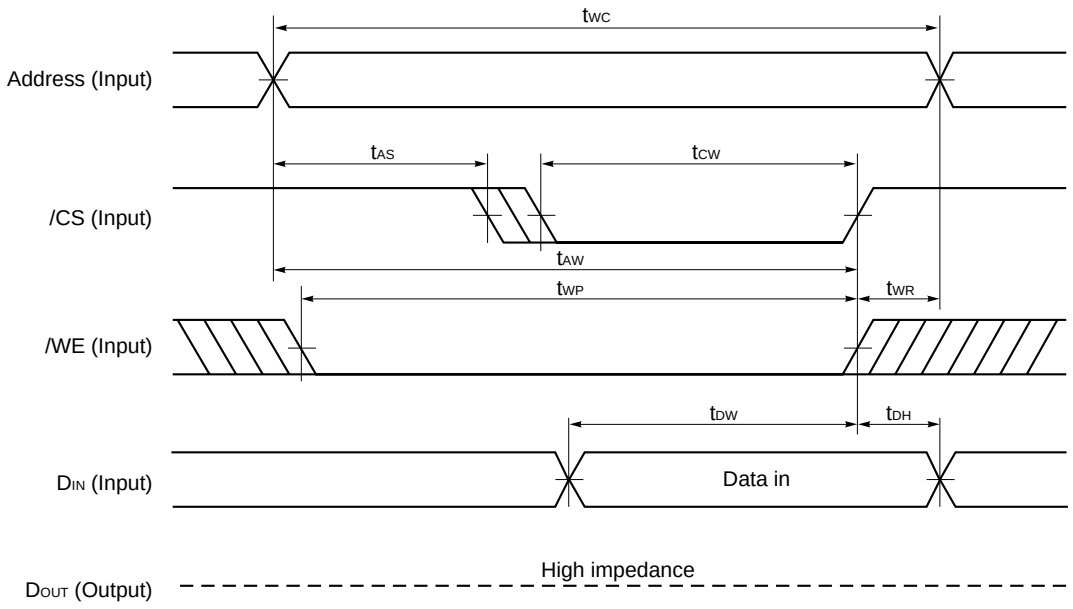
Cautions 1. /CS or /WE should be fixed to high level during address transition.

2. Do not input data to DOUT while DOUT is in the output state.

Remarks 1. Write operation is done during the overlap time of a low level /CS and a low level /WE.

2. When /WE is at low level, the DOUT pin is always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the DOUT pin high impedance.

Write Cycle Timing Chart 2 (/CS Controlled)



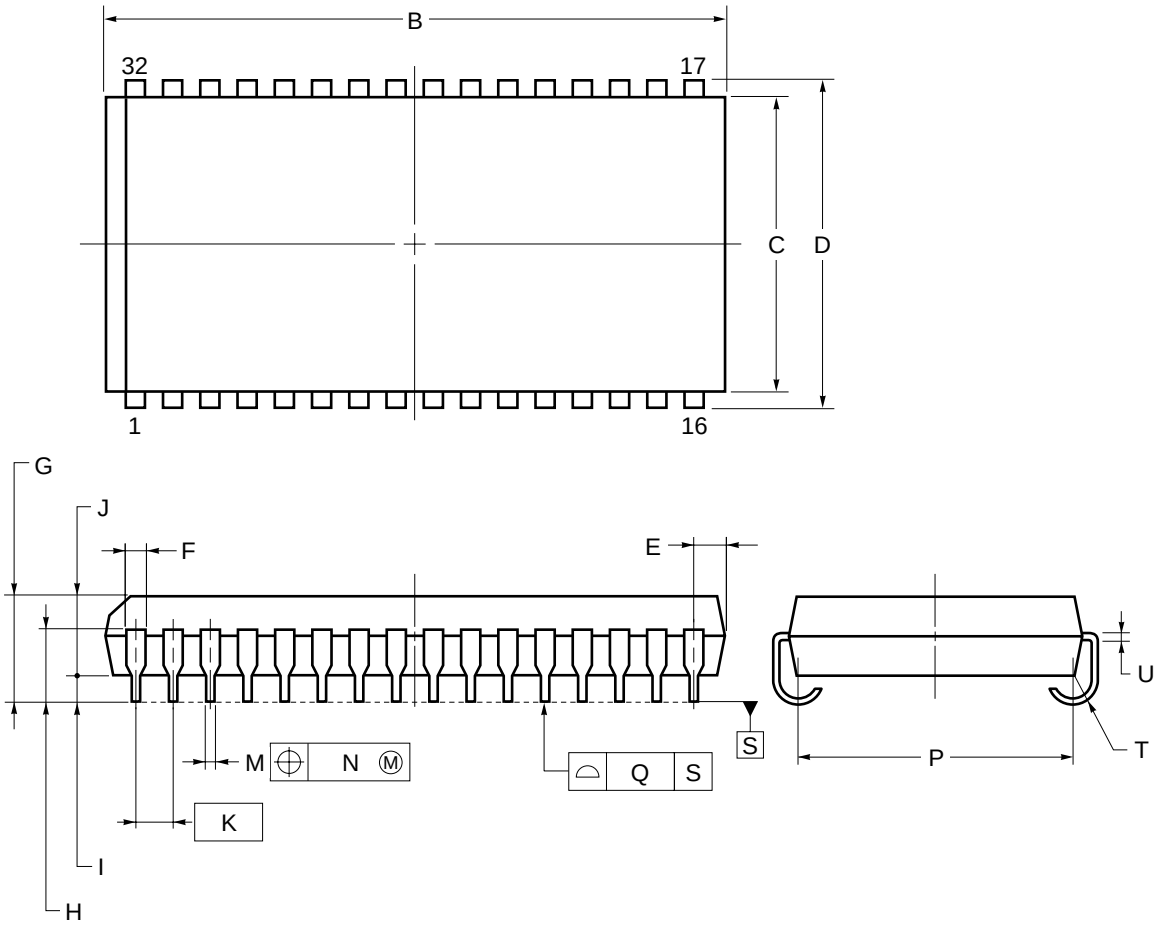
Cautions 1. /CS or /WE should be fixed to high level during address transition.

2. Do not input data to DOUT while DOUT is in the output state.

Remark Write operation is done during the overlap time of a low level /CS and a low level /WE.

★ **Package Drawing**

32-PIN PLASTIC SOJ (10.16mm (400))



NOTE
Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
B	21.26±0.2
C	10.16
D	11.18±0.2
E	1.005±0.1
F	0.74
G	3.5±0.2
H	2.545±0.2
I	0.8 MIN.
J	2.6
K	1.27(T.P.)
M	0.40±0.10
N	0.12
P	9.4±0.20
Q	0.1
T	R0.85
U	$0.20^{+0.10}_{-0.05}$

P32LE-400A-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD444001.

★ **Type of Surface Mount Device**

μPD444001LE : 32-pin PLASTIC SOJ (10.16 mm (400))

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
4th edition/ May 2002	p.1, 2, 12, 13	p.1, 2, 13, 14	Deletion	Ordering Information, Pin Configuration, Package Drawing, Type of Surface Mount Device	32-pin PLASTIC TSOP (II)
	p.5	p.5	Deletion	DC Characteristics	Remark2
			Modification	Capacitance	Remark2
	p.7, 9	p.7, 9	Modification	Read Cycle, Write Cycle	Note3
			Deletion		Remark

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

- **The information in this document is current as of May, 2002. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.

  (Note)

  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.

  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4