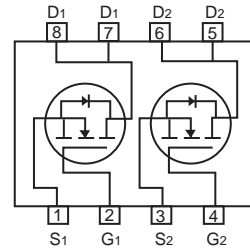
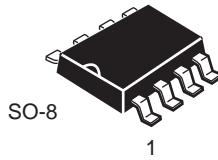


Dual N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 20V, 6.0A, $R_{DS(ON)} = 36m\Omega$ @ $V_{GS} = 10V$.
 $R_{DS(ON)} = 42m\Omega$ @ $V_{GS} = 4.5V$.
 $R_{DS(ON)} = 75m\Omega$ @ $V_{GS} = 2.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead free product is acquired.
- Surface mount Package.



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	6.0	A
Drain Current-Pulsed ^a	I_{DM}	24	A
Maximum Power Dissipation	P_D	2.0	W
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient ^b	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$



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Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current	I_{GSS}	$V_{GS} = 12V, V_{DS} = 0V$			± 100	nA
On Characteristics^c						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	0.5		1.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6.0A$		30	36	$m\Omega$
		$V_{GS} = 4.5V, I_D = 4.3A$		35	42	$m\Omega$
		$V_{GS} = 2.5V, I_D = 3.5A$		58	75	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS} = 10V, I_D = 4.3A$		7		S
Dynamic Characteristics^d						
Input Capacitance	C_{iss}	$V_{DS} = 15V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		511		pF
Output Capacitance	C_{oss}			216		pF
Reverse Transfer Capacitance	C_{rss}			73		pF
Switching Characteristics^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10V, I_D = 1A,$ $V_{GS} = 4.5V, R_{GEN} = 6\Omega$		20	50	ns
Turn-On Rise Time	t_r			12	30	ns
Turn-Off Delay Time	$t_{d(off)}$			50	100	ns
Turn-Off Fall Time	t_f			10	25	ns
Total Gate Charge	Q_g	$V_{DS} = 10V, I_D = 5.4A,$ $V_{GS} = 4.5V$		11	15	nC
Gate-Source Charge	Q_{gs}			3.6		nC
Gate-Drain Charge	Q_{gd}			2.8		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				1.7	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = 1.7A$			1.3	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10$ sec. c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. d.Guaranteed by design, not subject to production testing.						



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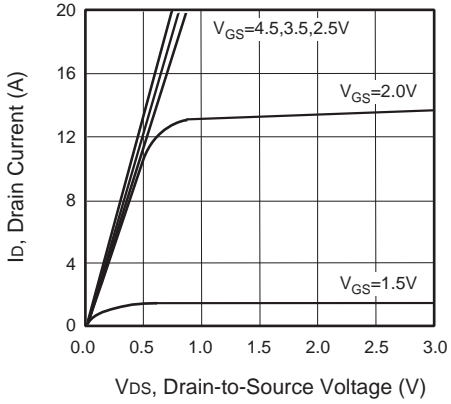


Figure 1. Output Characteristics

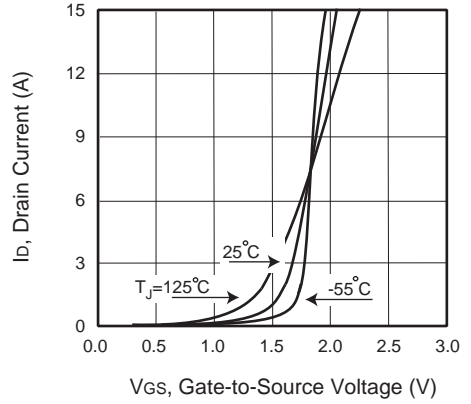


Figure 2. Transfer Characteristics

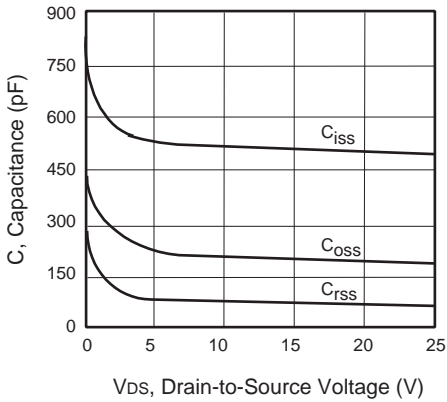


Figure 3. Capacitance

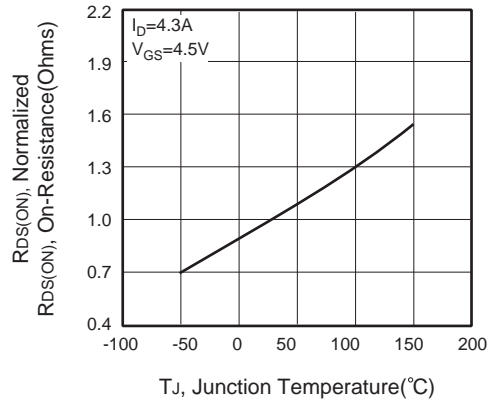


Figure 4. On-Resistance Variation with Temperature

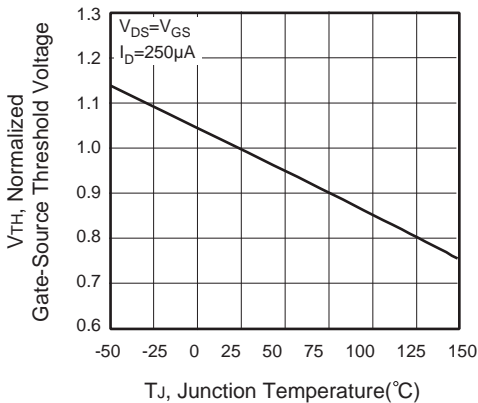


Figure 5. Gate Threshold Variation with Temperature

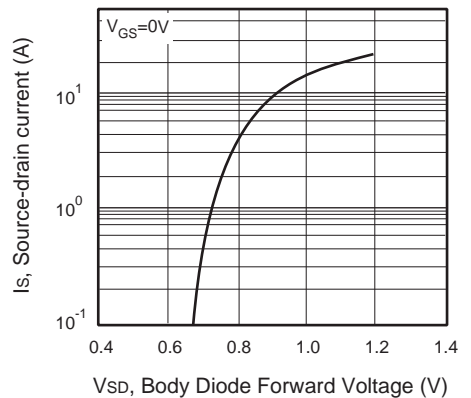


Figure 6. Body Diode Forward Voltage Variation with Source Current



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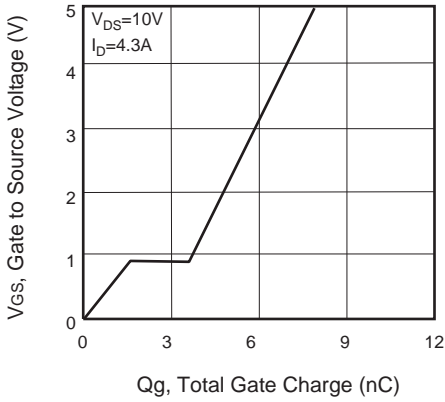


Figure 7. Gate Charge

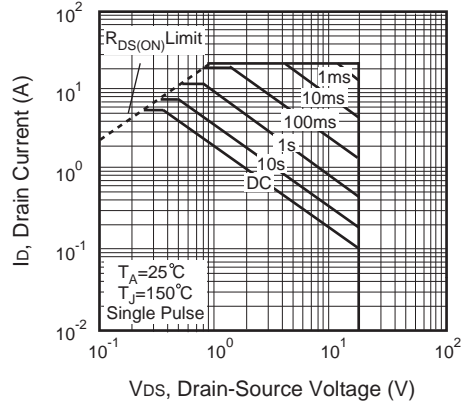


Figure 8. Maximum Safe Operating Area

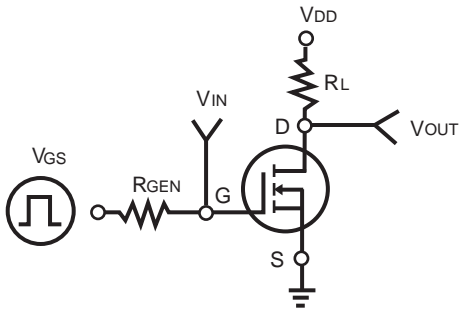


Figure 9. Switching Test Circuit

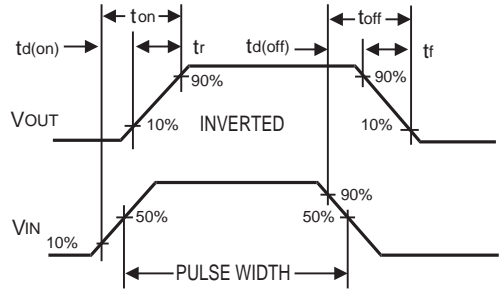


Figure 10. Switching Waveforms

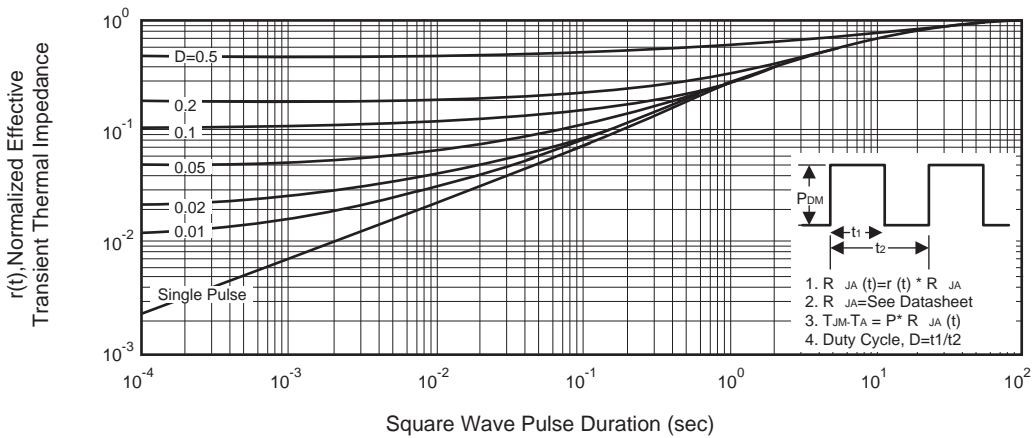


Figure 11. Normalized Thermal Transient Impedance Curve