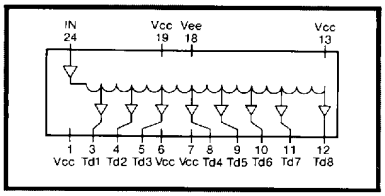
T-47-13
T-47-17

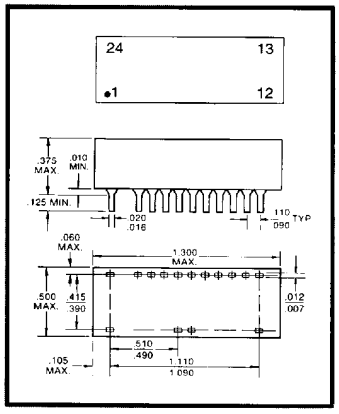
100K ECL Delay Modules

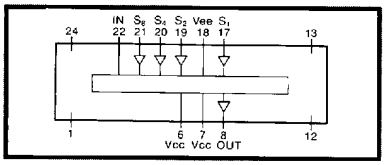
Part No.	T_{d1} ns	T_{d2} ns	T_{d3} ns	T_{d4} ns	T_{d5} ns	T_{d6} ns	T_{d7} ns	T_{d8} ns	T_d TOL. WIG.	Output Rise Time Max. (ns)
EKLDL005	1.2	2.2	2.5	3.0	3.5	4.0	4.5	5.0	±.25 or 10%	2.0
EKLDL008	1.2	2.2	3.0	4.0	5.0	6.0	7.0	8.0	±.45 or 5%	2.0
EKLDL016	2.0	4.0	6.0	8.0	10.0	12.0	14.0	16.0	±.50 or 5%	2.0
EKLDL025	4.0	7.0	10.0	13.0	16.0	19.0	22.0	25.0	±1.ns or 5%	2.0
EKLDL032	4.0	8.0	12.0	16.0	20.0	24.0	28.0	32.0	±1.5 or 5%	2.0
EKLDL040	5.0	10.0	15.0	20.0	25.0	30.0	35.0	40.0	±1.5 or 5%	2.0
EKLDL048	6.0	12.0	18.0	24.0	30.0	36.0	42.0	48.0	±1.5 or 5%	2.4
EKLDL056	7.0	14.0	21.0	28.0	35.0	42.0	49.0	56.0	±1.5 or 5%	2.8
EKLDL064	8.0	16.0	24.0	32.0	40.0	48.0	56.0	64.0	±1.5 or 5%	3.2
EKLDL072	9.0	18.0	27.0	36.0	45.0	54.0	63.0	72.0	±1.5 or 5%	3.6
EKLDL080	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	±1.5 or 5%	4.0
EKLDL100	12.5	25.0	37.5	50.0	62.5	75.0	87.5	100.0	±1.5 or 5%	5.0
EKLDL120	15.0	30.0	45.0	60.0	75.0	90.0	105.0	120.0	±1.5 or 5%	6.0
EKLDL160	20.0	40.0	60.0	80.0	100.0	120.0	140.0	160.0	±1.5 or 5%	8.0
EKLDL200	25.0	50.0	75.0	100.0	125.0	150.0	175.0	200.0	±1.5 or 5%	10.0

Delay characteristics V_{ee} = −4.5 ±.01Vdc and T_a = 25°C.
Delay time measured @ −1.3V level.
500 linear FPM airflow and output terminated with 50 ohm to −2.0 Vdc.
Rise time measured from 20 to 80% of output pulse.
For minimum input pulse width—contact factory.



Dimensions applicable to all modules on this page.





Part No.	Step Delay ns ± ns	Max. Delay ns ± ns	Output Rise Time Max (ns)
EKLPGR25	0.25 ± 0.13	5.25 ± 1.0	2.0
EKLPGR50	0.50 ± 0.20	9.00 ± 1.0	2.0
EKLPGR75	0.75 ± 0.25	12.75 ± 1.5	2.0
EKLPG010	1.00 ± 0.40	16.50 ± 1.5	2.0
EKLPG015	1.50 ± 0.50	24.00 ± 1.5	2.0
EKLPG020	2.00 ± 0.50	31.50 ± 1.5	2.0
EKLPG025	2.50 ± 0.50	39.00 ± 2.0	2.0
EKLPG030	3.00 ± 0.75	46.50 ± 2.5	2.0
EKLPG035	3.50 ± 0.75	54.00 ± 2.5	2.0
EKLPG040	4.00 ± 1.00	61.50 ± 3.0	2.0
EKLPG045	4.50 ± 1.00	69.00 ± 3.0	2.0
EKLPG050	5.00 ± 1.00	76.50 ± 4.0	2.0
EKLPG060	6.00 ± 1.00	91.50 ± 5.0	2.0
EKLPG070	7.00 ± 1.00	106.50 ± 5.0	2.0
EKLPG080	8.00 ± 1.00	121.50 ± 6.0	2.0
EKLPG090	9.00 ± 1.50	136.50 ± 7.0	2.0
EKLPG100	10.00 ± 1.50	151.50 ± 8.0	2.0

Delay characteristics V_{ee} = −4.5 ±.01Vdc and T_a = 25°C.
All delay times measured @ −1.3V level.
500 linear FPM airflow and output terminated with 50 ohm to −2.0 Vdc.
Rise time measured from 20 to 80% of output pulse.
Input is internally terminated; therefore the delay line driver does not require a pull-down resistor. For minimum input pulse width—contact factory.

100k ECL Delay Modules

- 100k ECL input and output.
- 24-pin transfer-molded DIP on .400 lead center.
- Available in delays from 5 ns to 200 ns.
- 8 equal taps each buffered with 70 ECL fanout capacity.
- Operating temperature range 0 to 85°C.
- Other delays available.
- Fanout: 70 ECL loads.

Notes
Only the pins specified in the schematics are provided with each package.
Pin numbers shown are for reference only and are not necessarily marked on unit.
Lead material is electro tin plated (alloy 42) or solder dipped.
All specifications are subject to change without notice.

100k ECL Programmable Delay Modules

- 100k ECL input and output.
- 24-pin transfer-molded DIP on .400 lead center.
- 4-bit binary programming gives 15 equal step delays.
- Available in 18 step delays from 0.10 ns to 10 ns; other step delays available.
- Low inherent delay (T_O); T_O = 1.5 ±1.0 ns.
- Temperature range 0 to ±85°C.
- Fanout: 70 ECL loads