

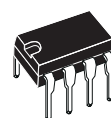
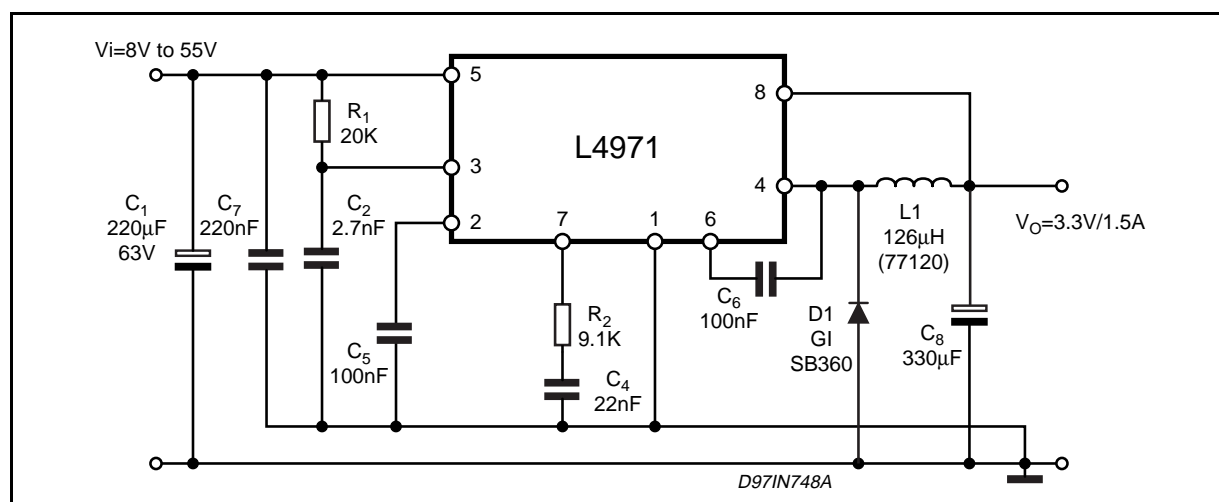
## 1.5A STEP DOWN SWITCHING REGULATOR

- UP TO 1.5A STEP DOWN CONVERTER
- OPERATING INPUT VOLTAGE FROM 8V TO 55V
- PRECISE 3.3V ( $\pm 1\%$ ) INTERNAL REFERENCE VOLTAGE
- OUTPUT VOLTAGE ADJUSTABLE FROM 3.3V TO 50V
- SWITCHING FREQUENCY ADJUSTABLE UP TO 300KHz
- VOLTAGE FEEDFORWARD
- ZERO LOAD CURRENT OPERATION
- INTERNAL CURRENT LIMITING (PULSE-BY-PULSE AND HICCUP MODE)
- INHIBIT FOR ZERO CURRENT CONSUMPTION
- PROTECTION AGAINST FEEDBACK DISCONNECTION
- THERMAL SHUTDOWN
- SOFT START FUNCTION

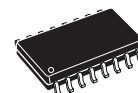
### DESCRIPTION

The L4971 is a step down monolithic power switching regulator delivering 1.5A at a voltage between 3.3V and 50V (selected by a simple external divider). Realized in BCD mixed technology, the device uses an internal power D-MOS transistor (with a typical  $R_{ds(on)}$  of  $0.25\Omega$ ) to obtain very high efficiency and high switching speed.

### TYPICAL APPLICATION CIRCUIT



Minidip



SO16W

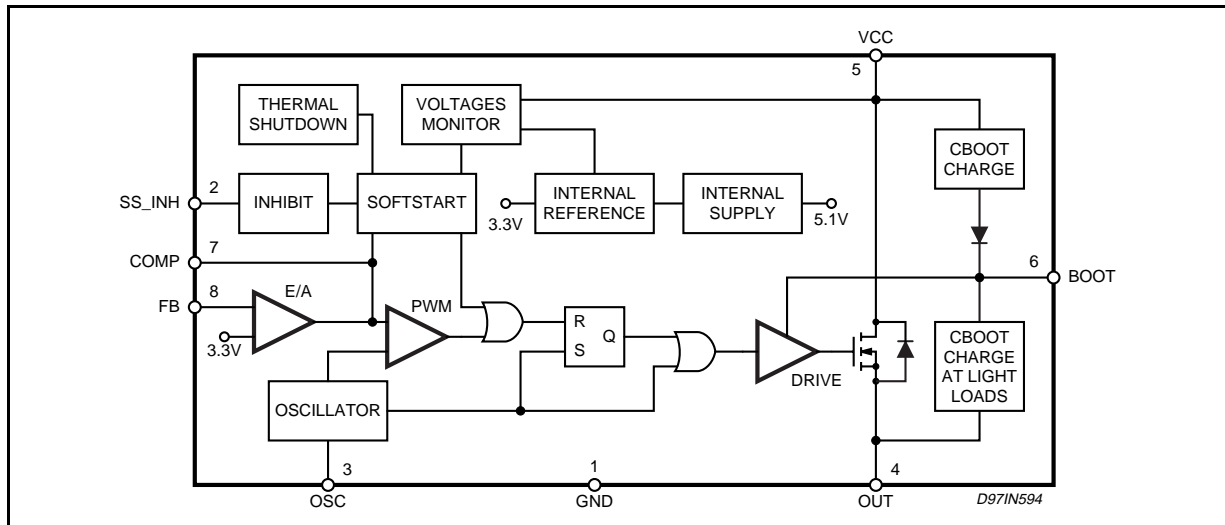
**ORDERING NUMBERS:** L4971 (Minidip)  
L4971D (SO16)

A switching frequency up to 300KHz is achievable (the maximum power dissipation of the packages must be observed).

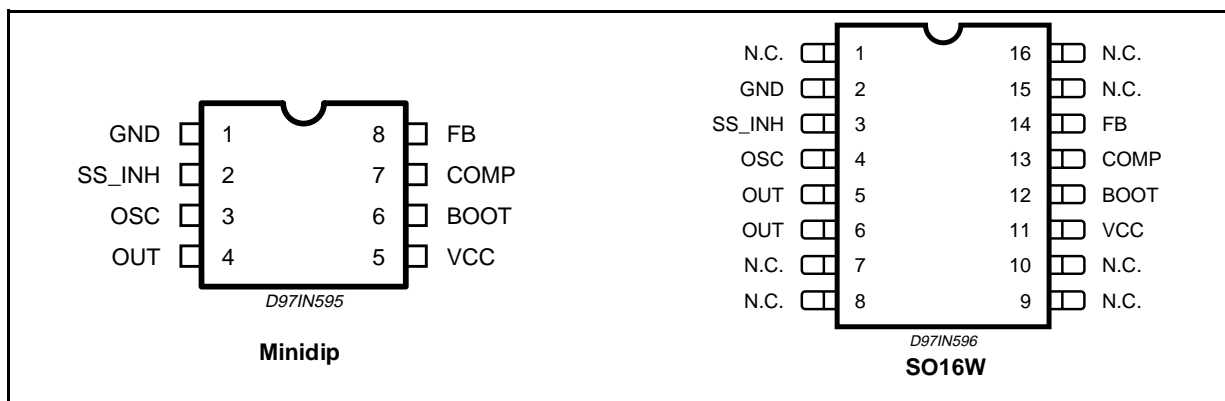
A wide input voltage range between 8V to 55V and output voltages regulated from 3.3V to 50V cover the majority of today's applications. Features of this new generations of DC-DC converter include pulse-by-pulse current limit, hiccup mode for short circuit protection, voltage feedforward regulation, soft-start, protection against feedback loop disconnection, inhibit for zero current consumption and thermal shutdown.

The device is available in plastic dual in line, MINIDIP 8 for standard assembly, and SO16W for SMD assembly.

**BLOCK DIAGRAM**



**PIN CONNECTIONS**



**PIN FUNCTIONS**

DIP	SO (*)	Name	Function
1	2	GND	Ground
2	3	SS_INH	A logic signal (active low) disables the device (sleep mode operation). A capacitor connected between this pin and ground determines the soft start time. When this pin is grounded disables the device (driven by open collector/drain).
3	4	OSC	An external resistor connected between the unregulated input voltage and this pin and a capacitor connected from this pin to ground fix the switching frequency. (Line feed forward is automatically obtained)
4	5, 6	OUT	Stepdown regulator output
5	11	V <sub>CC</sub>	Unregulated DC input voltage
6	12	BOOT	A capacitor connected between this pin and OUT allows to drive the internal DMOS Transistor
7	13	COMP	E/A output to be used for frequency compensation
8	14	FB	Stepdown feedback input. Connecting directly to this pin results in an output voltage of 3.3V. An external resistive divider is required for higher output voltages.

(\*) Pins 1, 7, 8, 9, 10, 15 and 16 are not internally, electrically connected to the die.

## THERMAL DATA

Symbol	Parameter	Max.	Minidip	SO16	Unit
$R_{th(j-amb)}$	Thermal Resistance Junction to ambient	Max.	90 (*)	110 (*)	°C/W

(\*) Package mounted on board.

## ABSOLUTE MAXIMUM RATINGS

Symbol		Parameter	Value	Unit	
Minidip	SO16				
$V_5$	$V_{11}$	Input voltage	58	V	
$V_4$	$V_5, V_6$	Output DC voltage	-1	V	
		Output peak voltage at $t = 0.1\mu s$ $f = 200kHz$	-5	V	
$I_4$	$I_5, I_6$	Maximum output current	int. limit.		
$V_6 - V_5$	$V_{12} - V_{11}$		14	V	
$V_6$	$V_{12}$	Bootstrap voltage	70	V	
$V_7$	$V_{13}$	Analogs input voltage ( $V_{CC} = 24V$ )	12	V	
$V_2$	$V_3$	Analogs input voltage ( $V_{CC} = 24V$ )	13	V	
$V_8$	$V_{14}$	( $V_{CC} = 20V$ )	6	V	
			-0.3	V	
$P_{tot}$		Power dissipation a $T_{amb} \leq 60^\circ C$	Minidip	1	W
			SO16	0.8	W
$T_j, T_{stg}$		Junction and storage temperature	-40 to 150	°C	

**ELECTRICAL CHARACTERISTICS** ( $T_j = 25^\circ C$ ,  $C_{osc} = 2.7nF$ ,  $R_{osc} = 20k\Omega$ ,  $V_{CC} = 24V$ , unless otherwise specified.) \* Specification Referred to  $T_j$  from 0 to  $125^\circ C$

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	
<b>DYNAMIC CHARACTERISTIC</b>							
$V_i$	Operating input voltage range	$V_o = 3.3$ to $50V$ ; $I_o = 1.5A$	*	8	55	V	
$V_o$	Output voltage	$I_o = 0.5A$		3.33	3.36	3.39	V
		$I_o = 0.2$ to $1.5A$		3.292	3.36	3.427	V
		$V_{CC} = 8$ to $55V$	*	3.22	3.36	3.5	V
$V_d$	Dropout voltage	$V_{CC} = 10V$ ; $I_o = 1.5A$		0.44	0.55	V	
			*		0.88	V	
$I_l$	Maximum limiting current	$V_{CC} = 8$ to $55V$	*	2	2.5	A	
	Efficiency	$V_o = 3.3V$ ; $I_o = 1.5A$		85		%	
$f_s$	Switching frequency		*	90	100	110	KHz
SVRR	Supply voltage ripple rejection	$V_i = V_{CC} + 2V_{RMS}$ ; $V_o = V_{ref}$ ; $I_o = 1.5A$ ; $f_{ripple} = 100Hz$		60			dB
	Voltage stability of switching frequency	$V_{CC} = 8$ to $55V$		3	6	%	
	Temp. stability of switching frequency	$T_j = 0$ to $125^\circ C$		4		%	
<b>Soft Start</b>							
	Soft start charge current			30	40	50	$\mu A$
	Soft start discharge current			6	10	14	$\mu A$
<b>Inhibit</b>							
$V_{LL}$	Low level voltage		*		0.9	V	
$I_{sLL}$	Isorce Low level		*	5	15	$\mu A$	

## ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>DC Characteristics</b>						
$I_{qop}$	Total operating quiescent current			4	6	mA
$I_q$	Quiescent current	Duty Cycle = 0; $V_{FB} = 3.8V$		2.5	3.5	mA
$I_{qst-by}$	Total stand-by quiescent current	$V_{inh} < 0.9V$		100	200	$\mu A$
		$V_{CC} = 55V$ ; $V_{inh} < 0.9V$		150	300	$\mu A$
<b>Error Amplifier</b>						
$V_{FB}$	Voltage Feedback Input		3.33	3.36	3.39	V
$R_L$	Line regulation	$V_{CC} = 8$ to $55V$		5	10	mV
	Ref. voltage stability vs temperature		*	0.4		mV/ $^{\circ}C$
$V_{oH}$	High level output voltage	$V_{FB} = 2.5V$	10.3			V
$V_{oL}$	Low level output voltage	$V_{FB} = 3.8V$			0.65	V
$I_{o\ source}$	Source output current	$V_{comp} = 6V$ ; $V_{FB} = 2.5V$	200	300		$\mu A$
$I_{o\ sink}$	Sink output current	$V_{comp} = 6V$ ; $V_{FB} = 3.8V$	200	300		$\mu A$
$I_b$	Source bias current			2	3	$\mu A$
SVRR E/A	Supply voltage ripple rejection	$V_{comp} = V_{fb}$ ; $V_{CC} = 8$ to $55V$	60	80		dB
	DC open loop gain	$R_L = \infty$	50	57		dB
gm	Transconductance	$I_{comp} = -0.1$ to $0.1mA$ $V_{comp} = 6V$		2.5		ms
<b>Oscillator Section</b>						
	Ramp Valley		0.78	0.85	0.92	V
	Ramp peak	$V_{CC} = 8V$	2	2.15	2.3	V
		$V_{CC} = 55V$	9	9.6	10.2	V
	Maximum duty cycle		95	97		%
	Maximum Frequency	Duty Cycle = 0% $R_{osc} = 13k\Omega$ , $C_{osc} = 820pF$			300	kHz

Typical Performance (Using Evaluation Board) fsw = 100kHz

Output Voltage	Output Ripple	Efficiency V <sub>CC</sub> =35V I <sub>O</sub> = 1.5A	Line Regulation I <sub>O</sub> = 1.5A V <sub>CC</sub> = 8 to 55V	Load Regulation V <sub>CC</sub> =35V I <sub>O</sub> = 0.5 to 1.5A
3.3V	10mV	84 (%)	3mV	6mV
5.1V	10mV	86 (%)	3mV	6mV
12V	12mV	93 (%)	3mV (V <sub>CC</sub> =15 to 55V)	4mV

Figure 1. Test and valuation board circuit.

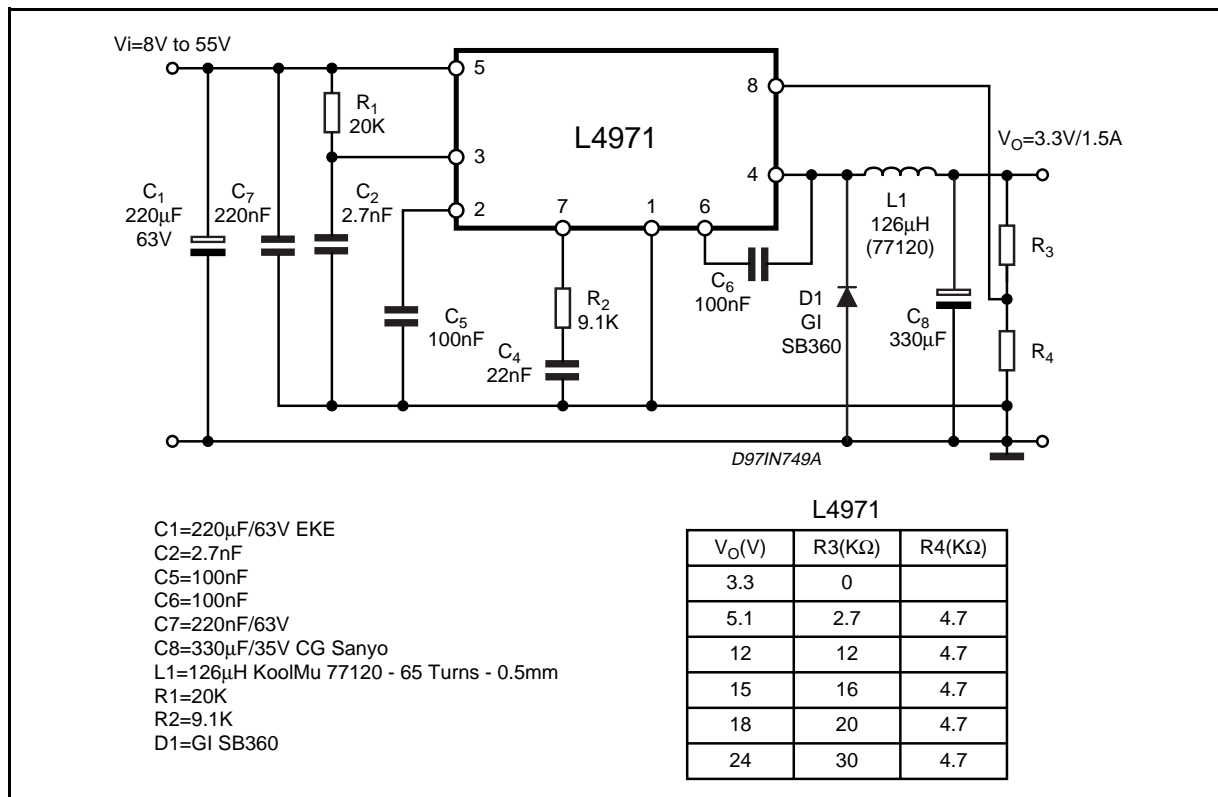


Figure 2. PCB and component layout of the figure 1.

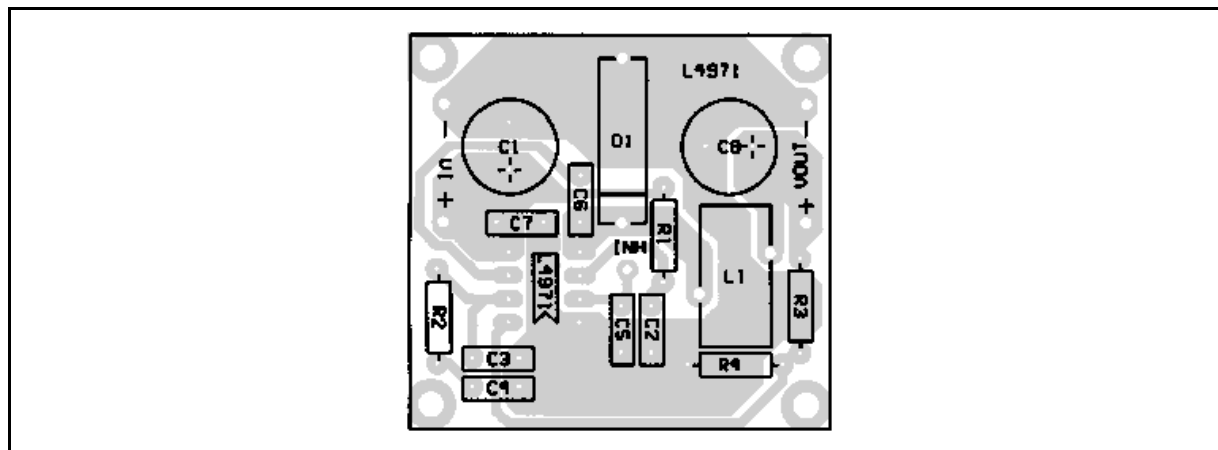


Figure 3. Quiescent drain current vs. input voltage.

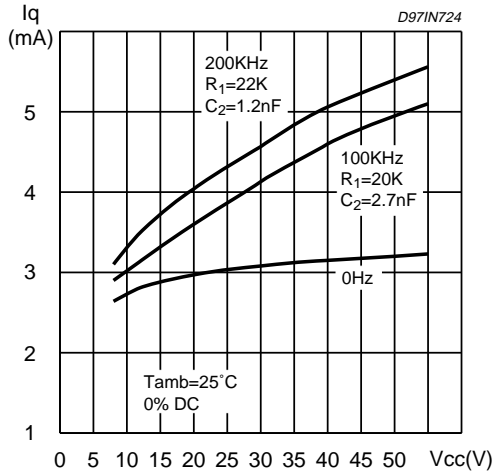


Figure 4. Quiescent current vs. junction temperature

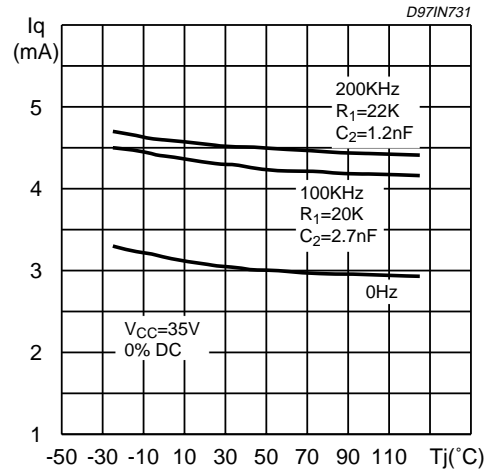


Figure 5. Stand-by drain current vs. input voltage

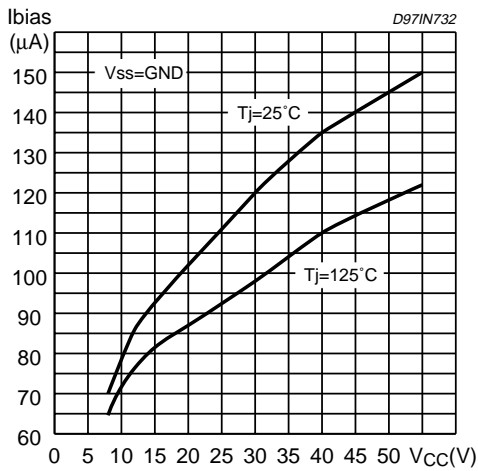


Figure 6. Line Regulation

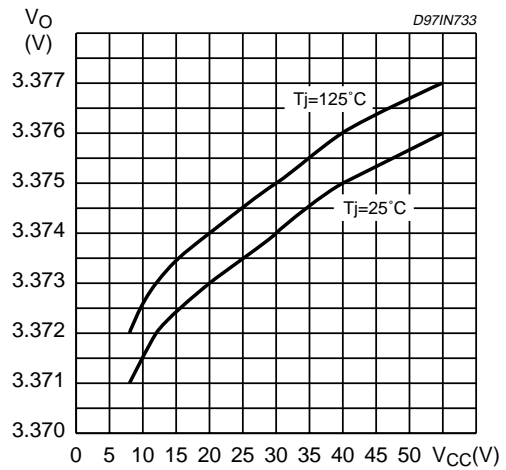


Figure 7. Load regulation

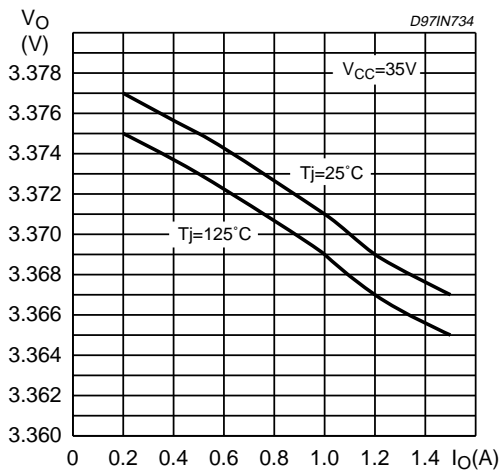


Figure 8. Switching frequency vs. R1 and C2

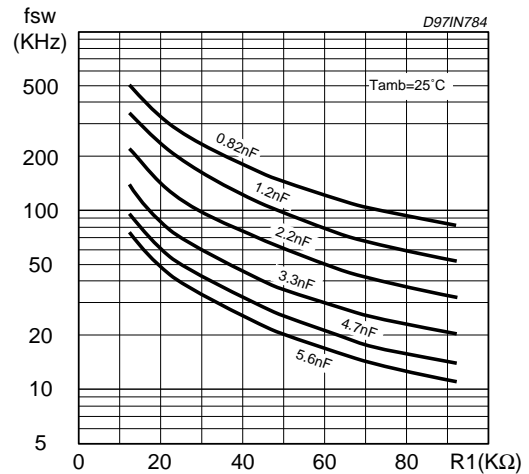


Figure 9. Switching Frequency vs. input voltage.

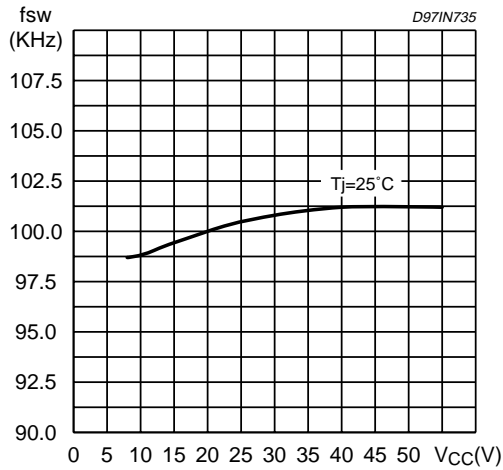


Figure 10. Switching frequency vs. junction temperature.

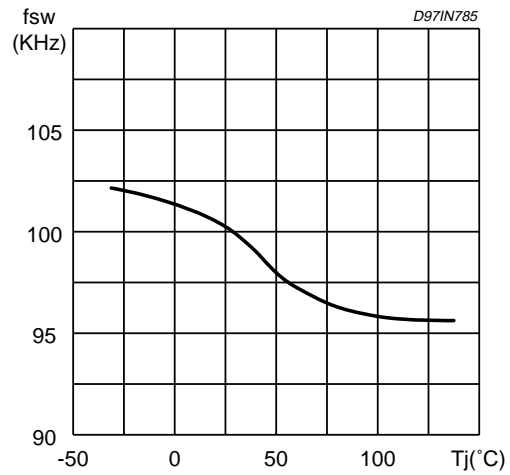


Figure 11. Dropout voltage between pin 5 and 4.

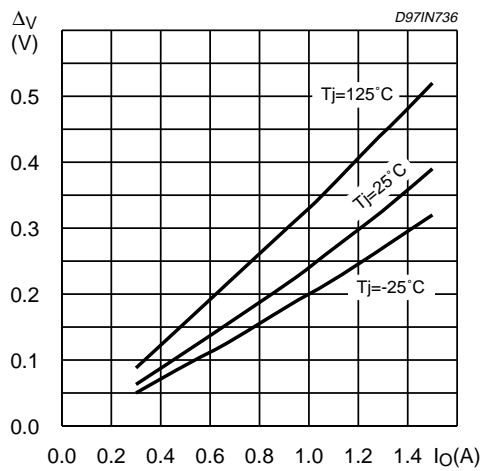


Figure 12. Efficiency vs output voltage.

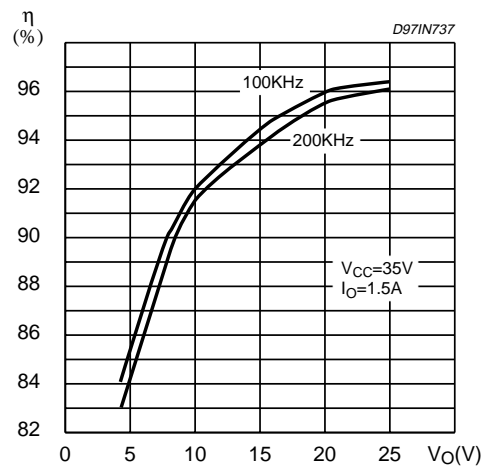


Figure 13. Efficiency vs. output current.

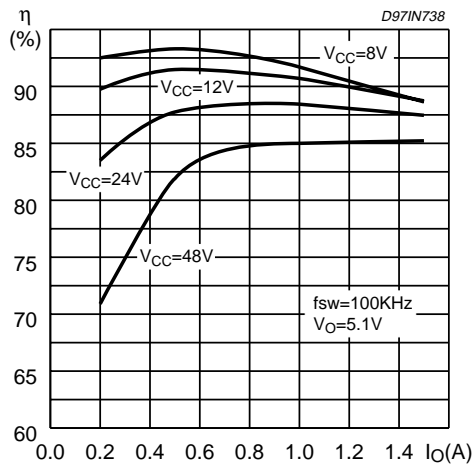


Figure 14. Efficiency vs. output current.

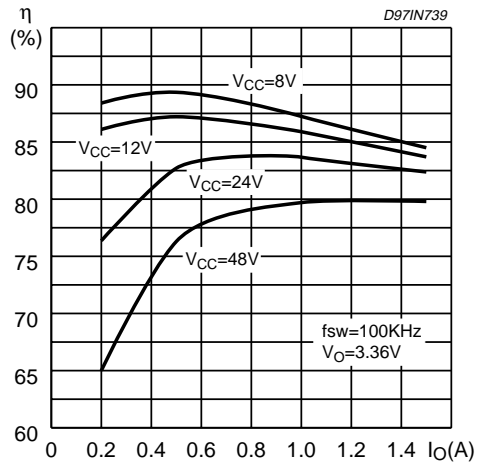


Figure 15. Efficiency vs. output current.

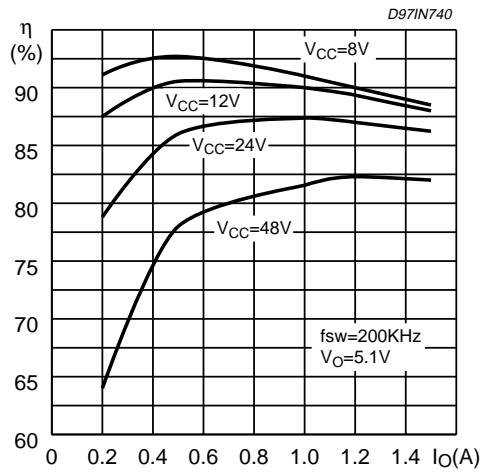


Figure 16. Efficiency vs. output current.

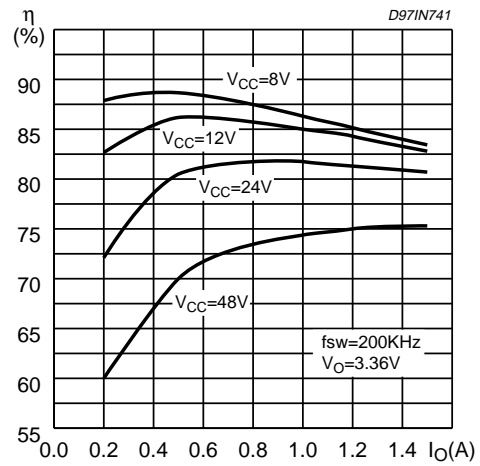


Figure 17. Efficiency vs. Vcc.

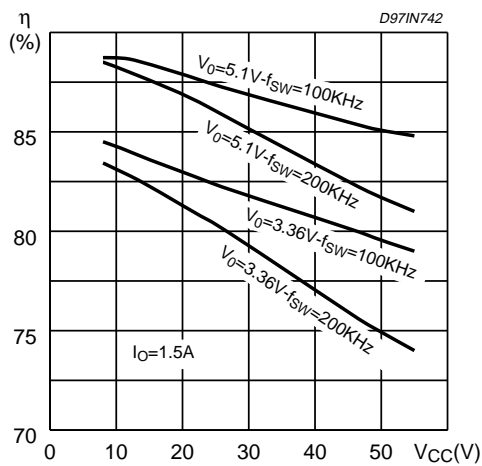


Figure 18. Power dissipation vs. Vcc.

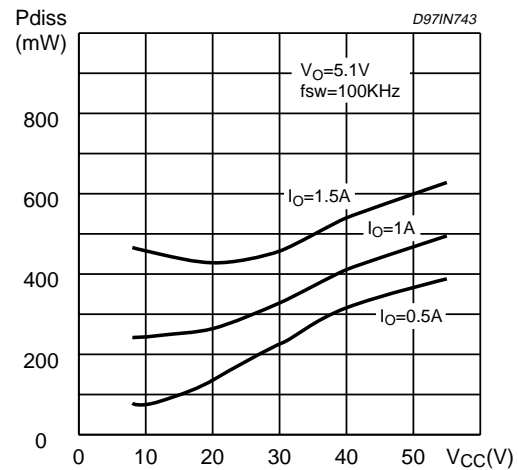


Figure 19. Efficiency vs. V\_o.

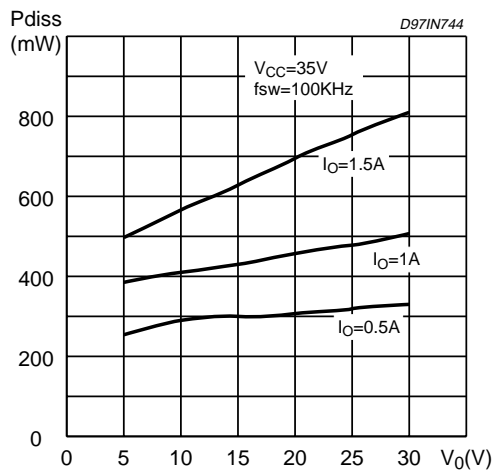


Figure 20. Pulse by pulse limiting current vs. junction temperature.

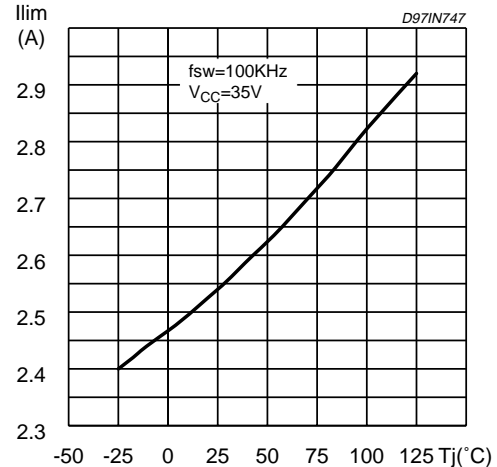




Figure 21. Load transient.

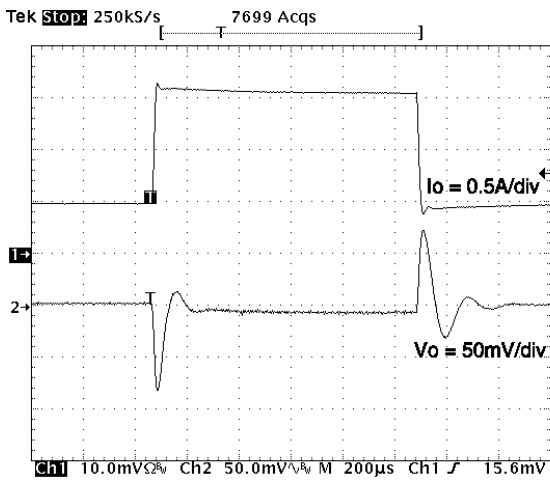


Figure 22. Line transient.

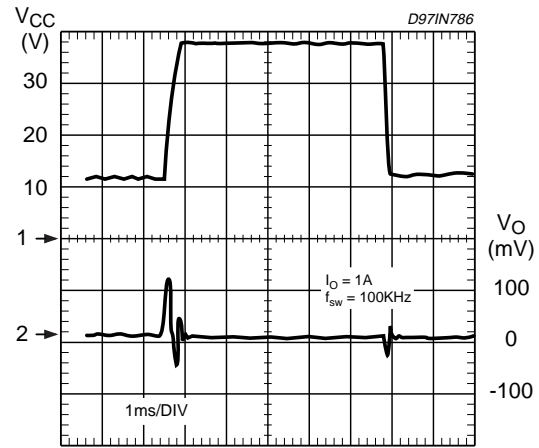


Figure 23. Soft start capacitor selection Vs inductor and Vccmax.

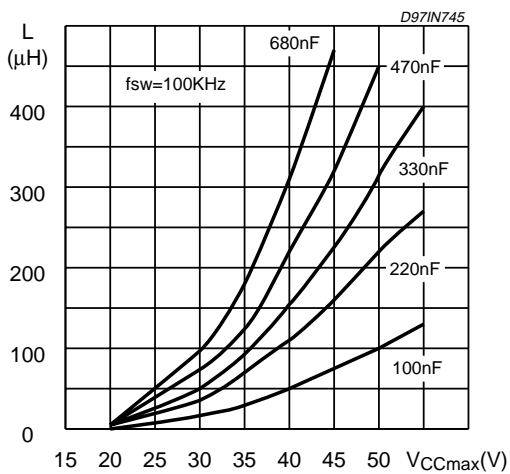


Figure 24. Soft start capacitor selection vs. inductor and Vccmax.

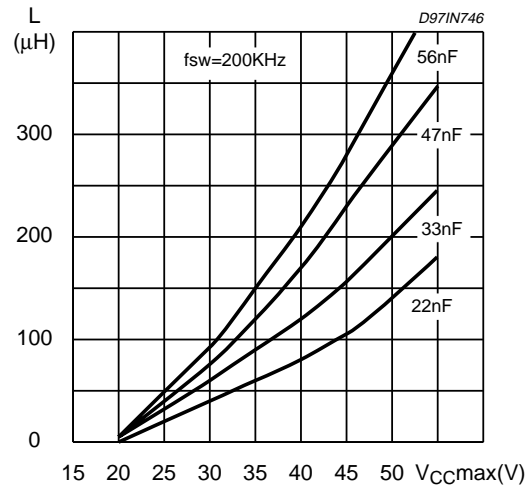
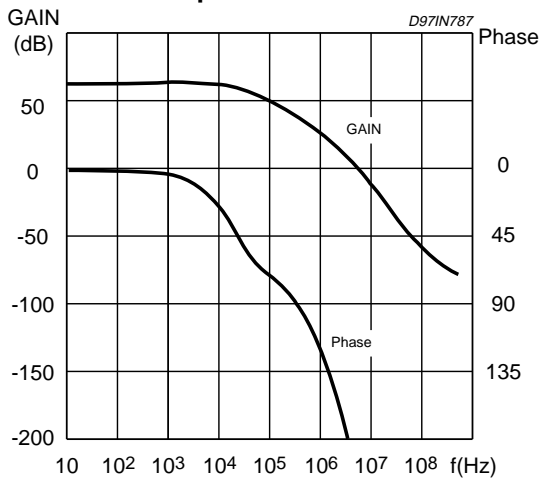
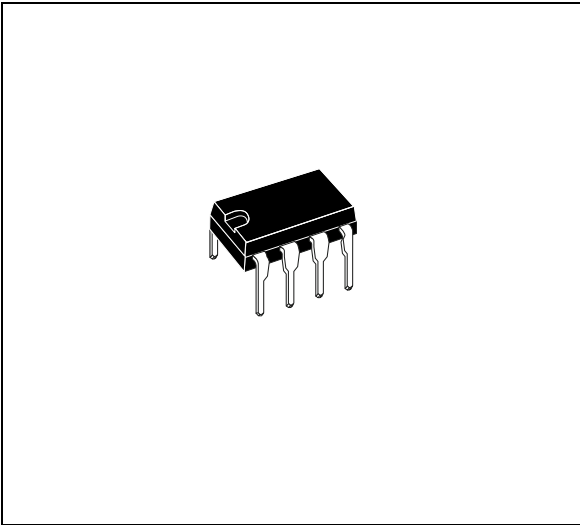


Figure 25. Open loop frequency and phase of error amplifier

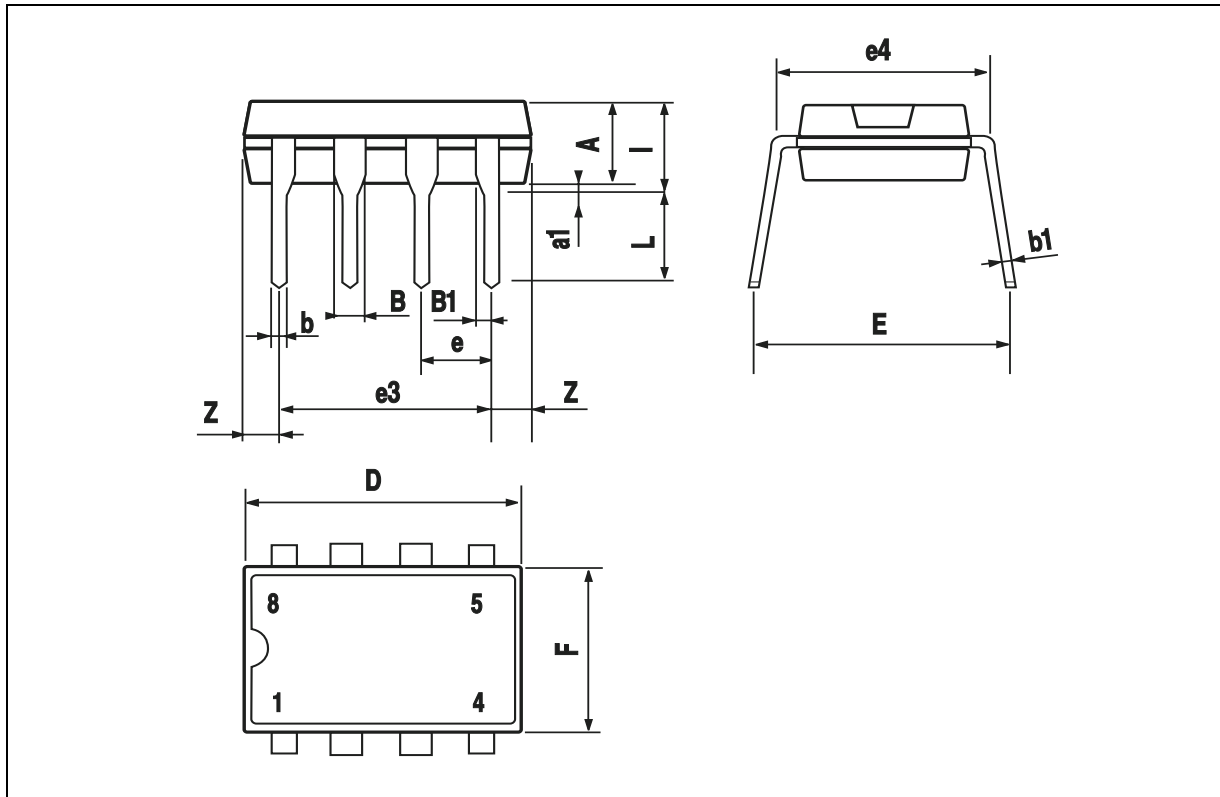


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

**OUTLINE AND MECHANICAL DATA**

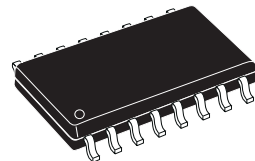


**Minidip**

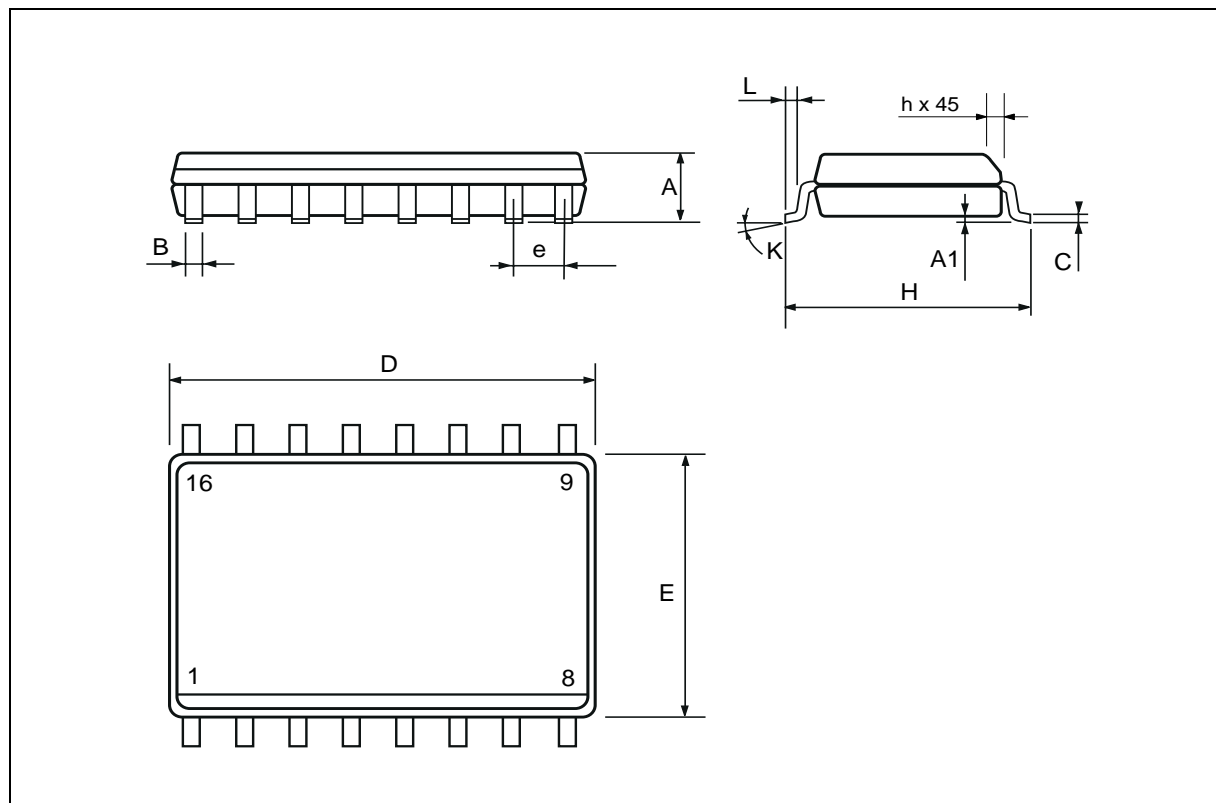


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	10.1		10.5	0.398		0.413
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

## OUTLINE AND MECHANICAL DATA



**SO16 Wide**



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