



## Performance Specifications

Table 1. Electrical Performance					
Parameter	Symbol	Min	Typical	Maximum	Units
Frequency <sup>1,2,3</sup>					
Input Frequency	$F_{IN}$	0.008		400	MHz
Capture Range	APR	±40			ppm
Output Frequency - Primary	$F_{OUT1}$	500		850	MHz
Output Frequency - Secondary	$F_{OUT2}$	125		850	MHz
Supply					
Voltage <sup>2,3</sup>	$V_{CC}$	3.13	3.3	3.46	V
Current (No Load) <sup>3</sup>	$I_{CC}$		140	180	mA
Input Signal					
LVC MOS	$F_{IN}$		LVC MOS		
LVDS <sup>2,3,7</sup>	$F_{IN}$		LVDS		
LVPECL	$F_{IN}$		LVPECL		
Differential Output (Options F and P) <sup>2,3,4,5</sup>					
Common Mode Output Voltage	$V_{OCM}$	$V_{CC}-1.5$	$V_{CC}-1.3$	$V_{CC}-1.1$	V
DC Output High Voltage	$V_{OH}$	$V_{CC}-1.085$	$V_{CC}-0.950$	$V_{CC}-0.880$	V
DC Output Low Voltage	$V_{OL}$	$V_{CC}-1.830$	$V_{CC}-1.7$	$V_{CC}-1.620$	V
Peak to Peak Output Voltage	$V_{P-P}$		700		mV p-p
Rise Time	$t_R$		0.5		ns
Fall Time	$t_F$		0.5		ns
Symmetry	SYM	45	50	55	%
SSB Phase Noise, $F_{out} = 155.52/622.08$ <sup>5,6</sup>					
10Hz Offset	$\Phi_n$		-64/-27		dBc/Hz
100Hz Offset	$\Phi_n$		-95/-55		dBc/Hz
1kHz Offset	$\Phi_n$		-123/-123		dBc/Hz
10kHz Offset	$\Phi_n$		-143/-110		dBc/Hz
100kHz Offset	$\Phi_n$		-146/-130		dBc/Hz
1 MHz Offset	$\Phi_n$		-146/-146		dBc/Hz
10 MHz Offset	$\Phi_n$		-146/-146		dBc/Hz
Jitter Generation <sup>5,6</sup>					
155.52 MHz (12kHz - 20MHz BW)	$\Phi_J$		0.30		ps RMS
622.08 MHz (12kHz - 20 MHz BW)	$\Phi_J$		0.12		ps RMS
Operating Temperature (Options C of F) <sup>1,3</sup>	$T_{OP}$	0 to 70 or -40 to 85			°C

1. See Standard Frequencies and Ordering Information.

2. Parameters are tested with production test circuit below (Fig 2).

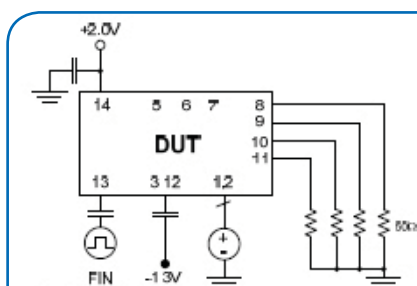
3. Parameters are tested at ambient temperature with test limits guard banded for specified operating temperature.

4. Measured from 20% to 80% of a full output swing (Fig 3).

5. Not tested in production, guaranteed by design, verified at qualification.

6. The FX-402 phase noise and jitter performance can be optimized for specific applications. Please consult with Vectron's Application Engineers for more information.

7. LVC MOS input signal levels are valid for input frequencies < 100 MHz.



Test Circuit Notes:  
 1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.  
 2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.  
 3) 50Ω Terminations are Within Test Equipment.

Figure 2. Test Circuit

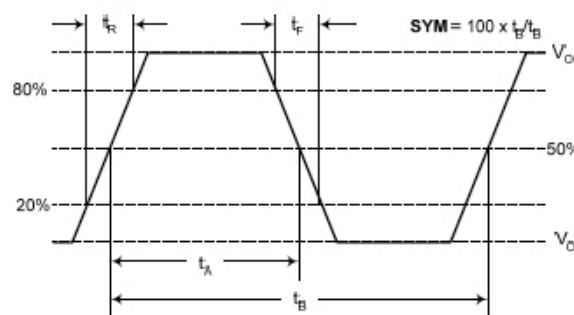


Figure 3. LVPECL Waveform

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

**Table 2. Absolute Maximum Ratings**

Parameter	Symbol	Ratings	Unit
Power Supply	$V_{DD}$	6	V
Storage Temperature	$T_{STR}$	-55 to 125	°C
Soldering Tewmp/Tlme	$T_{LS}$	260/40	°C/sec

## Reliability

The FX-402 is capable of meeting the following qualification tests

**Table 3. Environmental Compliance**

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

## Handling Precautions

Although ESD protection circuitry has been designed into the the FX-402, proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance=1.5Kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes

**Table 4. Predicted ESD R\$atings**

Model	Minimum	Conditions
Human Body Model	500 V	MIL-STD 883, Method 3015
Charged Device Model	500 V	JEDEC, JESD22-C101

**Table 5. Reflow Profile (IPC/JEDEC J-STD-020C)**

Parameter	Symbol	Value
PreHeat Time	$t_s$	60 sec Min, 180 sec Max
Ramp Up	$R_{UP}$	3 °C/sec Max
Time Above 217 °C	$t_L$	60 sec Min, 150 sec Max
Time To Peak Temperature	$t_{AMB-P}$	480 sec Max
Time At 260 °C	$t_p$	20 sec Min, 40 sec Max
Ramp Down	$R_{DN}$	6 °C/sec Max

The FX-402 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-402 should not be subjected to a wash process that will immerse it in solvents. NO CLEAN is the recommended procedure. The FX-402 has been designed for pick and place reflow soldering. The FX-402 may be reflowed once and should not be reflowed in the inverted position.

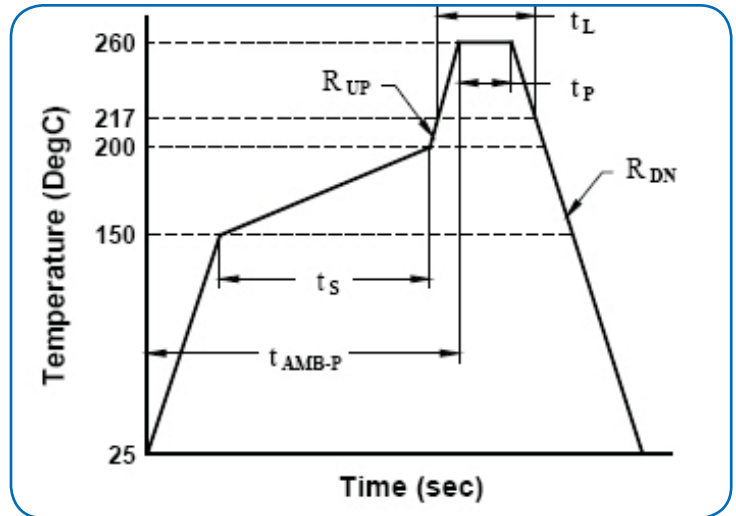


Figure 4. Suggested IR Profile

## Tape and Reel

**Table 6. Tape and Reel Information**

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
32	14.2	1.5	4	20	330	1.5	13	20.2	100	44.4	50.4	200

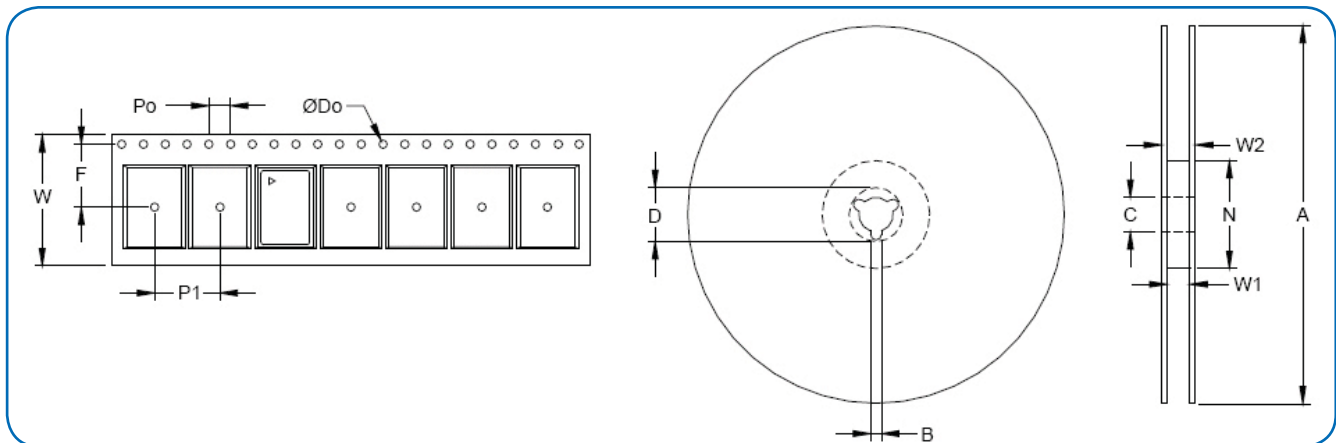


Figure 5. Tape and Reel

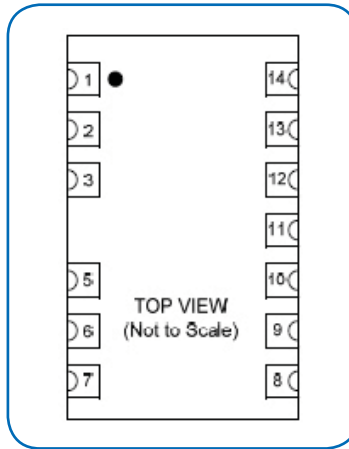


Figure 6. Pin Configuration

**Table 7. Pin Functions**

Pin #	Symbol	I/O	Level	Function
1	SEL0	I	LVC MOS	Frequency Select - see table 3
2	SEL1	I	LVC MOS	Frequency Select - see table 3
3	GND	GND	Supply	Case and Electrical Ground
4				Not present
5	VMON	O		VCXO Control Voltage Monitor Under locked conditions VMON should be > 0.3V and <3.0V. The input frequency may be out of range if the voltage exceeds these levels
6	OD	I	LVC MOS	Output Disable Disabled = Logic "1" Enabled = Logic "0" or no connect
7	LD	O	LVC MOS	Lock Detect Locked = Logic "1" Loss of Lock = Logic "0"
8	FOUT1	O	LCPECL	Frequency Output - Primary
9	CFOUT1	O	LVPECL	Complimentary Frequency Output - Primary
10	FOUT2	O	LVPECL	Divided-Down VCXO/VCXO Output, or Disabled
11	CFOUT2	O	LVPECL	Complimentary Divided-Down VCXO/VCXO Output, or Disabled
12	GND	GND	Supply	Case and Electrical Ground
13	FIN	I	LVC MOS or LVPECL	Input Frequency - AC Coupled
14	VCC	VCC	Supply	Power Supply Voltage (3.3 V ±5%)

LVC MOS input signal levels are valid for input frequencies < 100 MHz.

**Table 8. Control Logic (LVC MOS)**

SEL 0	SEL 1	Clock Input
0	0	FIN <sub>1</sub>
0	1	FIN <sub>2</sub>
1	0	FIN <sub>3</sub>
1	1	FIN <sub>4</sub>

## FX-402 Outline Diagram and Pad Layout

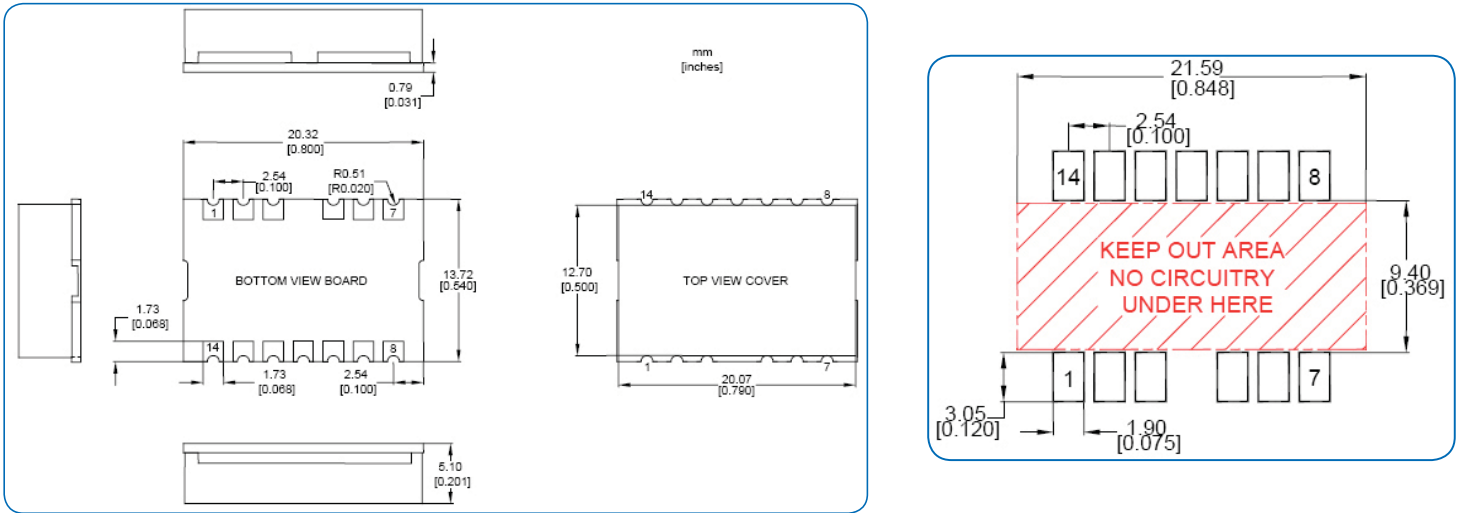
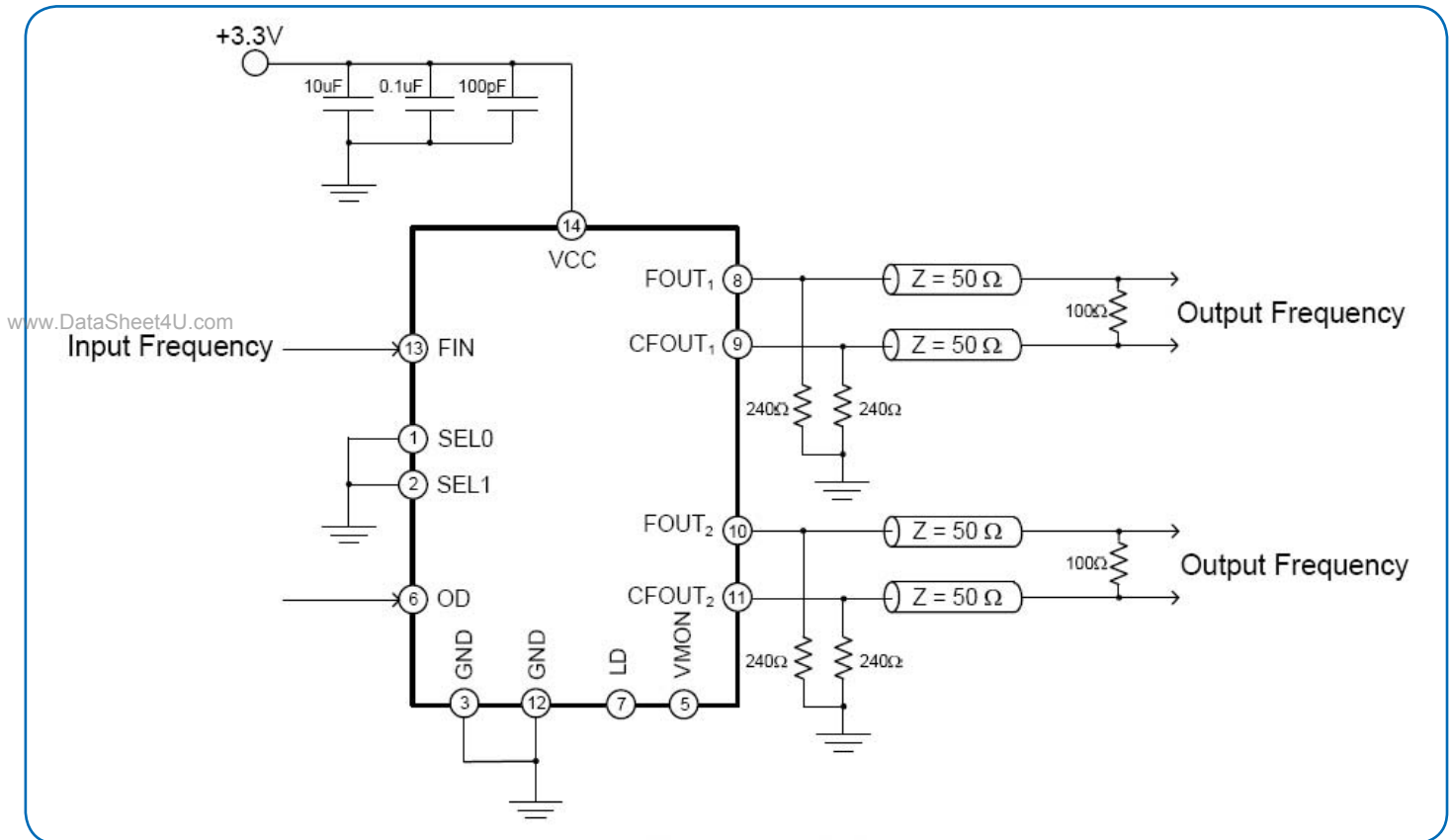


Figure 7. Outline and Pad Layout

## Suggested Output Load Configurations



**LV-PECL to LV-PECL:** For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.

### Table 9. Standard Frequencies

0.00080000	AN	1.92000000	B1	14.8351600	DL	30.7200000	H1	52.0000000	JP	110.000000	L1	300.000000	PT	669.326582	R3
0.00100000	A1	2.00000000	B8	15.0000000	D4	30.8800000	HF	53.3300000	JU	112.000000	L2	307.200000	RX	669.642900	R1
0.00200000	AR	2.04800000	B4	15.0336000	DR	31.2500000	H8	54.7460000	JL	114.000000	L3	311.040000	P1	670.838600	R7
0.00320000	AG	2.30400000	BD	15.3600000	DW	32.0000000	H2	55.0000000	JX	120.000000	LC	312.500000	PU	672.000000	RT
0.00400000	A2	2.45760000	BJ	16.0000000	D9	32.7680000	H3	60.0000000	JR	122.880000	LB	318.750000	PV	672.156250	TX
0.00800000	A3	2.50000000	BM	16.3840000	D5	33.0000000	H7	61.3800000	KY	124.416000	L7	320.000000	PP	672.162712	R5
0.00819200	BY	2.55750000	B9	17.1840000	DE	33.3330000	HC	61.4400000	J5	125.000000	L4	322.265650	PW	673.456600	RA
0.00946900	AU	3.08800000	B6	18.4320000	D7	34.3680000	H6	62.2080000	J8	130.000000	LD	328.710950	PX	684.255400	R9
0.01000000	A6	3.24000000	BL	18.5280000	DC	34.5600000	HB	62.5000000	J9	139.264000	L5	333.257150	PY	687.700000	TV
0.01562500	AL	3.25000000	BC	18.7500000	EE	36.8640000	HG	62.9145000	LE	150.000000	M8	334.663300	RB	690.569196	R4
0.01573400	AD	3.37500000	BH	19.2000000	DD	37.0560000	H4	63.3600000	JJ	150.144000	M6	336.081350	RC	693.468750	RV
0.01575000	AC	3.84000000	B7	19.3926580	DX	37.1250000	H9	63.8976000	JN	153.600000	MA	353.676350	RD	693.482991	R6
0.01600000	A4	4.00000000	BN	19.4400000	D6	37.5000000	HK	64.0000000	JT	155.520000	M2	368.640000	RY	693.750000	R8
0.02400000	BX	4.09600000	B5	19.5312500	DZ	38.8800000	H5	64.1520000	JH	156.250000	M3	375.000000	RF	696.390625	RW
0.02500000	BR	4.19430400	CJ	19.6608000	DB	39.0625000	HH	65.5360000	J6	159.375000	M7	382.800000	RU	696.421478	V1
0.03200000	BW	5.00000000	C6	19.6989680	DK	39.3216000	HD	66.0000000	JA	160.000000	M1	400.000000	RR	696.421875	TY
0.04000000	AP	5.12000000	CD	19.7190000	DH	39.8437500	HJ	70.0000000	KB	161.132813	M4	409.600000	RE	704.380600	TG
0.04410000	AA	6.14400000	CG	19.9218750	ED	40.0000000	JF	70.6560000	KC	164.355475	M9	491.520000	PM	707.352700	TC
0.04800000	AB	6.29140000	CC	20.0000000	E2	40.2830630	KK	71.6100000	KF	166.628572	M5	500.000000	RK	707.500000	V2
0.04807700	AV	6.29145600	CF	20.1416000	E3	40.9600000	J1	73.7280000	K8	167.331646	N2	505.000000	V3	710.948600	T2
0.05000000	BT	6.31200000	C7	20.4800000	E4	41.0888870	KM	74.1250000	K1	168.040678	N3	531.000000	PH	712.520000	TW
0.06400000	A5	6.48000000	C2	20.5444340	EF	41.6571440	KP	74.1758000	KA	170.000000	N4	531.250000	P8	716.573200	T1
0.08000000	A9	6.75000000	CB	20.7135000	E1	41.6600000	LM	74.2500000	K7	172.500000	NU	568.928600	PJ	718.750000	T5
0.10000000	AH	7.68000000	C9	20.8285720	EG	41.8329130	KT	75.0000000	KH	173.370748	ND	569.196400	P9	719.734400	T3
0.12800000	AX	7.77600000	C5	20.8286000	EB	42.0000000	JB	76.8000000	K4	173.437500	NP	588.000000	RH	737.280000	TL
0.24300000	A8	8.19200000	C3	20.9165460	EH	42.0101690	KV	77.7600000	K2	176.838175	NA	595.056000	PL	739.200000	TT
0.25600000	AM	9.21600000	CH	21.0050840	EJ	42.5000000	JC	78.0000000	LH	182.016000	N8	600.000000	PR	742.500000	V4
0.32000000	AW	9.72000000	C8	22.0000000	E9	42.6600000	JZ	78.1250000	K3	182.857142	NM	614.400000	RG	748.070900	T6
0.38400000	AY	9.75000000	CE	22.1047720	EK	44.2095440	KX	78.6432000	K5	184.000000	NG	622.080000	P2	750.000000	T7
0.40000000	AF	9.83040000	C1	22.2171000	E5	44.4343000	LF	79.6875000	KG	184.320000	NH	624.693800	PD	768.000000	TN
0.48000000	AK	10.0000000	C4	22.5792000	E8	44.6218000	JW	80.0000000	K9	187.500000	N5	624.704800	P6	777.600000	T4
0.50000000	BP	10.2300000	DP	24.0000000	EC	44.7360000	J3	80.5664130	KJ	195.000000	N7	625.000000	P3	779.568600	T8
0.51200000	AJ	10.2400000	DM	24.5760000	E6	44.9280000	JE	82.1777380	KL	200.000000	NE	627.329600	P7	780.881000	TD
0.65545000	AE	10.4142850	DV	24.7040000	E7	45.1584000	JG	82.9440000	K6	200.192000	N6	629.987800	PA	781.250000	T9
0.77200000	AT	10.4582260	DU	25.0000000	F7	45.8240000	JM	83.3142880	KN	201.416020	N1	637.500000	PG	796.875000	TB
0.96000000	A7	10.4872000	DN	25.1658000	F8	46.0379460	LG	83.6658250	KR	212.500000	NF	640.000000	PN	800.000000	TK
1.00000000	BB	10.9490000	DG	25.6000000	F6	46.7200000	JK	84.0203380	KU	219.429571	NL	644.531250	P4	805.664100	TA
1.02400000	B2	10.9500000	DJ	25.9200000	F2	46.8750000	JY	86.6853740	LJ	240.000000	NR	645.120000	RJ	809.063500	TE
1.21500000	BU	11.1840000	DF	26.0000000	F3	48.0000000	JV	88.4190880	KW	243.000000	NC	647.239400	PE	819.200000	TH
1.22880000	BK	12.2880000	D8	27.0000000	F4	49.1520000	J7	95.7000000	LK	245.760000	N9	647.250800	PK	821.777300	TF
1.25000000	BG	12.3076860	DY	27.6480000	FB	49.4080000	J2	97.5000000	KE	250.000000	NT	649.970300	PF	850.000000	TJ
1.33330000	BF	12.3520000	D1	28.7040000	F1	50.0000000	JD	100.000000	L8	252.571428	NJ	657.421875	PB	983.400000	TU
1.50000000	BE	12.8000000	D2	29.4912000	F5	50.0480000	KD	105.000000	L6	256.000000	NK	665.625600	PC	1,000.0000	TM
1.53600000	BV	13.0000000	D3	29.5000000	F9	51.2000000	LL	106.250000	L9	262.144000	NB	666.514286	P5		
1.54400000	B3	13.5000000	DT	30.0000000	HE	51.8400000	J4	108.000000	LA	292.571429	NN	669.128100	R2		



# FX-402-ECE-KANN-XX-XX

**Product Family**

FX: Frequency Translator

**Package**

402: 20.3 13.0 5.1mm

**Input**

E: 3.3 Vdc ±10%

**Output**

C: LVPECL  
D: LVDS

**Operating Temperature**

E: -40 to 85 °C  
T: 0 to 70 °C

**Absolute Pull Range**

K: ± 50 ppm  
S: ± 100 ppm

**Output Frequency**  
(See Above)

**Input Frequency**  
(See Above)

**Factory Use**

**Factory Use**

**Output 2 Divider**  
A: Divide by 1  
B: Divide by 2  
C: Divide by 4  
K: Disabled

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