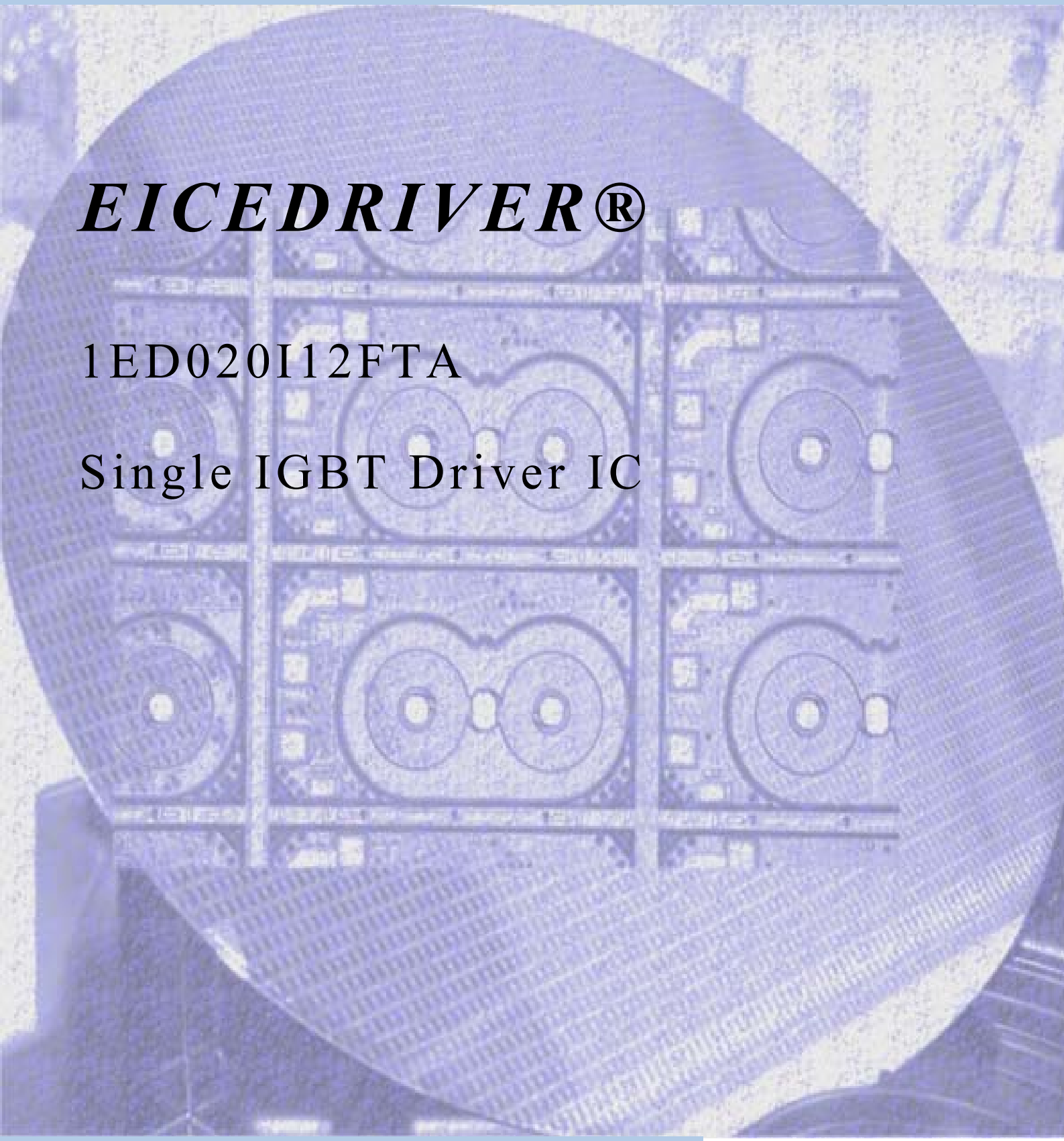

EICEDRIVER®

1ED020I12FTA

Single IGBT Driver IC

Power Management & Drives

Never stop thinking.

1ED020I12FTA

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Previous Version:	0	
Page	Subjects (major changes since last revision)	
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Single IGBT Driver IC

Product Highlights

- **Coreless transformer isolated driver**
- **Galvanic Insulation**
- **Integrated protection features**
- **Suitable for operation at high ambient temperature**
- **Automotive Qualified (pending)**
- **Two level turn off**

Features

- Single channel isolated IGBT Driver
- For 600V/1200V IGBTs
- 2A rail-to-rail output
- Vcesat-detection
- Active Miller Clamp

Typical Application

- Drive inverters for HEV and EV
- Auxilliary inverters for HEV and EV
- Inverters for electrical drives in CAV
- High Power DC/DC inverters

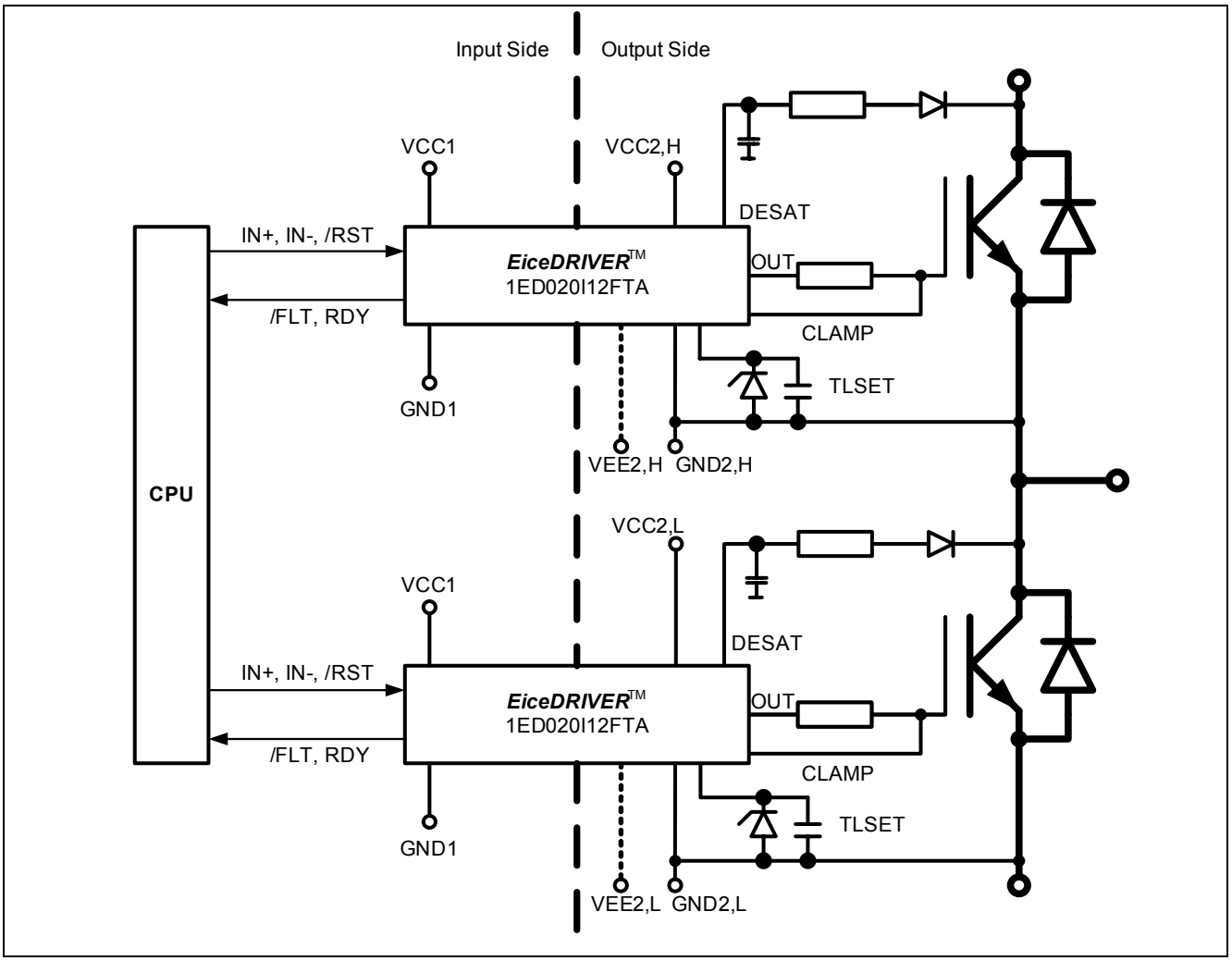

Figure 1: Typical Application

Type		Gate drive current	Package
1ED020I12FTA		+/- 2A	PG-DSO-20-55

1 Block Diagram and Application

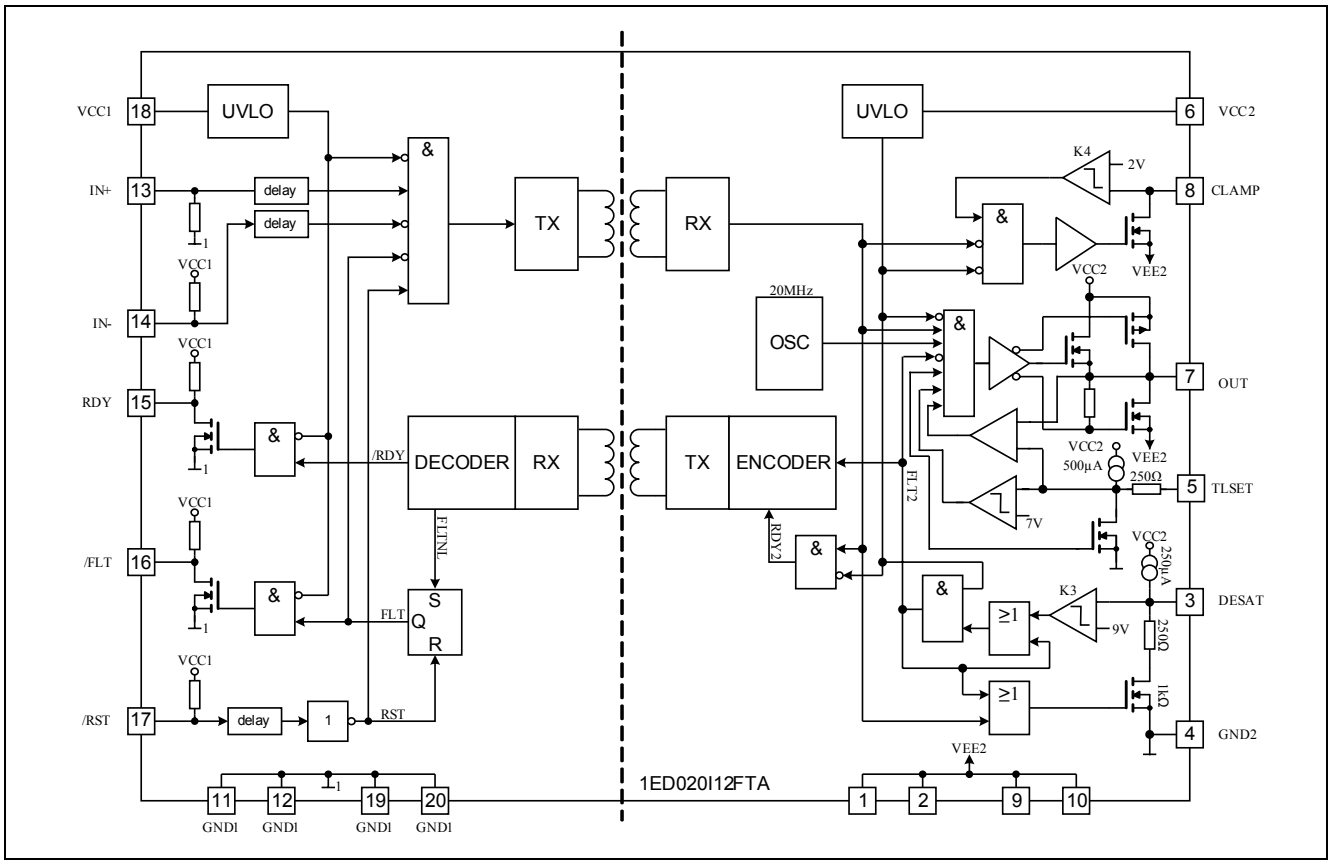

Figure 1: Block Diagram 1ED020I12FTA

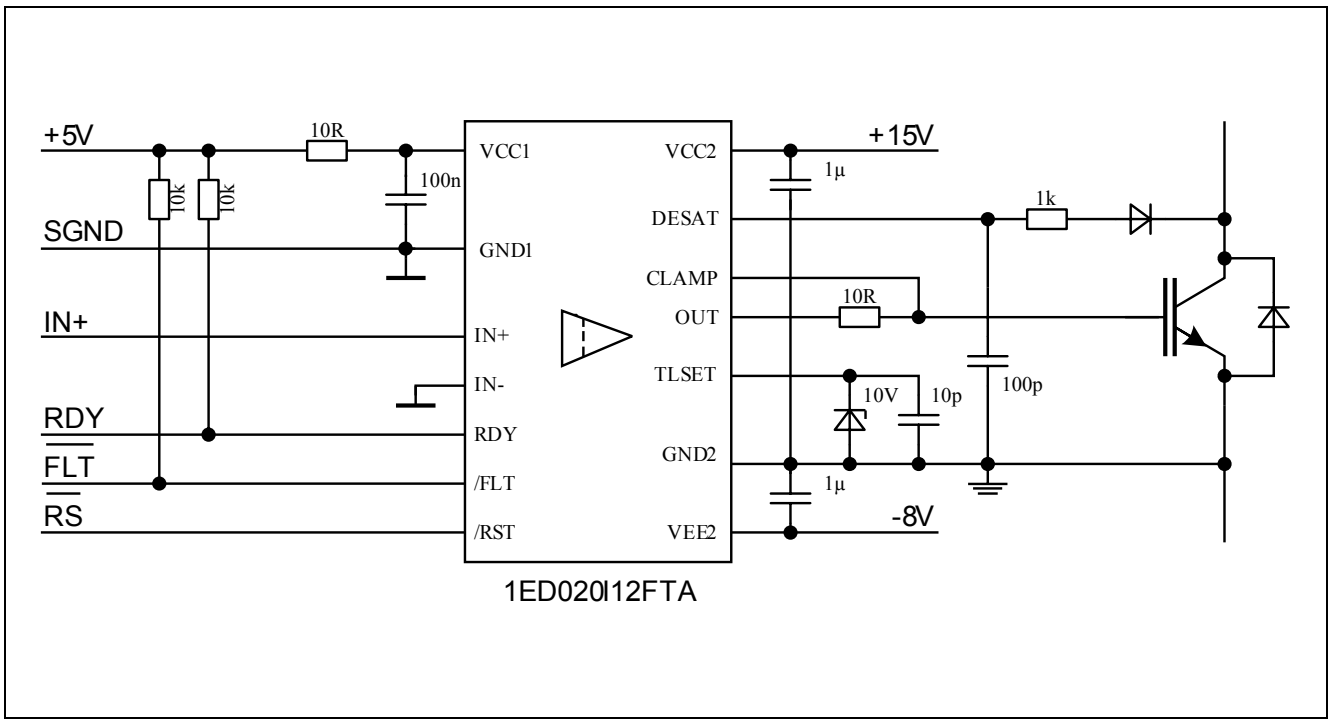

Figure 2: Application Example

2 Functional Description

2.1 Introduction

The 1ED020I12FTA is an advanced IGBT gate driver for motor drives typical greater 10kW. Control and protection functions are included to make possible the design of high reliability systems.

The device consists of two galvanic separated parts. The input chip can be directly connected to a standard 5V DSP or microcontroller with CMOS in/output and the output chip is connected to the high voltage side.

An effective active Miller clamp function avoids the need of negative gate driving in some applications and allows the use of a simple bootstrap supply for the high side driver.

A rail-to-rail driver output enables the user to provide easy clamping of the IGBTs gate voltage during short circuit of the IGBT. So an increase of short circuit current due to the feedback via the Miller capacitance can be avoided. Further, a rail-to-rail output reduces power dissipation.

The device also includes an IGBT desaturation protection with a FAULT status output.

A two-level turn-off feature with adjustable delay protects against excessive overvoltage at turn-off in case of overcurrent or short circuit condition. The same delay is applied at turn-on to prevent pulse width distortion.

A READY status output reports if the device is supplied and operates correctly.

2.2 Internal Protection Features

2.2.1 Undervoltage Lockout (UVLO)

To ensure correct switching of IGBTs the device is equipped with an undervoltage lockout for both chips.

If the power supply voltage V_{VCC1} of the input chip drops below V_{UVLOL1} a turn-off signal is sent to the output chip before power-down. The IGBT is switched off and the signals at IN+ and IN- are ignored as long as V_{VCC1} reaches the power-up voltage V_{UVLOH1} .

If the power supply voltage V_{VCC2} of the output chip goes down below V_{UVLOL2} the IGBT is switched off and signals from the input chip are ignored as long as V_{VCC2} reaches the power-up voltage V_{UVLOH2} .

2.2.2 READY status output

The READY output at pin /RDY shows the status of three internal protection features.

- UVLO of the input chip
- UVLO of the output chip after a short delay
- Internal signal transmission

It is not necessary to reset the READY signal since its state only depends on the status of the former mentioned protection signals.

2.2.3 Watchdog Timer

The 1ED020I12FA incorporates two levels of protection to ensure signal integrity by two independent watchdog timers. First level ensures the short term signal integrity by resending the (turn on/off) signals with a watchdog period of typical 500ns. The second level monitors the internal signal transmission during normal operation. If the transmission fails for a given time, the IGBT is switched off and the READY output reports an internal error.

2.2.4 Active Shut-Down

The Active Shut-Down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply.

2.3 Non-Inverting and Inverting Inputs

There are two possible input modes to control the IGBT. At non-inverting mode IN+ controls the driver output while IN- is set to low. At inverting mode IN- controls the driver output while IN+ is set to high. A minimum input pulse width is defined to filter occasional glitches.

2.4 Driver Output

The output driver section uses only MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage during on-state and short circuit can be maintained as long as the drivers supply is stable. Due to the low internal voltage drop, switching behaviour of the IGBT is predominantly governed by the gate resistor. Furthermore, it reduces the power to be dissipated by the driver.

2.5 Two-Level Turn-Off

The Two-Level Turn-OFF introduces a second turn off voltage level at the driver output in between ON- and OFF-level. This additional level ensures lower V_{CE} overshoots at turn off by reducing gate emitter voltage of the IGBT at short circuits or over current events. The V_{GE} level is adjusting the current of the IGBT at the end two level turn off interval, therequired timing is depending on stray inductance and over current at beginning of two level turn off interval.

Reference voltage level and hold up time could be adjusted at TLSET pin. The reference voltage is set by the required Zener diode connected between pin TLSET and GND2. The hold up time is set by the capacitor connected to the same pin TLSET and GND2.

The hold time can be adjusted during switch on using the whole capacitance connected at pin TLSET including capacitor, parasitic wiring capacitance and junction capacitance of Zener diode. When a switch on signal is given the IC starts to discharge C_{TLSET}. Discharging C_{TLSET} is stopped after 500nsec. Then Ctlset is charged with an internal charge current Itlset. When the voltage of the capacitor Ctlset exceeds 7V a second current source starts charging Ctlset up to V_{ZDIODE}. At the end of this discharge-charge cycle the gate driver is switched on.

The time between IN initiated switch-on signal (minus an internal propagation delay of approximately 200ns) and switch-on of the gate drive is sampled and stored digitally. It represents the two level turn off set time T_{TLSET} during switch-off. Due to digitalization the tpdon time can vary in time steps of 50nsec.

If switch off is initiated from IN+, IN- or /RST signal, the gate driver is switched off immediately after internal propagation delay of approximately 200ns and V_{OUT} begins to decrease. For switch off initiated by DESAT, the gate driver switch off is delayed by desaturation sense to OUT delay. The output voltage V_{OUT} is sensed and compared with the Zener voltage V_{ZDIODE}. When V_{OUT} falls below the reference voltage V_{ZDIODE} of the Zener diode the switch off process is interrupted and Vout is adjusted to V_{ZDIODE}. OUT is switched to VEE2 after the hold up time has passed.

The Two-Level Turn-OFF function can not be disabled.

2.6 Minimal On Time / Off Time

The 1ED020I12FTA driver requires minimal on and off time for propper operation in the application. Minimal on time must be greater than the adjustable two level plateau time T_{TLSET}, shorter on times will be surpressed by generating of the plateau time. Due to the short on time, the voltage at TLSET pin does not reach the comparator threshold, therefore the driver do not turn on. A similar principle takes place for off time. Minimal off time must be greater than T_{TLSET}, shorter off times will be surpressed, which means OUT stays on. A two level turn off plateau can not be shortened by the driver. If the driver has entered the turn off sequence it can not switch off due to the fact, that the driver has already entered the shut off mode. But if the driver input signal is turned on again, it will leave the lower level after T_{TLSET} time by switching OUT to high.

2.7 External Protection Features

2.7.1 Desaturation Protection

A desaturation protection ensures the protection of the IGBT at short circuit. When the DESAT voltage goes up and reaches 9V, the output is driven low. Further, the FAULT output is activated. A programmable blanking time is used to allow enough time for IGBT saturation. Blanking time is provided by a highly precise internal current source and an external capacitor.

2.7.2 Active Miller Clamping

A Miller clamp allows sinking the Miller current during a high dV/dt situation. Therefore, the use of a negative supply voltage can be avoided in many applications. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2V (related to VEE2). The clamp is designed for a Miller current up to 2A.

2.7.3 Short Circuit Clamping

During short circuit the IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to OUT and CLAMP limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10us may be fed back to the supply through one of this paths. If higher currents are expected or a tighter clamping is desired external Schottky diodes may be added.

2.8 RESET

The reset input has two functions.

Firstly, /RST is in charge of setting back the FAULT output. If /RST is low longer than a given time , /FLT will be reseted at the rising edge of /RST; otherwise, it will remain unchanged. Moreover, it works as enable/shutdown of the input logic.

3 Pin Configuration and Functionality

3.1 Pin Configuration

Pin	Symbol	Function
1	VEE2	Negative power supply output side
2	VEE2	Negative power supply output side
3	DESAT	Desaturation protection
4	GND2	Signal ground output side
5	TLSET	Two level set
6	VCC2	Positive power supply output side
7	OUT	Driver output
8	CLAMP	Miller clamping
9	VEE2	Negative power supply output side
10	VEE2	Negative power supply output side
11	GND1	Signal ground input side
12	GND1	Signal ground input side
13	IN+	Non inverted driver input
14	IN-	Inverted driver input
15	RDY	Ready output
16	$\overline{\text{FLT}}$	Fault output, low active
17	$\overline{\text{RST}}$	Reset input, low active
18	VCC1	Positive power supply input side
19	GND1	Signal ground input side
20	GND1	Signal ground input side

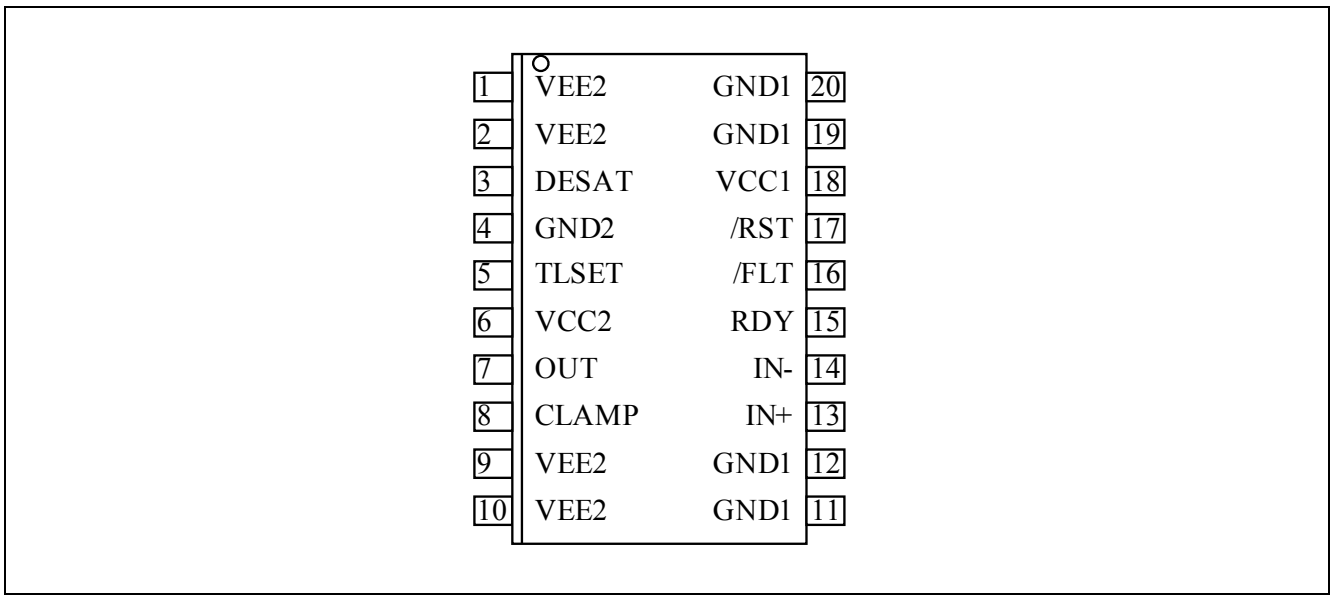

Figure 3: Pin Configuration PG-DSO-20-55 (top view)

3.2 Pin Functionality

GND1

Ground connection of the input side.

IN+ Non-inverting driver input

IN+ control signal for the driver output if IN- is set to low. (The IGBT is on if IN+ = high and IN- = low)

A minimum pulse width is defined to make the IC robust against glitches at IN+. An internal Pull-Down-Resistor ensures IGBT Off-State.

IN- Inverting driver input

IN- control signal for driver output if IN+ is set to high. (IGBT is on if IN- = low and IN+ = high)

A minimum pulse width is defined to make the IC robust against glitches at IN-. An internal Pull-Up-Resistor ensures IGBT Off-State.

/RST (Reset) input

Function 1: Enable/shutdown of the input chip. (The IGBT is off if /RST = low). A minimum pulse width is defined to make the IC robust against glitches at IN-.

Function 2: Resets the DESAT-FAULT-state of the chip if /RST is low for a time T_{RST}. An internal Pull-Up-Resistor is used to ensure FLT status output.

/FLT (Fault output)

Open-drain output to report a desaturation error of the IGBT (FLT is low if desaturation occurs)

RDY (Ready status)

Open-drain output to report the correct operation of the device. (RDY = high if both chips are above the UVLO level and the internal chip transmission is faultless)

VCC1

5V power supply of the input chip

VEE2

Negative power supply pins of the output chip. If no negative supply voltage is available, all VEE2 pins have to be connected to GND2.

DESAT (Desaturation)

Monitoring of the IGBT saturation voltage (V_{CE}) to detect desaturation caused by short circuits. If OUT is high, V_{CE} is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an external capacitor.

CLAMP (Clamping)

Ties the gate voltage to ground after the IGBT has been switched off at a defined voltage to avoid a parasitic switch-on of the IGBT.During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2V (related to VEE2).

GND2

Reference ground of the output chip.

OUT (Driver output)

Output pin to drive an IGBT. The voltage is switched between VEE2 and VCC2. In normal operating mode Vout is controlled by IN+, IN- and /RST. During error mode (UVLO, internal error or DESAT) Vout is set to VEE2 independent of the input control signals.

VCC2

Positive power supply pin of the output side.

TLSET (Two-Level turn-off)

Setting up the timing (with ext. capacitor) and voltage reference (with ext. Zener diode) for the two-level turn-off, see figure 5.

4 Electrical Parameters

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Positive power supply output side	V_{VCC2}	-0.3	20	V	1)
Negative power supply output side	V_{VEE2}	-12	0.3	V	1)
Maximum power supply voltage output side (V_{VCC2}-V_{VEE2})	V_{max2}	—	28	V	
Gate driver output	V_{OUT}	V_{VEE2}-0.3	V_{max2}+0.3	V	
Gate driver high output maximum current	I_{OUT}		2.4	A	t = 2µs
Gate driver low output maximum current	I_{OUT}		2.4	A	t = 2µs
Maximum short circuit clamping time	t_{CLP}	—	10	us	$I_{CLAMP/OUT}$ = 500mA
Positive power supply input side	V_{VCC1}	-0.3	6.5	V	
Logic input voltages (IN+,IN-,$\overline{RST}$)	$V_{LogicIN}$	-0.3	6.5	V	
Opendrain Logic output voltage ($\overline{FLT}$)	$V_{\overline{FLT}}$	-0.3	6.5	V	
Opendrain Logic output voltage (RDY)	V_{RDY}	-0.3	6.5	V	
Opendrain Logic output current ($\overline{FAULT}$)	$I_{\overline{FLT}}$	—	10	mA	
Opendrain Logic output current (RDY)	I_{RDY}	—	10	mA	
Pin DESAT voltage	V_{DESAT}	-0.3	V_{VCC2} +0.3		1) V_{VEE2} = -8V
Pin TLSET voltage	V_{TLSET}	-0.3	V_{VCC2} +0.3		1) V_{VEE2} = -8V
Pin CLAMP voltage	V_{CLAMP}	V_{VEE2}-0.3	V_{VCC2}+0.3 2)		
Junction temperature	T_J	-40	150	°C	
Storage temperature	T_S	-55	150	°C	
Power dissipation, Input chip	$P_{D, IN}$	—	100	mW	3)@TA = 25°
Power dissipation, Output chip	$P_{D, OUT}$	—	700	mW	2)3)@TA = 25°
Thermal resistance (Input chip active)	$R_{THJA,IN}$	—	139	K/W	2)@TA = 25°C
Thermal resistance (Output chip active)	$R_{THJA,OUT}$	—	117	K/W	2)@TA = 25°C
ESD Capability	V_{ESD}	—	1.5	kV	Human Body Model4)

1) With respect to GND2.

2) may be exceeded during short circuit clamping

3) Output IC power dissipation is derated linearly at 8.5 mW/°C above 68°C. Input IC power dissipation does not require derating. See section 8.1 for reference layouts for these thermal data. Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

4) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor).

4.2 Operating Parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Positive power supply output side	V_{VCC2}	13	20	V	1)
Negative power supply output side	V_{VEE2}	-12	0	V	1)
Maximum power supply voltage output side (V_{VCC2}-V_{VEE2})	V_{max2}	—	28	V	
Positive power supply input side	V_{VCC1}	4.5	5.5	V	
Logic input voltages (IN+,IN-,$\overline{RST}$)	$V_{LogicIN}$	-0.3	5.5	V	
Pin CLAMP voltage	V_{CLAMP}	V_{VEE2}-0.3	V_{VCC2} 2)	V	
Pin DESAT voltage	V_{DESAT}	-0.3	V_{VCC2}	V	1)
Pin TLSETvoltage	V_{TLSET}	-0.3	V_{VCC2}	V	1)
Ambient temperature	T_A	-40	125	°C	
Common mode transient immunity3)	$\|\Delta V_{ISO}/dt\|$	—	50	kV/µs	@ 500V

1) With respect to GND2.

2) May be exceeded during short circuit clamping

3) The parameter is not subject to production test - verified by design/characterization

4.3 Recommended Operating Parameters

Note: Unless otherwise noted all parameters refer to GND1.

Parameter	Symbol	Values	Unit	Remarks
Positive power supply output side	V_{VCC2}	15	V	1)
Negative power supply output side	V_{VEE2}	-8	V	1)
Positive power supply input side	V_{VCC1}	5	V	

1) With respect to GND2.

4.4 Electrical Characteristics

Note: The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 11 to 20, GND2 for pins 1 to 10).

4.4.1 Voltage Supply.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
UVLO Threshold Input Chip	V_{UVLOH1}	—	4.1	4.3	V	
	V_{UVLOL1}	3.5	3.8	—	V	
UVLO Hysteresis Input Chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS1}	0.15	—	—	V	
UVLO Threshold Output Chip	V_{UVLOH2}	—	12.0	12.6	V	
	V_{UVLOL2}	10.4	11.0	—	V	
UVLO Hysteresis Output Chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS2}	0.7	0.9	—	V	
Quiescent Current Input Chip	I_{Q1}	—	7	9	mA	V_{VCC1} =5V IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High
Quiescent Current Output Chip	I_{Q2}	—	4.5	6	mA	V_{VCC2} =15V V_{VEE2} =-8V IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High

4.4.2 Logic Input and Output

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
IN+,IN-, $\overline{RST}$ Low Input Voltage	V_{IN+L}, V_{IN-L}, $V_{\overline{RST}L}$	—	—	1.5	V	
IN+,IN-, $\overline{RST}$ High Input Voltage	V_{IN+H}, V_{IN-H} $V_{\overline{RST}H}$	3.5	—	—	V	
IN-, $\overline{RST}$ Input Current	I_{IN-}, $I_{\overline{RST}}$	—	100	400	uA	V_{IN-}=GND1 $V_{\overline{RST}}$=GND1
IN+ Input Current	I_{IN+},	—	100	400	uA	V_{IN+}=VCC1
RDY,$\overline{FLT}$ Pull Up Current	I_{PRDY}, $I_{\overline{PFLT}}$	—	100	400	uA	V_{RDY}=GND1 $V_{\overline{FLT}}$=GND1
Input Pulse Suppression IN+, IN-	T_{MININ+}, T_{MININ-}	30	40	—	ns	
Input Pulse Suppression $\overline{RST}$ for ENABLE/SHUTDOWN	T_{MINRST}	30	40	—	ns	
Pulse Width $\overline{RST}$ for Reseting $\overline{FLT}$	T_{RST}	800	—	—	ns	
$\overline{FLT}$ Low Voltage	V_{FLTL}	—	—	300	mV	$I_{SINK(\overline{FLT})}$ = 5mA
RDY Low Voltage	V_{RDYL}	—	—	300	mV	$I_{SINK(RDY)}$ = 5mA

4.4.3 Gate Driver

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
High Level Output Voltage	V_{OUTH1}	V_{VCC2}-1.2	V_{VCC2}-0.8	—	V	I_{OUTH} = -20mA
	V_{OUTH2}	V_{VCC2}-2.5	V_{VCC2}-2.0	—	V	I_{OUTH} = -200mA
	V_{OUTH3}	V_{VCC2}-9	V_{VCC2}-5	—	V	I_{OUTH} = -1A
	V_{OUTH4}		V_{VCC2}-10	—	V	I_{OUTH} = -2A
High Level Output Peak Current	I_{OUTH}	-1.5	-2.0	—	A	IN+ = High, IN- = Low; OUT = High
Low Level Output Voltage	V_{OUTL1}	—	V_{VEE2}+0.04	V_{VEE2}+0.09	V	I_{OUTL} = 20mA
	V_{OUTL2}	—	V_{VEE2}+0.3	V_{VEE2}+0.85	V	I_{OUTL} = 200mA
	V_{OUTL3}	—	V_{VEE2}+2.1	V_{VEE2}+5.0	V	I_{OUTL} = 1A
	V_{OUTL4}	—	V_{VEE2}+7	—	V	I_{OUTL} = 2A
Low Level Output Peak Current	I_{OUTL}	1.5	2.0	—	A	IN+ = Low, IN- = Low; OUT = Low, V_{VCC2} =15V, V_{VEE2} =-8V

4.4.4 Active Miller Clamp

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Low Level Clamp Voltage	$V_{CLAMPL1}$		V_{VEE2}+0.03	V_{VEE2} +0.08	V	I_{OUTL} = 20mA
	$V_{CLAMPL2}$		V_{VEE2}+0.3	V_{VEE2} +0.8	V	I_{OUTL} = 200mA
	$V_{CLAMPL3}$		V_{VEE2}+1.9	V_{VEE2} +4.8	V	I_{OUTL} = 1A
Low Level Clamp Current	I_{CLAMPL}	2	—	—	A	1)
Clamp Threshold Voltage	V_{CLAMP}	1.6	2.1	2.4	V	Related to VEE2

1) The parameter is not subject to production test - verified by design/characterization

4.4.5 Short Circuit Clamping

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Clamping voltage (OUT) (V_{OUT}-V_{VCC2})	V_{CLPout}	—	0.8	1.3	V	IN+=High, IN-=Low, OUT=High I_{OUT} = 500mA (pulse test,t_{CLPmax}=10us)
Clamping voltage (CLAMP) (V_{VCLAMP}-V_{VCC2})	$V_{CLPclamp}$	—	1.3	—	V	IN+=High, IN-=Low, OUT=High I_{CLAMP} = 500mA (pulse test,t_{CLPmax}=10us)
Clamping voltage (CLAMP)	$V_{CLPclamp}$	—	0.7	1.1	V	IN+=High, IN-=Low, OUT=High I_{CLAMP} = 20mA

4.4.6 Dynamic Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
IN+ Input to output propagation delay ON/OFF and IN- OFF	T_{PDON}	1.6	1.8	2.1	us	C_{TLSET}=0, TA=25°C
IN+ Input to output propagation delay distortion (TPDOFF-TPDON)	T_{PDISTO}	0	30	60	ns	C_{TLSET}=0, TA=25°C
IN- Input to output propagation delay ON	T_{PDON-}	1.6	1.8	tbd 2.8[1)]	us	C_{TLSET}=0, TA=25°C
IN- Input to output propagation delay distortion (TPDOFF-TPDON)	$T_{PDISTO-}$	tbd -545[1)]	30	60	ns	C_{TLSET}=0, TA=25°C
IN+ Input to output propagation delay ON/OFF and IN- OFF	T_{PDONt}	1.5	1.9	2.3	us	C_{TLSET}=0, TA=125°C
IN+ Input to output propagation delay distortion (TPDOFF-TPDON)	$T_{PDISTOt}$	0	40	70	ns	C_{TLSET}=0, TA=125°C
IN- Input to output propagation delay ON	T_{PDON-t}	1.5	1.9	tbd 3.0[1)]	us	C_{TLSET}=0, TA=125°C
IN- Input to output propagation delay distortion (TPDOFF-TPDON)	$T_{PDISTO-t}$	tbd -700[1)]	40	70	ns	C_{TLSET}=0, TA=125°C
IN+ Input to output propagation delay ON/OFF and IN- OFF	T_{PDONt}	1.5	1.8	2.3	us	C_{TLSET}=0, @TA=-40°C
IN+ Input to output propagation delay distortion (TPDOFF-TPDON)	$T_{PDISTOt}$	0	20	50	ns	C_{TLSET}=0, @TA=-40°C
IN- Input to output propagation delay ON	T_{PDON-t}	1.5	1.8	tbd 3.0[1)]	us	C_{TLSET}=0, @TA=-40°C
IN- Input to output propagation delay distortion (TPDOFF-TPDON)	$T_{PDISTO-t}$	tbd -700[1)]	20	50	ns	C_{TLSET}=0, @TA=-40°C
Rise Time	T_{RISE}	10	30	60	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 1nF, VL 10% ,VH 90%
		150	400	800	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 34nF VL 10% ,VH 90%
Fall Time	T_{FALL}	10	20	40	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 1nF VL 10% ,VH 90%
		100	250	500	ns	V_{VCC2}=15V,V_{VEE2}=-8V C_{LOAD}= 34nF VL 10% ,VH 90%

1) The maximum value of input to output propagation delay ON at IN- occures only in case of electromagnetic interferences, typically the input to output delay is 2.1µs at TA =25°C, one worst case watchdog clock cycle shorter (see chapter 2.2.3). The turn OFF-signal is prioritized/dominant and will not show up this behavior.

4.4.7 Desaturation protection

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Blanking Capacitor Charge Current	I_{DESATC}	450	500	550	uA	V_{VCC2}=15V,V_{VEE2}=-8V V_{DESAT}=2V
Blanking Capacitor Discharge Current	I_{DESATD}	11	15	—	mA	V_{VCC2}=15V,V_{VEE2}=-8V V_{DESAT}=6V
Desaturation Reference Level	V_{DESAT}	8.5	9	9.5	V	V_{VCC2}=15V,V_{VEE2}=-8V
Desaturation Reference Level	V_{DESAT}	8.5	9	9.5	V	V_{VCC2}=15V,V_{VEE2}=0V
Desaturation Sense to OUT TLTO	$T_{DESATOUT}$	—	270	320	ns	V_{OUT}=90% C_{LOAD}= 1nF
Desaturation Sense to FLT Low Delay	$T_{DESATFLT}$	—		2.25	us	$V_{\overline{FLT}}$=10%; $I_{\overline{FLT}}$=5mA
Desaturation Low Voltage	V_{DESATL}	40	70	110	mV	IN+=Low, IN-=Low, OUT=Low

4.4.8 Active Shut Down

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Active Shut Down Voltage	V_{ACTSD} [1)]	—	—	2.0	V	I_{OUT}=-200mA, V_{CC2} open

1) With reference to VEE2

4.4.9 Two-level Turn-off

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
External reference voltage range (Zener-Diode)	V_{ZDIODE}	7.5	—	VCC2-0.5	V	
Reference Voltage for setting two-level delay time	V_{TLSET}	6.6	7	7.3	V	
Current for setting two-level delay time and external reference voltage (Zener-Diode)	I_{TLSET}	420	500	550	uA	V_{TLSET}=10V
External Capacitance Range	C_{TLSET}	0	—	220	pF	

5 Insulation Characteristics

5.1 Complies with DIN EN 60747-5-2 (VDE 0884 Teil 2): 2003-01. Basic Insulation

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1 for rated mains voltage ≤ 150 V_{RMS} for rated mains voltage ≤ 300 V_{RMS} for rated mains voltage ≤ 600 V_{RMS}		 I-IV I-III I-II	
Climatic Classification		40/125/21	
Pollution Degree (EN 60664-1)		2	
Minimum External Clearance	CLR	8	mm
Minimum External Creepage	CPG	8	mm
Minimum Comparative Tracking Index	CTI	175	
Maximum Repetitive Insulation Voltage	V_{IORM}	1420	V_{PEAK}
Highest Allowable Overvoltage[1)]	V_{IOTM}	6000	V_{PEAK}
Maximum Surge Insulation Voltage	V_{IOSM}	6000	V

5.2 According to UL 1577

Description	Symbol	Characteristic	Unit
Insulation Withstand Voltage / 1min	V_{ISO}	3750	V_{rms}
Insulation Test Voltage / 1sec	V_{ISO}	4500	V_{rms}

5.3 Reliability

For Qualification Report please contact your local Infineon Technologies office.

6 Timing Diagrams

All diagrams related to the Two-level switch-off feature

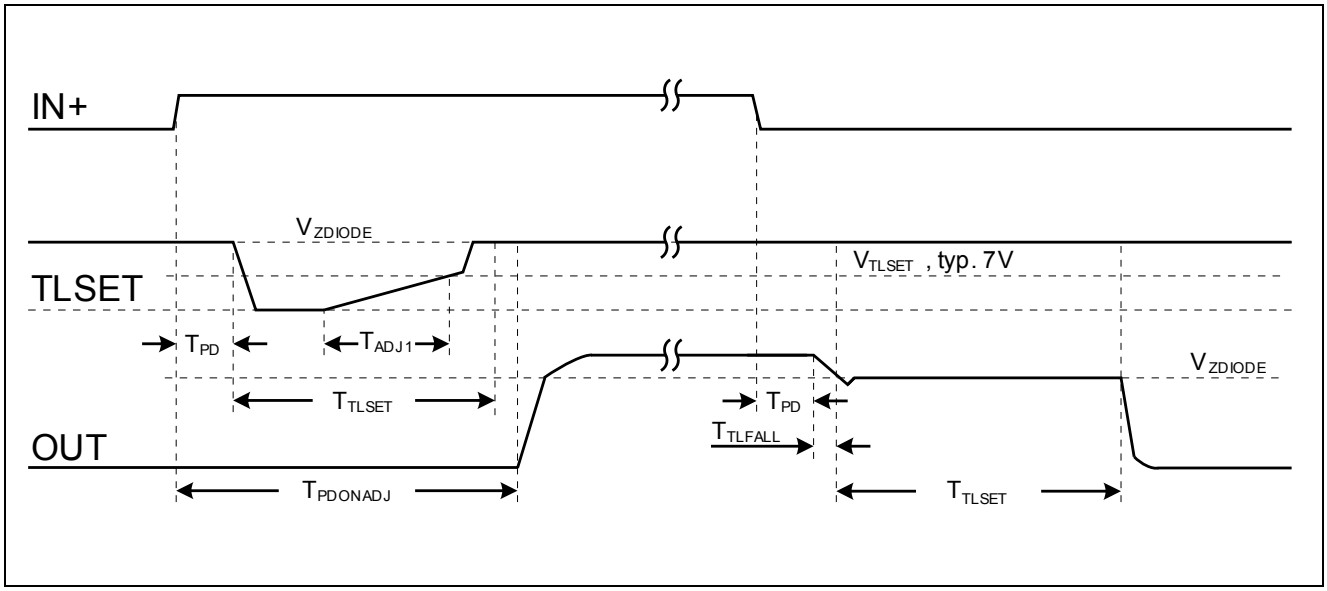

Figure 4: Typical Switching Behavior

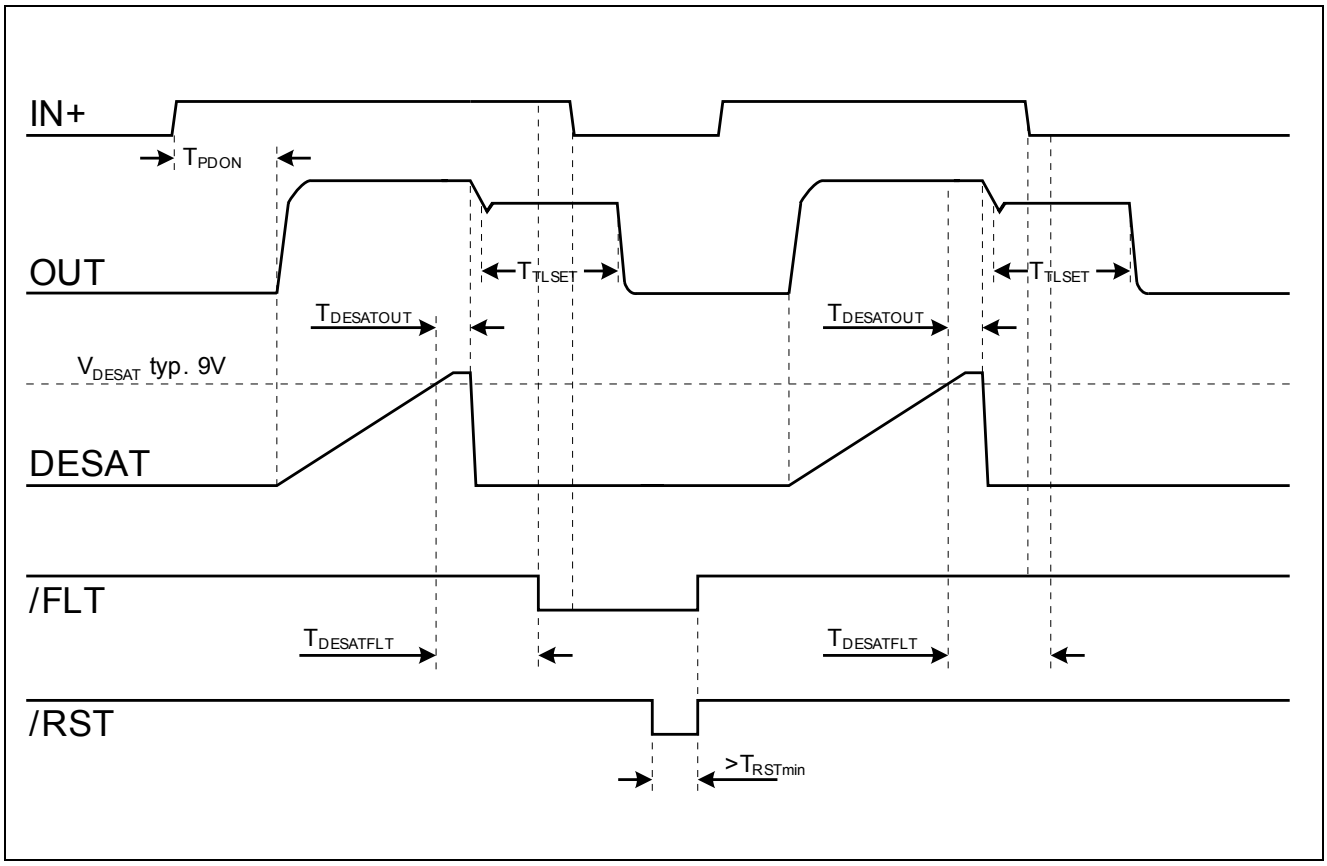

Figure 5: DESAT Switch-OFF Behavior

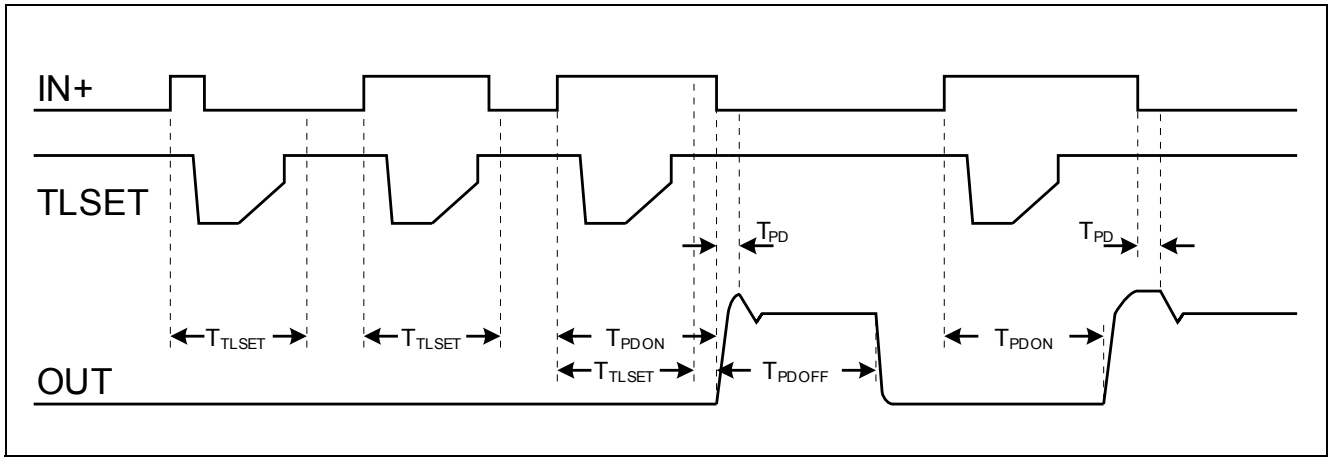

Figure 6: Short Switch ON Pulses

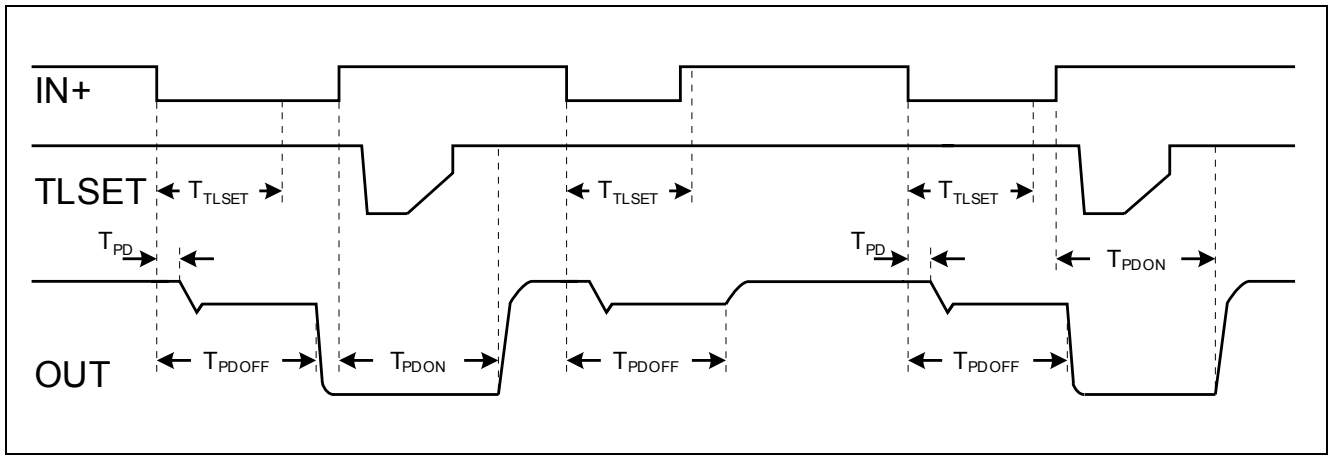

Figure 7: Short Switch OFF Pulses

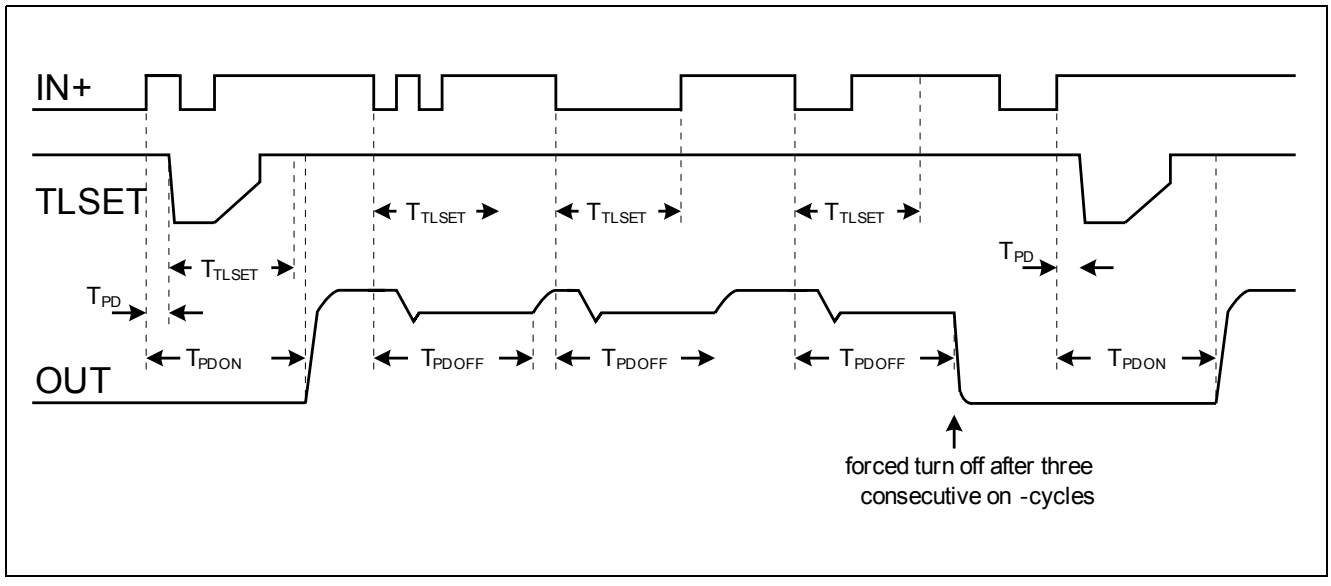

Figure 8: Short Switch OFF Pulses, Ringing Surpression

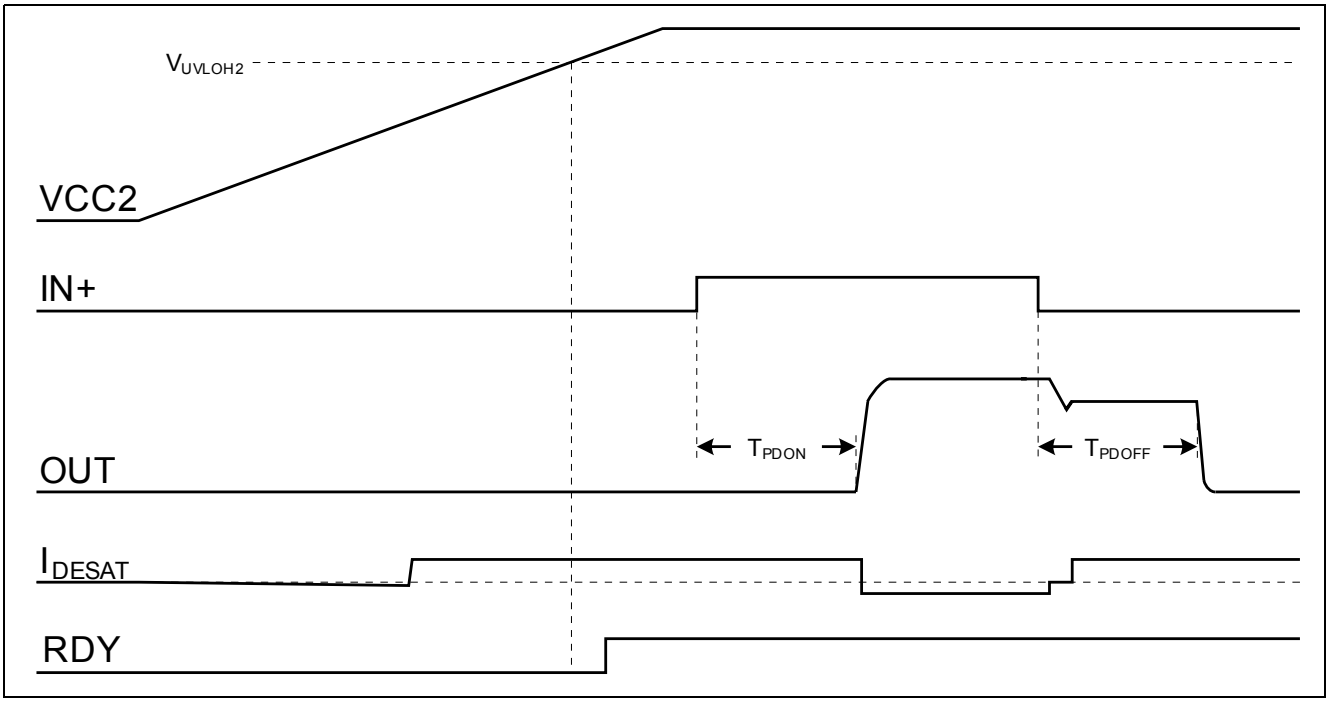

Figure 9: VCC2 Ramp Up

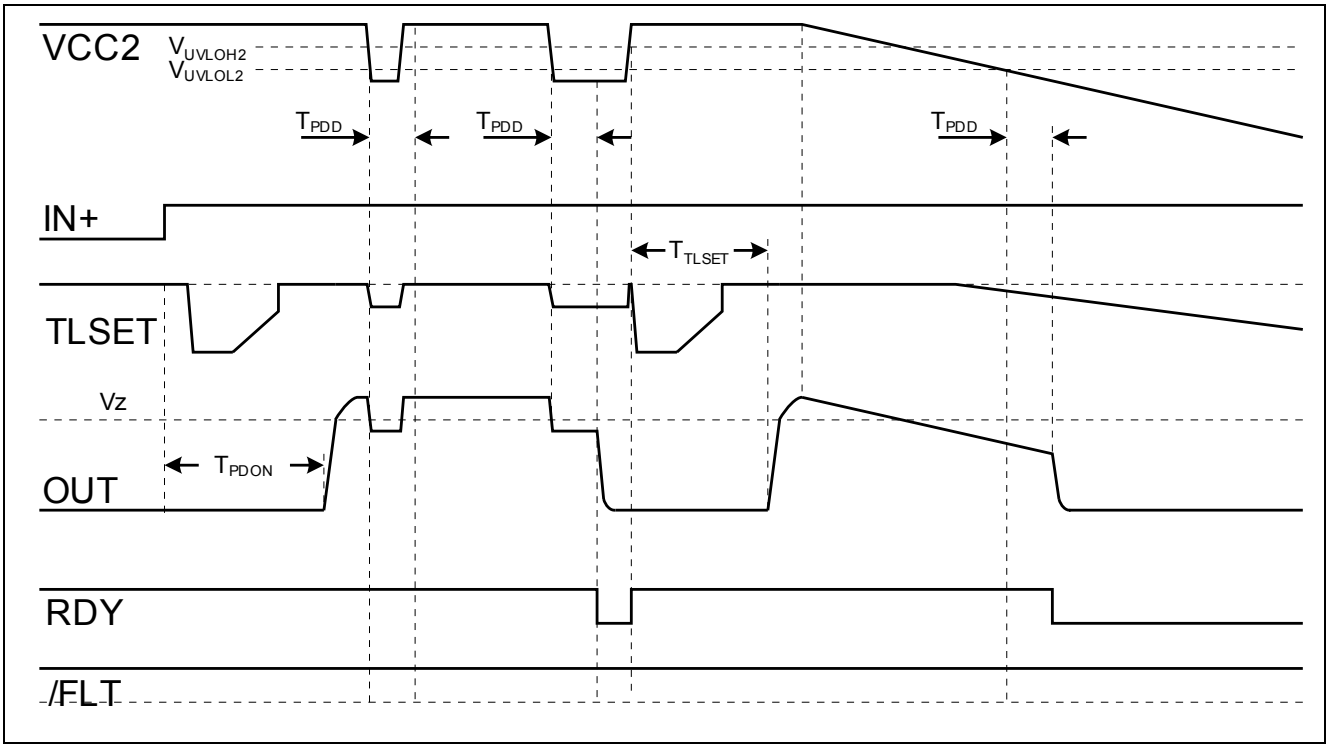

Figure 10: VCC2 Ramp Down and VCC2 Drop

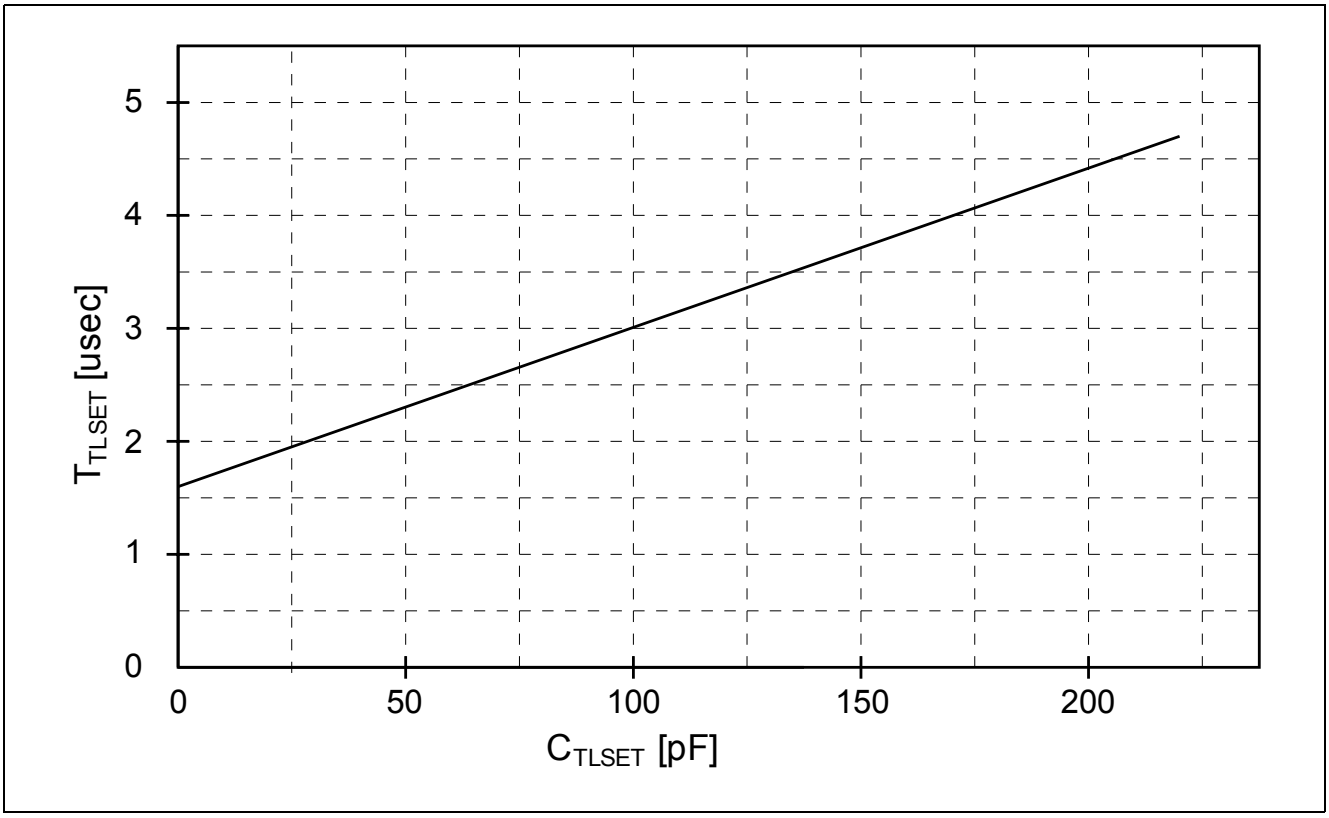

Figure 11: Typical T_{TLSET} Time over C_{TLSET} Capacitance

7 Package Outlines

PG-DSO-20-55

(Plastic Dual Small Outline Package)

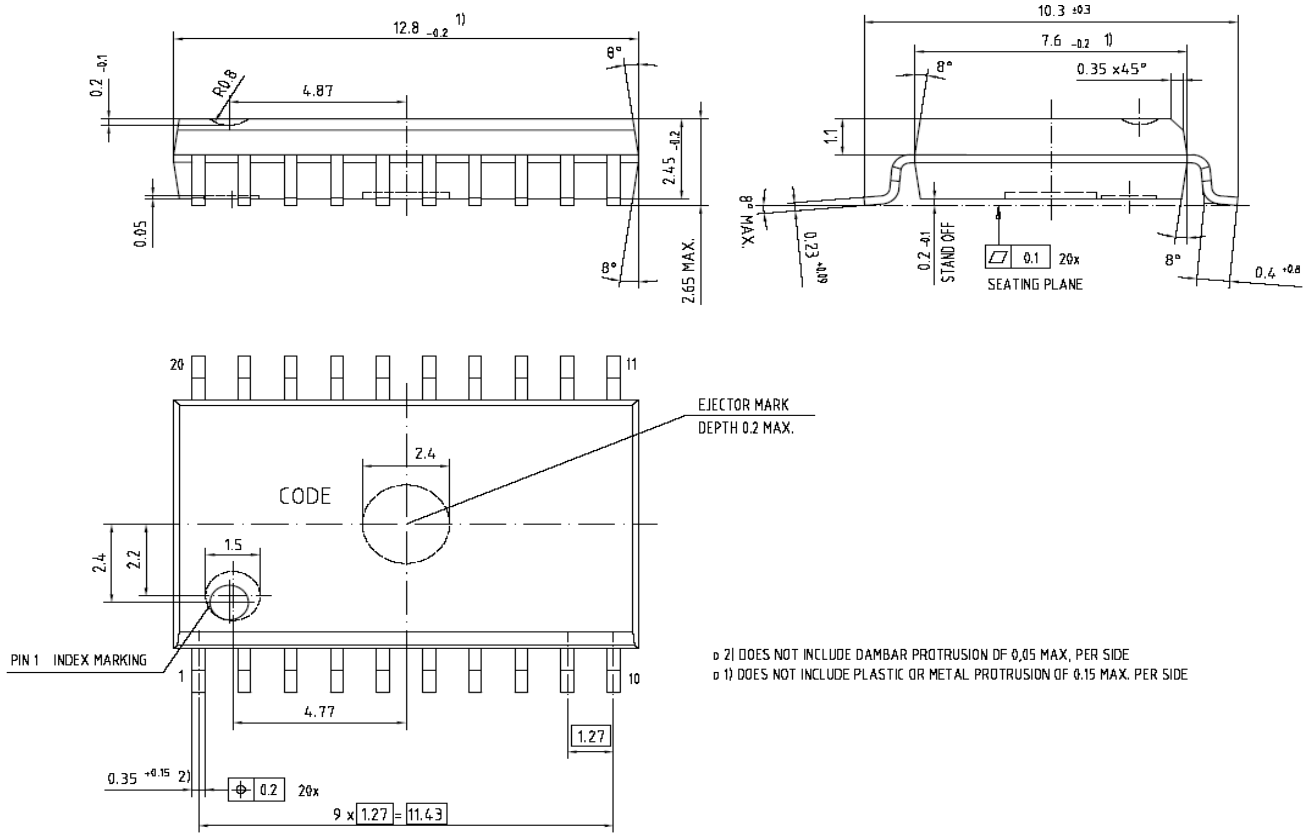

Figure 12: PG-DSO-20-55

8 Application Notes

8.1 Reference Layout for Thermal Data

The PCB layout shown in figure 12 represents the reference layout used for the thermal characterisation. Pins 11, 12, 19 and 20 (GND1) and pins 1, 2, 9 and 10 (VEE2) require ground plane connections for achiving maximum power dissipation. The 1ED020I12FTA is conceived to dissipate most of the heat generated through this pins.

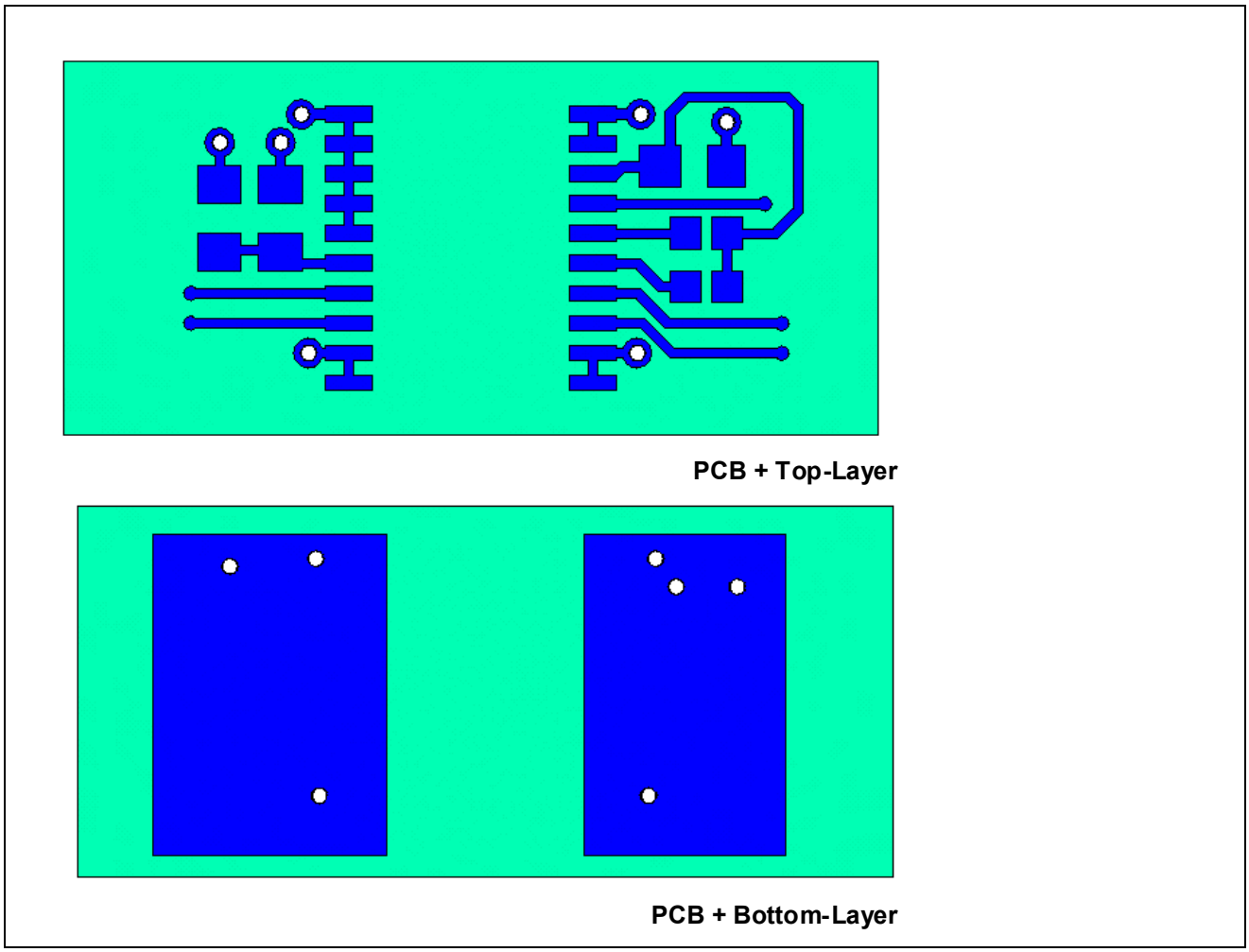

Figure 13: Reference layout for thermal data (Copper thickness 102mm)

8.2 Printed Circuit Board Guidelines

Following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.

- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and reduce parasitic coupling.

- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.

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