

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and GSM EDGE base station applications with frequencies from 864 to 894 MHz. Suitable for CDMA and multicarrier amplifier applications.

- Typical GSM Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 300$ mA, $P_{out} = 35.5$ Watts CW

Frequency	G_{ps} (dB)	η_D (%)
864 MHz	19.9	58.7
880 MHz	20	58.5
894 MHz	19.8	57.7

- Capable of Handling 5:1 VSWR, @ 32 Vdc, 880 MHz, 70 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out}), Designed for Enhanced Ruggedness
- Typical P_{out} @ 1 dB Compression Point ≈ 47 Watts CW
- Typical GSM EDGE Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 285$ mA, $P_{out} = 17.8$ Watts Avg.

Frequency	G_{ps} (dB)	η_D (%)	Spectral Regrowth @ 400 kHz (dBc)	Spectral Regrowth @ 600 kHz (dBc)	EVM (% rms)
864 MHz	19.8	43.8	61.2	70.9	2.1
880 MHz	19.9	43.6	63.4	72.5	2
894 MHz	19.8	43.1	63.7	73	2

Features

- Class F Output Matched for Higher Impedances and Greater Efficiency
- Designed for High Efficiency. Typical Drain Efficiency @ P1dB $\approx 66\%$
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +66	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

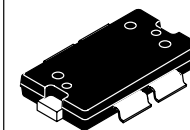
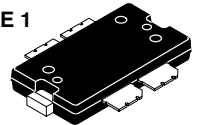
1. Continuous use at maximum temperature will affect MTTF.

2. MTTF calculator available at <http://www.freescale.com/rtf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

MRFE6S8046NR1
MRFE6S8046GNR1

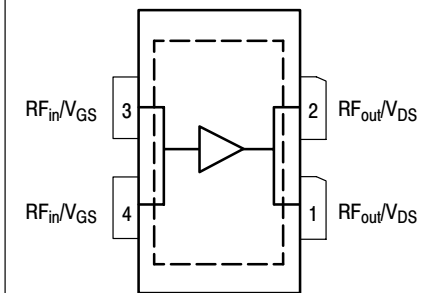
864-894 MHz, 35.5 W CW, 28 V
GSM, GSM EDGE
LATERAL N-CHANNEL
RF POWER MOSFETs

CASE 1486-03, STYLE 1
TO-270 WB-4
PLASTIC
MRFE6S8046NR1



CASE 1487-05, STYLE 1
TO-270 WB-4 GULL
PLASTIC
MRFE6S8046GNR1

PARTS ARE SINGLE-ENDED



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 35.5 W CW, 28 Vdc, I _{DQ} = 300 mA Case Temperature 82°C, 18 W CW, 28 Vdc, I _{DQ} = 285 mA	R _{θJC}	1.7 1.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics

Zero Gate Voltage Drain Leakage Current (V _{DS} = 66 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 100 μAdc)	V _{GS(th)}	1	2.3	3	Vdc
Gate Quiescent Voltage (V _{DD} = 28 Vdc, I _D = 300 mAdc, Measured in Functional Test)	V _{GS(Q)}	2	3	4	Vdc
Drain-Source On-Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	0.1	0.3	0.4	Vdc

Functional Tests ^(3,4) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, P_{out} = 35.5 W CW, I_{DQ} = 300 mA, f = 894 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G _{ps}	17.5	19.8	21.5	dB
Drain Efficiency	η _D	54	57.7	—	%
Input Return Loss	IRL	—	-17	-7	dB

1. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
3. Part internally matched both on input and output.
4. Measurement made with device in straight lead configuration before any lead forming operation is applied.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)**Typical Broadband Performance** (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 300\text{ mA}$, $P_{out} = 35.5\text{ W CW}$

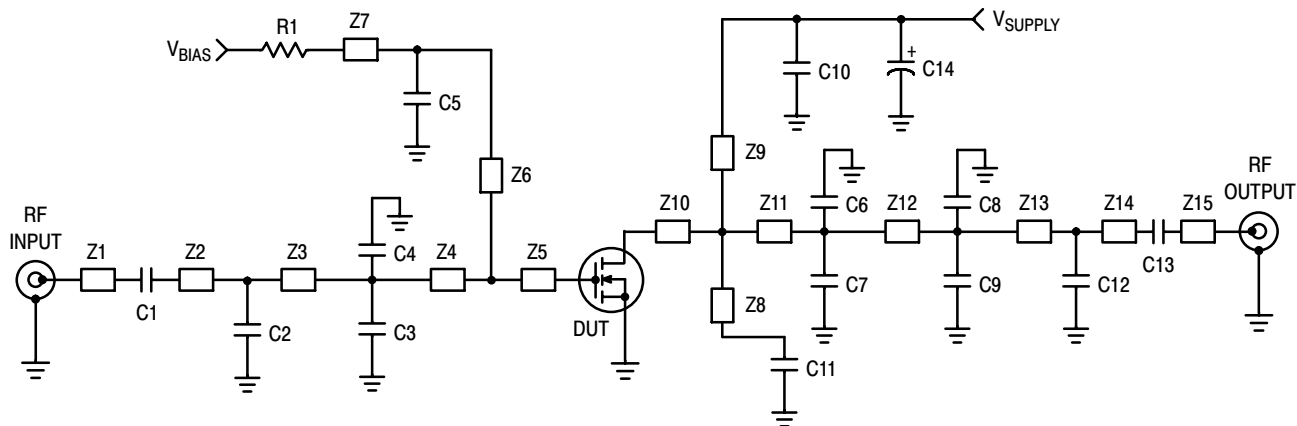
Frequency	G_{ps} (dB)	η_D (%)	IRL (dB)
864 MHz	19.9	58.7	-12
880 MHz	20	58.5	-17
894 MHz	19.8	57.7	-17

Typical Performances (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 300\text{ mA}$, 864-894 MHz Bandwidth

Characteristic	Symbol	Min	Typ	Max	Unit
P_{out} @ 1 dB Compression Point	P1dB	—	47	—	W
IMD Symmetry @ 41 W PEP, P_{out} where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands $> 2\text{ dB}$)	IMD _{sym}	—	22	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW _{res}	—	25	—	MHz
Gain Flatness in 30 MHz Bandwidth @ $P_{out} = 35.5\text{ W CW}$	G_F	—	0.2	—	dB
Gain Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔG	—	0.017	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔP_{1dB}	—	0.004	—	dBm/ $^\circ\text{C}$

Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 285\text{ mA}$, $P_{out} = 17.8\text{ W Avg.}$, 864-894 MHz EDGE Modulation

Frequency	G_{ps} (dB)	η_D (%)	Spectral Regrowth @ 400 kHz (dBc)	Spectral Regrowth @ 600 kHz (dBc)	EVM (% rms)
864 MHz	19.8	43.8	61.2	70.9	2.1
880 MHz	19.9	43.6	63.4	72.5	2
894 MHz	19.8	43.1	63.7	73	2



Z1	1.320" x 0.044" Microstrip	Z10	0.040" x 0.450" Microstrip
Z2	0.212" x 0.044" Microstrip	Z11	0.321" x 0.450" Microstrip
Z3	0.362" x 0.044" Microstrip	Z12	0.080" x 0.280" Microstrip
Z4	0.321" x 0.450" Microstrip	Z13	0.263" x 0.044" Microstrip
Z5	0.039" x 0.450" Microstrip	Z14	0.233" x 0.044" Microstrip
Z6*	0.306" x 0.040" Microstrip	Z15	1.332" x 0.044" Microstrip
Z7	0.708" x 0.051" Microstrip	PCB	Rogers R04350, 0.020", $\epsilon_r = 3.50$
Z8* Z9*	0.738" x 0.040" Microstrip		

* Line length includes microstrip bends

Figure 2. MRFE6S8046NR1 (GNR1) Reference Design Test Circuit Schematic

Table 6. MRFE6S8046NR1 (GNR1) Reference Design Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C13	56 pF Chip Capacitors	ATC600F560BT500XT	ATC
C2	3.9 pf Chip Capacitor	ATC600F3R0BT250XT	ATC
C3, C4	8.2 pF Chip Capacitors	ATC600F8R2BT500XT	ATC
C5	0.01 μ F Chip Capacitor	C1825C103K1GAC	Kemet
C6, C7	1.5 pF Chip Capacitors	ATC600F1R5BT250XT	ATC
C8, C9	1.2 pF Chip Capacitors	ATC600F1R2BT250XT	ATC
C10, C11	39 pF Chip Capacitors	ATC600F390BT500XT	ATC
C12	6.8 pF Chip Capacitor	ATC600F6R8BT500XT	ATC
C14	470 μ F 63V Electrolytic Capacitor	MCGPR63V477M13X26-RH	MultiComp
R1	4.7 K Ω , 1/4 W Chip Resistor	CRCW12064K70FKEA	Vishay

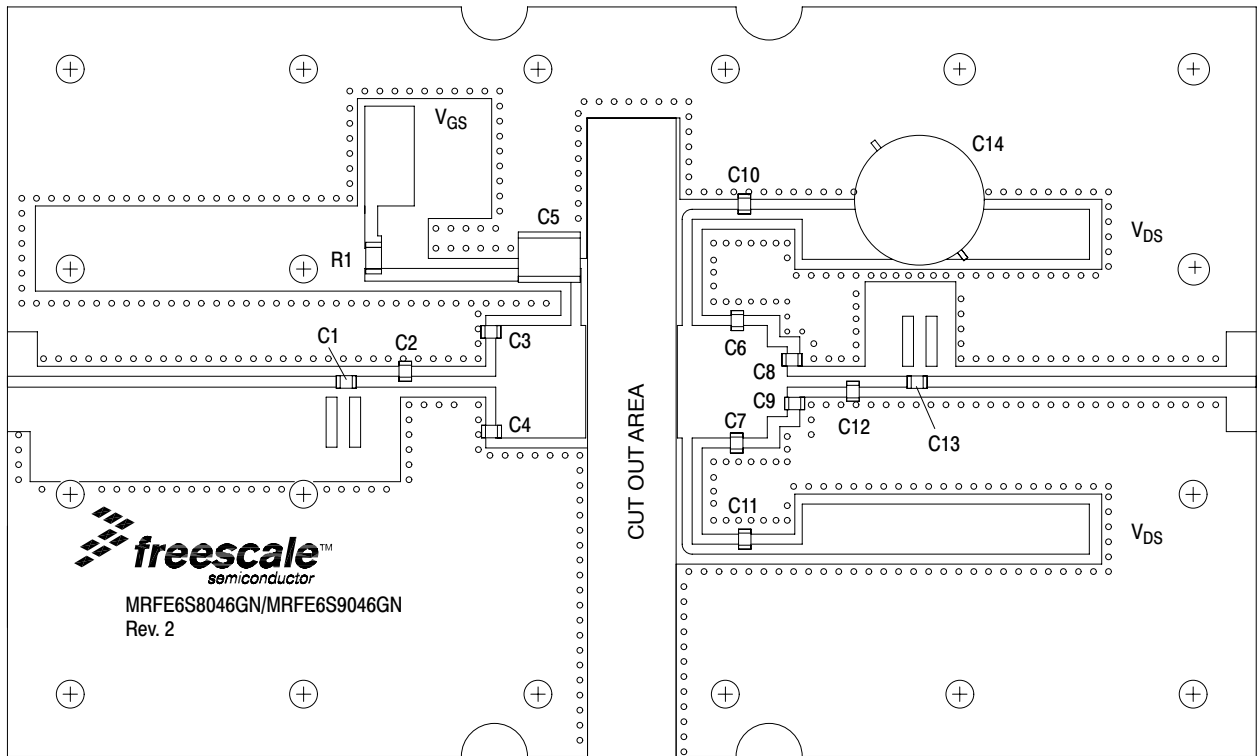


Figure 3. MRFE6S8046NR1(GNR1) Reference Design Test Circuit Component Layout

TYPICAL CHARACTERISTICS

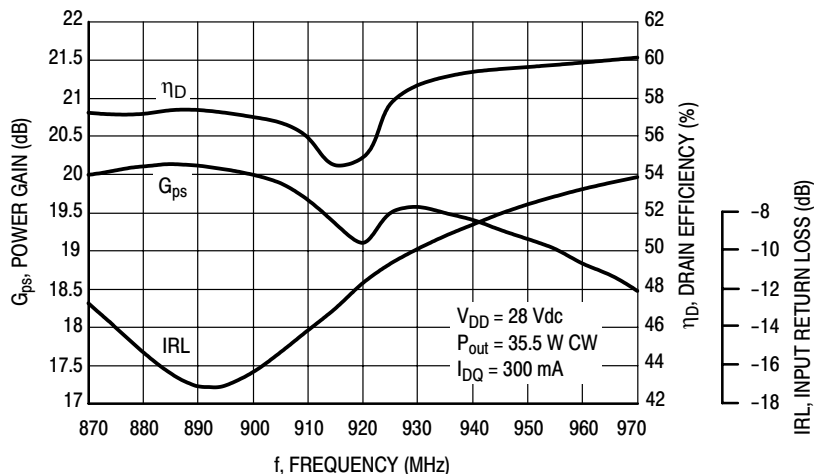


Figure 4. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @ $P_{out} = 35.5$ Watts CW

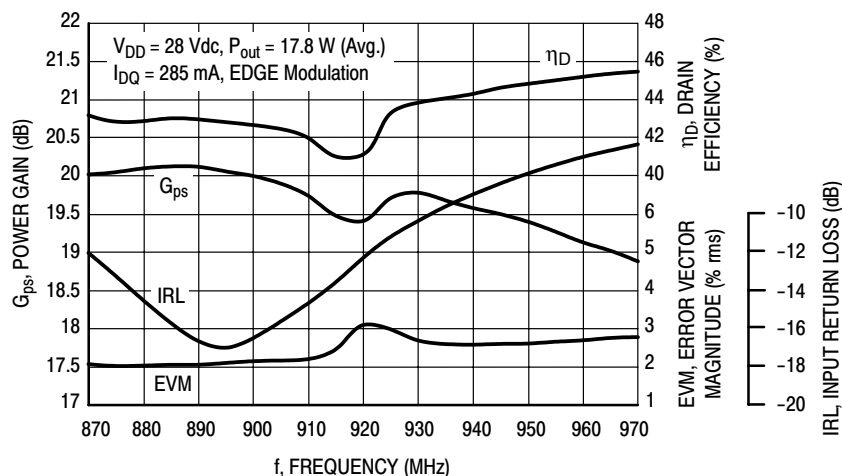


Figure 5. Power Gain, Input Return Loss, EVM and Drain Efficiency versus Frequency @ $P_{out} = 17.8$ Watts Avg.

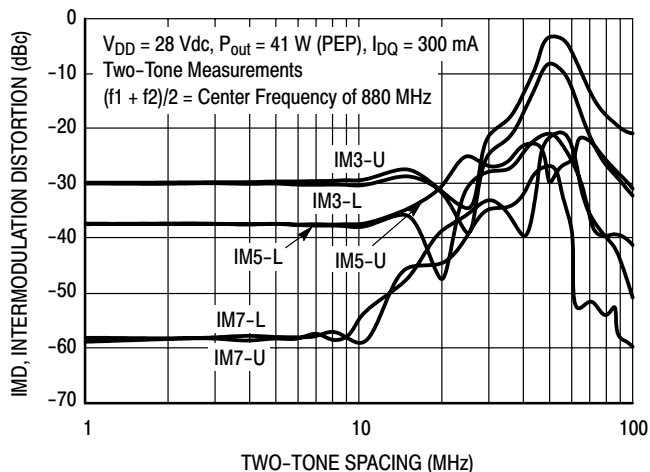


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

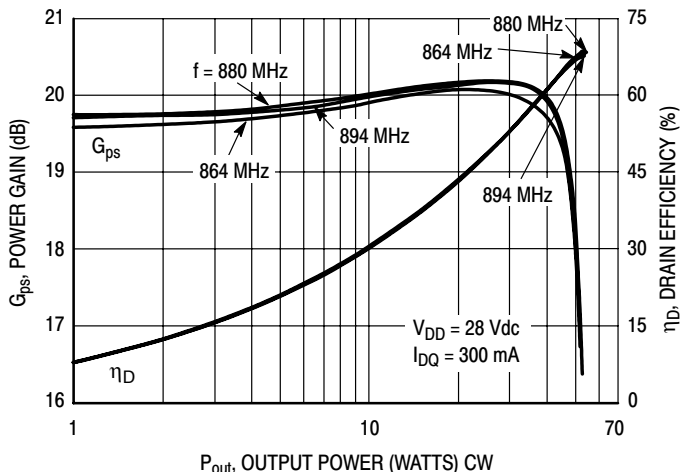


Figure 7. Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS

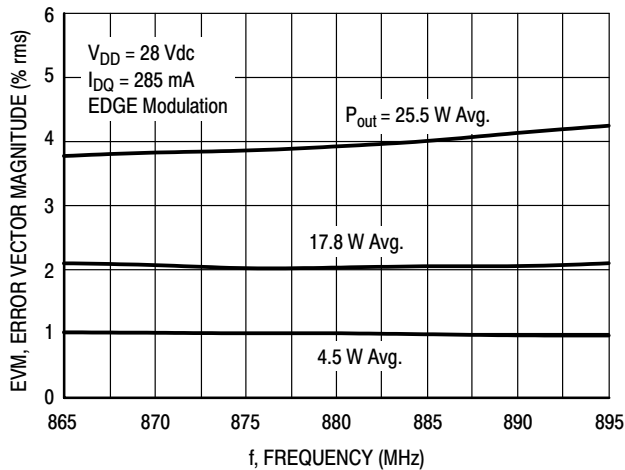


Figure 8. EVM versus Frequency

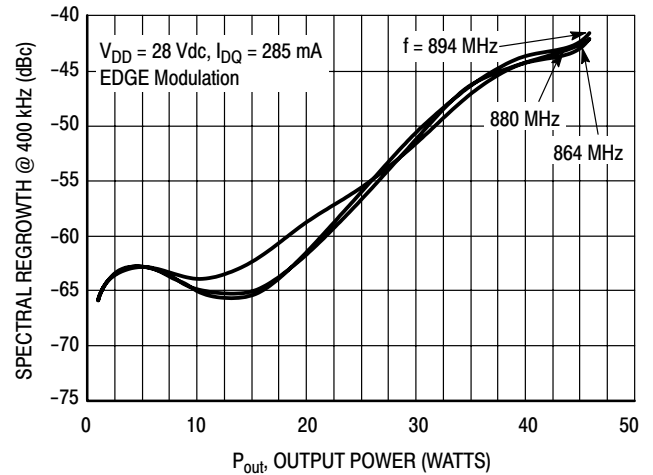


Figure 9. Spectral Regrowth at 400 kHz versus Output Power

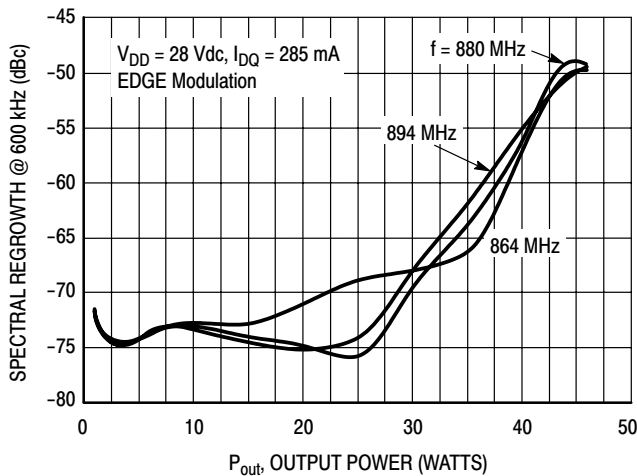


Figure 10. Spectral Regrowth at 600 kHz versus Output Power

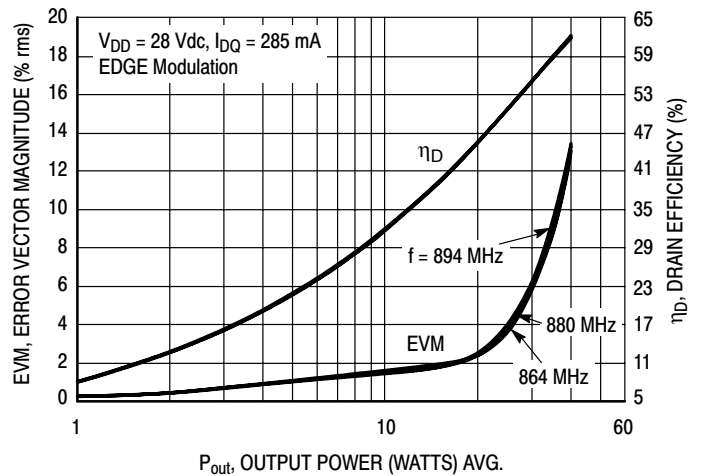


Figure 11. EVM and Drain Efficiency versus Output Power

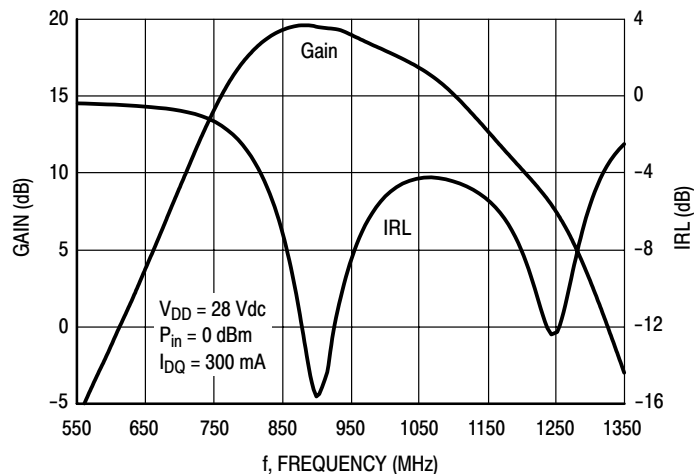


Figure 12. Broadband Frequency Response

GSM TEST SIGNAL

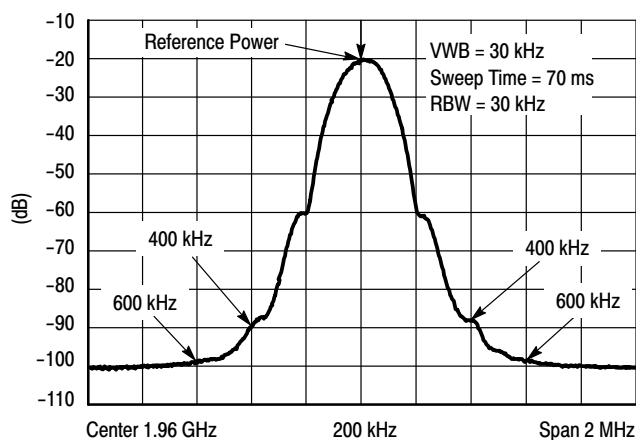


Figure 13. EDGE Spectrum

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 300 \text{ mA}$, $P_{out} = 35.5 \text{ W CW}$

f (MHz)	$Z_{source} \Omega$	$Z_{load} \Omega$
820	4.11 - j6.76	7.93 - j3.90
840	3.74 - j6.21	7.23 - j3.60
860	3.42 - j5.75	6.71 - j3.29
880	3.17 - j5.29	6.27 - j2.95
900	2.94 - j4.86	5.87 - j2.61
920	2.78 - j4.47	5.33 - j2.29
940	2.65 - j4.14	5.32 - j1.62
960	2.51 - j3.82	5.15 - j1.35
980	2.38 - j3.57	4.98 - j1.00

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

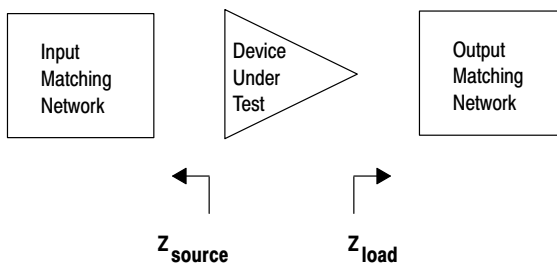
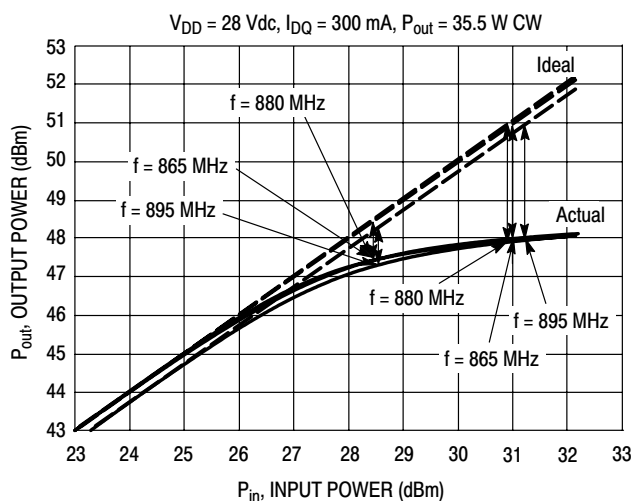


Figure 14. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

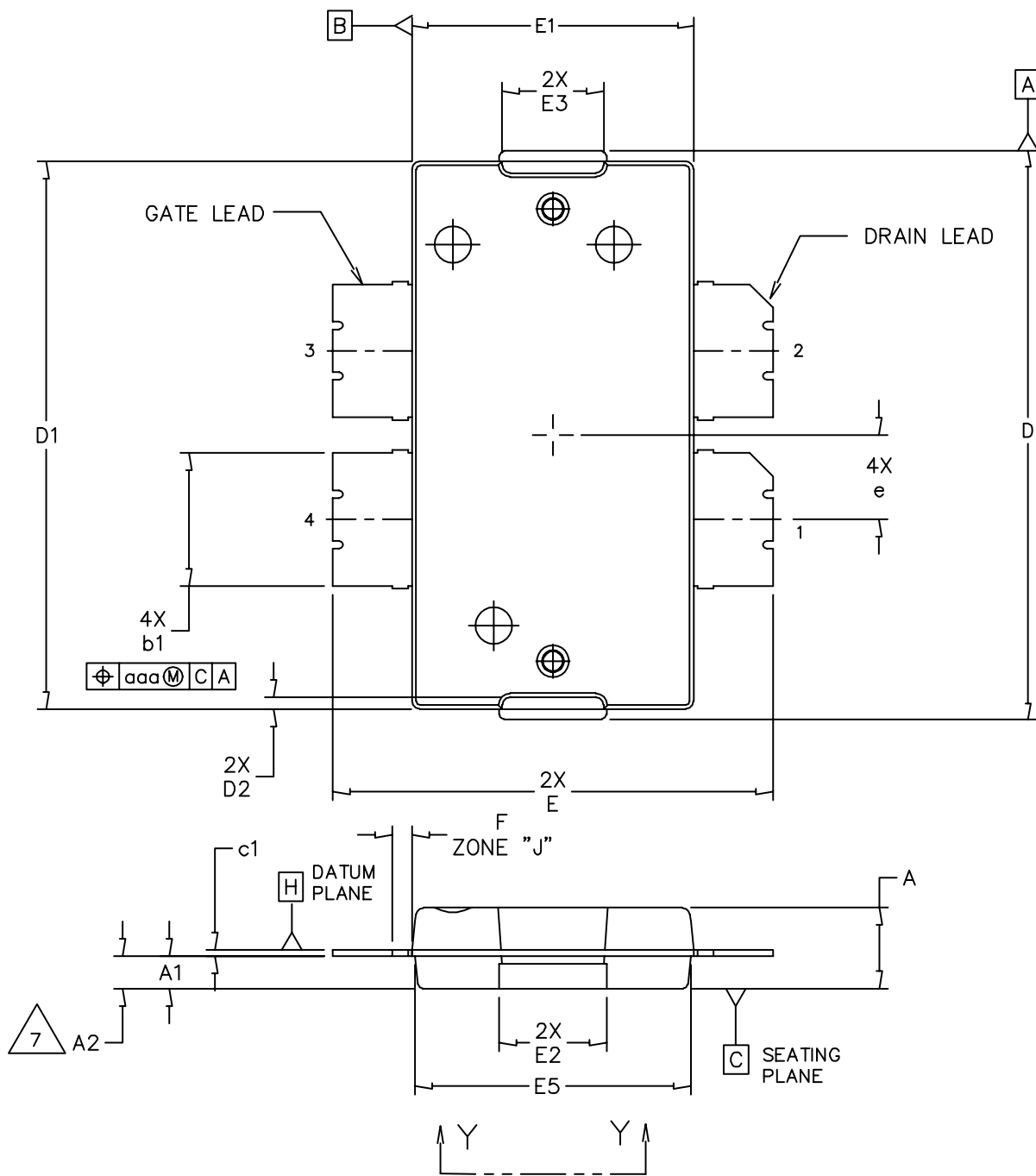
f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
865	55	47.4	63	48.0
880	55	47.4	62	47.9
895	54	47.3	62	47.9

Test Impedances per Compression Level

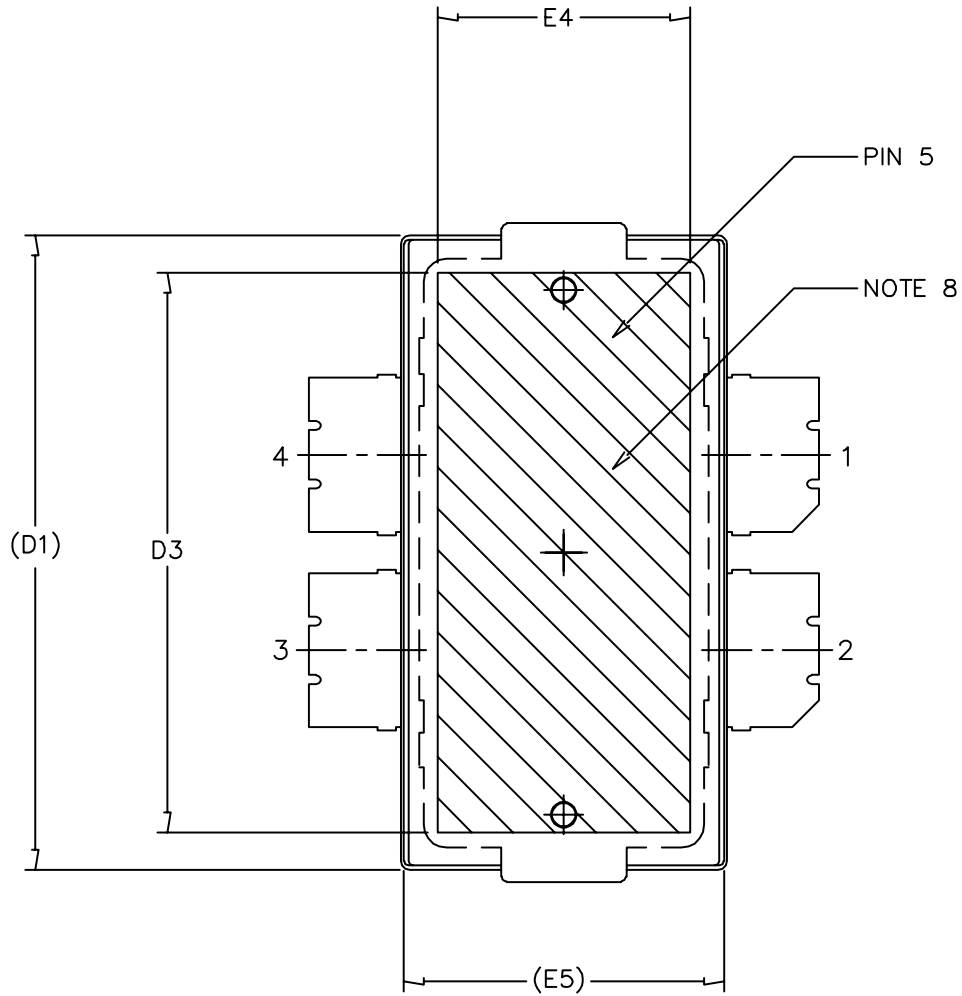
f (MHz)		Z_{source} Ω	Z_{load} Ω
865	P1dB	2.08 - j5.40	4.39 - j2.89
880	P1dB	2.54 - j5.63	4.63 - j2.96
895	P1dB	3.31 - j6.08	4.42 - j3.30

Figure 15. Pulsed CW Output Power versus Input Power @ 28 V

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-270 4 LEAD, WIDE BODY		DOCUMENT NO: 98ASA10577D	REV: D
		CASE NUMBER: 1486-03	13 AUG 2007
		STANDARD: NON-JEDEC	



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 4 LEAD, WIDE BODY		DOCUMENT NO: 98ASA10577D	REV: D
		CASE NUMBER: 1486-03	13 AUG 2007
		STANDARD: NON-JEDEC	

NOTES:

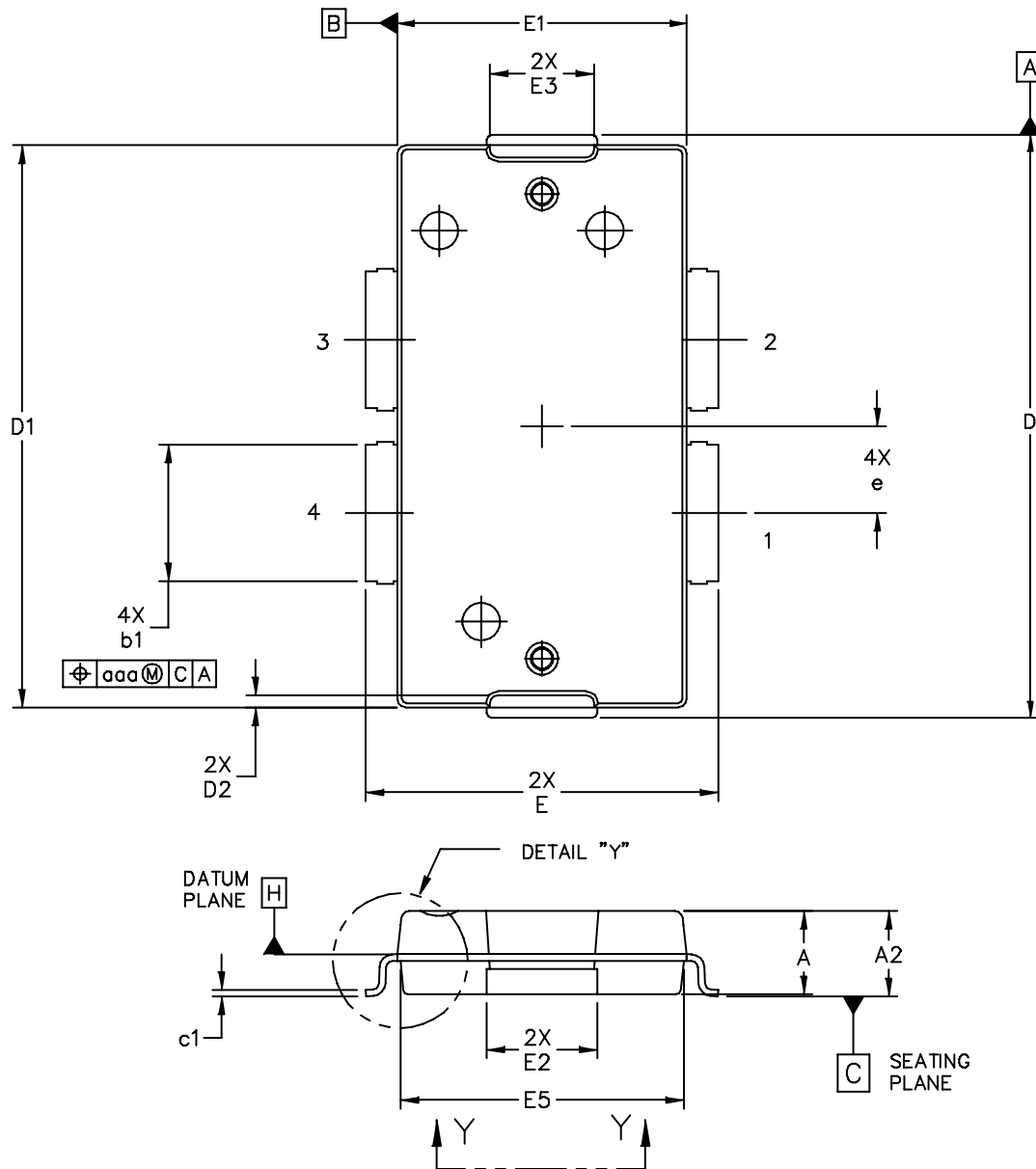
1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:

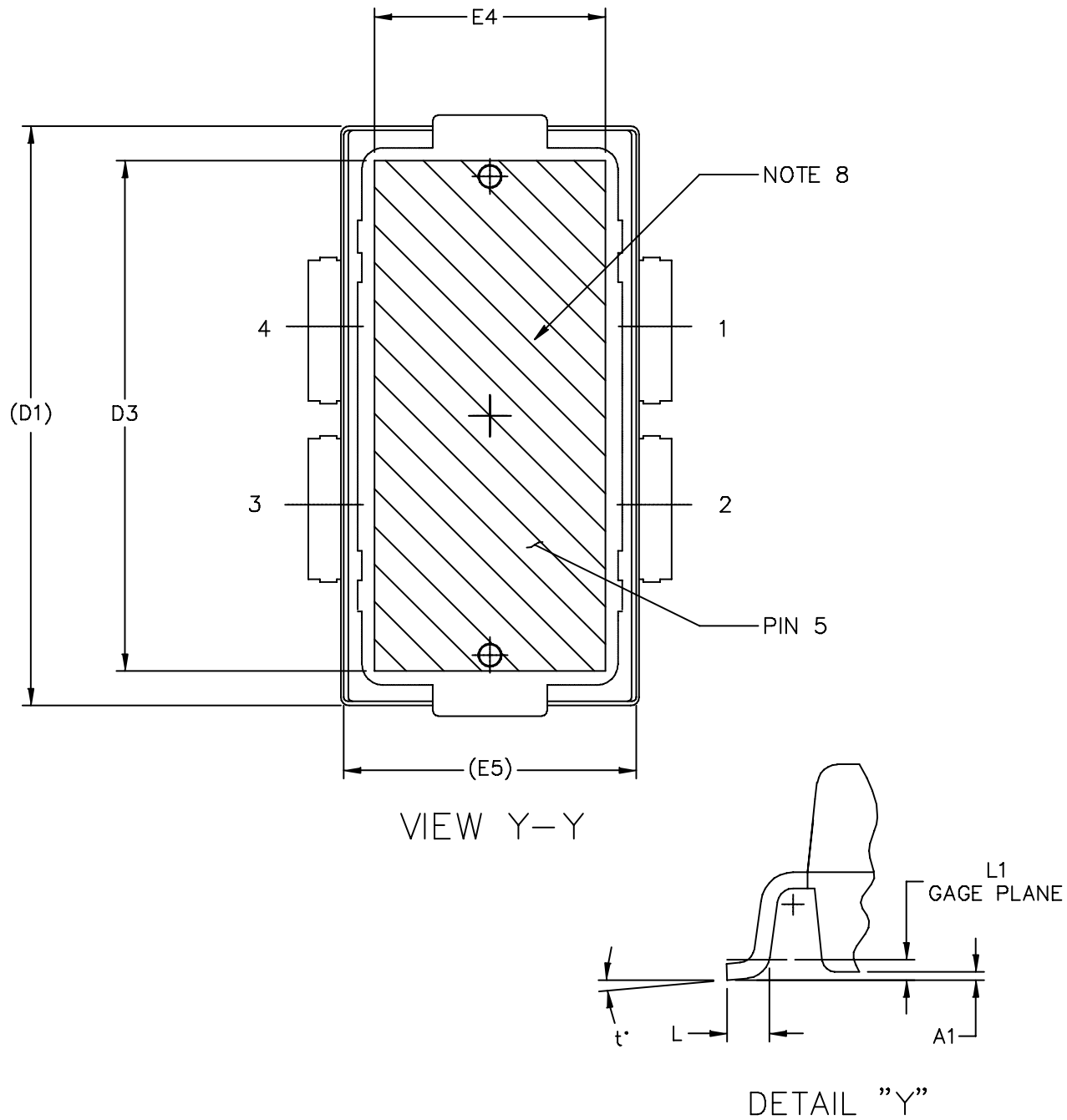
PIN 1 - DRAIN PIN 2 - DRAIN
 PIN 3 - GATE PIN 4 - GATE
 PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: TO-270 4 LEAD WIDE BODY		DOCUMENT NO: 98ASA10577D		REV: D	
		CASE NUMBER: 1486-03		13 AUG 2007	
		STANDARD: NON-JEDEC			



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 4 LEAD, WIDE BODY GULL WING	DOCUMENT NO: 98ASA10578D	REV: D	
	CASE NUMBER: 1487-05	03 AUG 2007	
	STANDARD: JEDEC TO-270 BB		



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-270 4 LEAD, WIDE BODY GULL WING	DOCUMENT NO: 98ASA10578D	REV: D	
	CASE NUMBER: 1487-05	03 AUG 2007	
	STANDARD: JEDEC TO-270 BB		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:

- PIN 1 - DRAIN
- PIN 2 - DRAIN
- PIN 3 - GATE
- PIN 4 - GATE
- PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.01 BSC		0.25 BSC	
A2	.101	.108	2.56	2.74	b1	.164	.170	4.17	4.32
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.106 BSC		2.69 BSC	
D2	.011	.019	0.28	0.48	t	2'	8'	2'	8'
D3	.600	----	15.24	----	aaa	.004		0.1	
E	.429	.437	10.90	11.10					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	----	6.86	----					
E5	.346	.350	8.79	8.89					

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: TO-270 4 LEAD, WIDE BODY GULL WING			DOCUMENT NO: 98ASA10578D		REV: D
			CASE NUMBER: 1487-05		03 AUG 2007
			STANDARD: JEDEC TO-270 BB		

PRODUCT DOCUMENTATION

Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2009	<ul style="list-style-type: none">• Initial Release of Data Sheet

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2009. All rights reserved.

