MHS

September 1989

DATA SHEET

HM 65161

2 k x 8
GENERAL PURPOSE CMOS SRAM

FEATURES

- **ACCESS TIME**
  MILITARY: 90 ns (max)
  INDUSTRIAL : 80 ns (max)
  COMMERCIAL : 70 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 240 mW (typ)
  STANDBY : 25 µW (typ)
  DATA RETENTION : 4 µW (typ)
- **600 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **SINGLE 5 VOLT SUPPLY**
- **EQUAL CYCLE AND ACCESS TIME**
- **NO CLOCK AND STROBES REQUIRED**
- **GATED INPUTS**
- **WIDE TEMPERATURE RANGE : – 55 TO + 125°C**

DESCRIPTION

The HM 65161 is a low power CMOS static RAM organized as 2048 x 8 bits. It is manufactured using the MHS high performance CMOS technology.
70 ns access time for commercial temperature range is available with a maximum power consumption of only 385mW.
The HM 65161 features fully static operation requiring no external clocks or timing strobes. Thanks to the special input buffer "gated inputs", the circuit stays in stand by mode when the $\overline{CS}$ goes to an intermediate level (VIH).
Easy memory expansion is provided by an active low chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.
The HM 65161 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM-65161 is processed following the test methods of MIL STD 883C.

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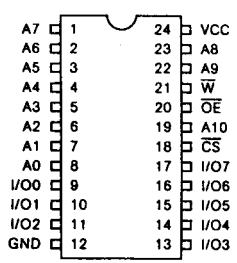
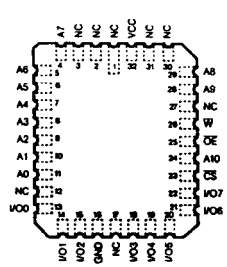
PACKAGES

Plastic 600 mils, 24 pins, DIL.
Ceramic 600 mils, 24 pins, DIL.
LCC, 32 pins.

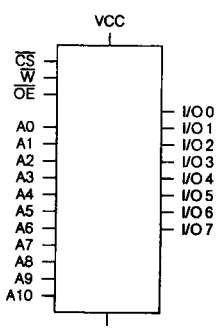
Pinout DIL 24 pins (top view)



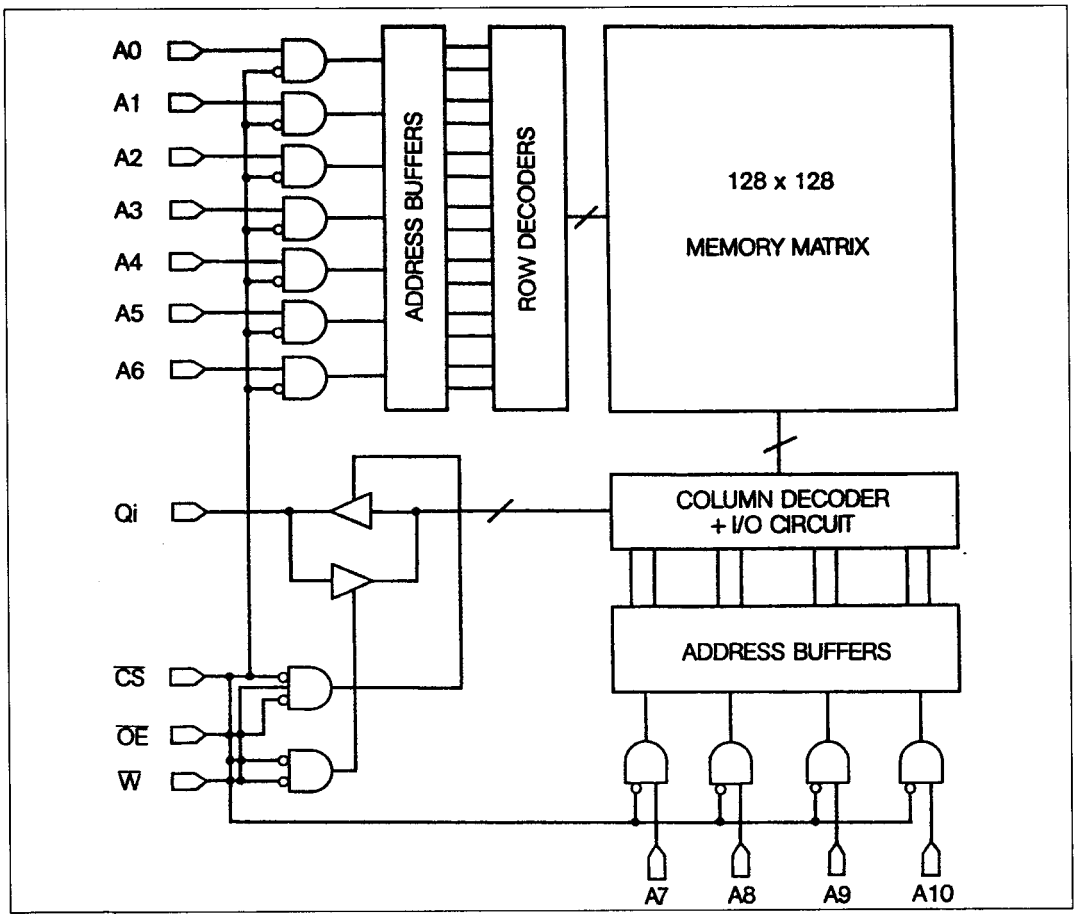
Pinout LCC 32 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A10 : Address inputs	I/O0-I/O7 : Input/Output
Vcc : Power	$\overline{CS}$: Chip Select
$\overline{OE}$: Output enable	$\overline{W}$: Write Enable

TRUTH TABLE

$\overline{CS1}$	$\overline{OE}$	W	DATA-IN	DATA-OUT	MODE
H	X	X	Z	Z	Deselect
L	L	H	Z	Valid	Read
L	H	L	Valid	Z	Write
L	L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.3 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	Vcc ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	Vcc ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	Vcc ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	3.5	V_{CC} + 0.3V	V

Note : 1. VIL min = – 0.3 V or – 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	8	pF
Cout (2)	Output capacitance	–	–	10	pF

Note : 2. TA = 25°C, f = 1 MHz, VCC = 5.0 V, these parameters are not 100 % tested.

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ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	– 1.0*	–	1.0*	µA
IOZ	(3)	Output leakage current	– 1.0*	–	1.0*	µA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc output disabled.
* Specified to ± 2 µA for the HM-65161
4. Vcc min, IOL = 3.2 mA, IOH = – 1.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65161-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	2.0	mA	max
ICCSB1	(6)	Standby supply current	100.0	µA	max
ICC	(7)	Operating supply current	70.0	mA	max
ICCOP	(8)	Operating supply current	70.0	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL		PARAMETER	65161-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	3.0	mA	max
ICCSB1	(6)	Standby supply current	350.0	µA	max
ICC	(7)	Operating supply current	80.0	mA	max
ICCOP	(8)	Operating supply current	80.0	mA	max

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Consumption for Military specification (– 2) :

SYMBOL		PARAMETER	65161-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	4.0	mA	max
ICCSB1	(6)	Standby supply current	1000.0	µA	max
ICC	(7)	Operating supply current	85.0	mA	max
ICCOP	(8)	Operating supply current	85.0	mA	max

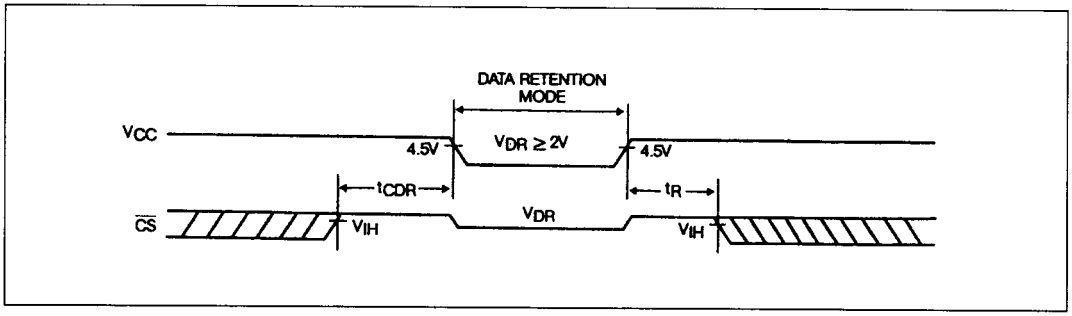
Notes : 5. $\overline{CS} \geq VIH$
6. $\overline{CS} \geq Vcc - 0.3$ V, Iout = 0 mA
7. $CS \leq VIL$, Iout = 0 mA, Vin = Gnd/Vcc
8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation
3. $\overline{CS}$ and $\overline{OE}$ must kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1 (11)	Data retention current @ 2.0 V : HM-65161-5	–	2.0	30.0	µA
	HM-65161-9	–	2.0	140.0	µA
	HM-65161-2	–	2.0	400.0	µA
ICCDR2 (11)	Data retention current @ 3.0 V : HM-65161-5	–	3.0	45.0	µA
	HM-65161-9	–	3.0	210.0	µA
	HM-65161-2	–	3.0	600.0	µA

Notes : 9. TA = 25°C
10. TAVAV = Read cycle time
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

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ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

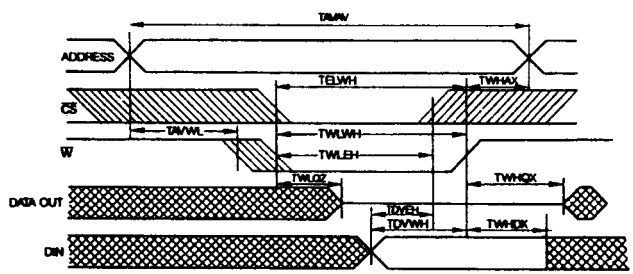
Input pulse levels	: Gnd to 3.0 V	Input timing reference levels	: 1.5 V
Input rise	: 10 ns	Output load	: 1 TTL gate + 100 pF

WRITE CYCLE

SYMBOL	PARAMETER	65161 -5	65161 -9	65161 -2	UNIT	VALUE
TAVAV	Write cycle time	70	80	90	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	65	65	65	ns	min
TDVWH	Data set-up time	30	30	30	ns	min
TELWH	$\overline{CS}$ low to write end	65	65	65	ns	min
TWLQZ (12)	Write low to high Z	35	35	35	ns	max
TWLWH	Write pulse width	65	65	65	ns	min
TWHAX	Address hold to end of write	5	5	5	ns	min
TWHDX	Data hold time	5	5	5	ns	min
TWHQX (12)	Write high to low Z	5	5	5	ns	min

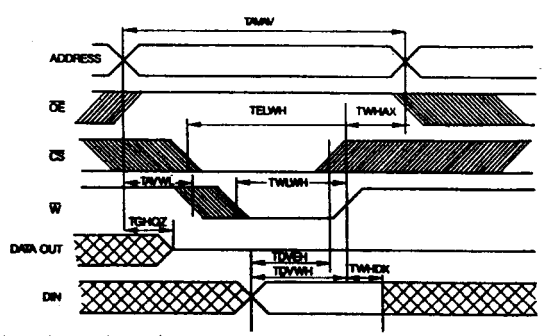
Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

WRITE CYCLE 1



$\overline{OE}$ = VIH during this write cycle.
This write cycle is recommended for continuous writing.

WRITE CYCLE 2

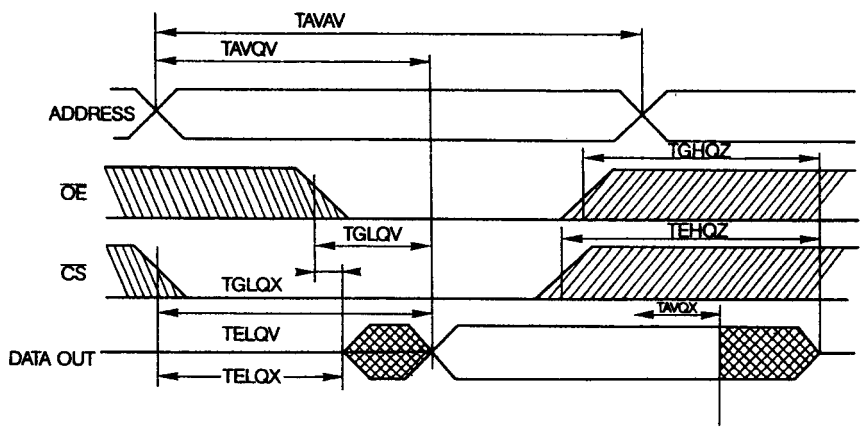


Note : $\overline{OE}$ is low throughout write cycle.
This write cycle time way be used for write and read in the same cycle (write followed by read).

READ CYCLE

SYMBOL	PARAMETER	65161 -5	65161 -9	65161 -2	UNIT	VALUE
TAVAV	READ cycle time	70	80	90	ns	min
TAVQV	Address access time	70	80	90	ns	max
TAVQX	Address valid to low Z	10	10	10	ns	min
TELQV	Chip-select access time	70	80	90	ns	max
TELQX	$\overline{CS}$ low to low Z	10	10	10	ns	min
TEHQZ	$\overline{CS}$ high to high Z	35	35	35	ns	max
TGLQV	Ouptut Enable access time	40	40	60	ns	max
TGLQX	$\overline{OE}$ low to low Z	0	0	0	ns	min
TGHQZ	$\overline{OE}$ high to high Z	35	35	35	ns	max

READ CYCLE



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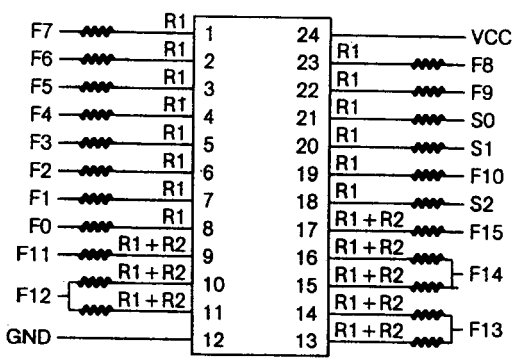
ORDERING INFORMATION

Package	Device type	Level
HM1	65161	– 5
0 - Chip form 1 - Ceramic 24 pins 3 - Plastic 24 pins 4 - LCC 32 pins	2 k x 8 general purpose static RAM	– 5 : Commercial – 5+ : Commercial with B.I. – 9 : Industrial – 9+ : Industrial with B.I. – 2 : Military – 8 : Military with B.I. (B.I. = Burn-in)

BURN-IN SCHEMATICS



R1 = 220 Ω per row
R2 = 2.2 KΩ per driver

Fo = 25 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1, S2 : programmable signals for write / read cycles

VCC = 5.5 V

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