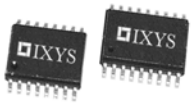
# IXYS

# IX6Q11

## 1 MHz, 300 Volt, 6 Ampere High & Low-side Driver for N-Channel MOSFETs and IGBTs



### Features

- Floating High Side Driver with boot-strap Power supply along with a Low Side Driver.
- Fully operational to 300V*
- ± 50V/ns dV/dt immunity
- Gate drive power supply range: 10 - 35V
- Undervoltage lockout for both output drivers
- Separate Logic power supply range: 3.3V to $V_{CL}$
- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up protected over entire operating range
- High peak output current: 6A
- Matched propagation delay for both outputs
- Low output impedance
- Low power supply current
- Immune to negative voltage transients

### Applications

- Driving MOSFETs and IGBTs in half-bridge circuits
- High voltage, high side and low side drivers
- Motor Controls
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Class D Switching Amplifiers

### General Description

The IX6Q11 Bridge Driver for N-channel MOSFETs and IGBTs with a high side and low side output, whose input signals reference the low side. The High Side driver can control a MOSFET or IGBT connected to a positive bus voltage up to 300V in dynamic conditions. The logic input stages are compatible with TTL or CMOS, have built-in hysteresis and are fully immune to latch up over the entire operating range. The IX6Q11 can withstand dV/dt on the output side up to ± 50V/ns.

### Ordering Information

The IX6Q11 is available in the 14-Pin DIP, the 16-Pin SOIC, and the heat-sinkable 18-Pin SOIC Cooltab™ packages.

| Part Number | Package Type |
|---|---|
| IX6Q11P7 | 14-Pin DIP |
| IX6Q11S3 | 16-Pin SOIC |
| IX6Q11S6 | 18-Pin SOIC |

**Warning: The IX6Q11 is ESD Sensitive**

**Precaution: when performing the High-Voltage tests, adequate safety precautions should be taken!**

* Operational voltage rating of 300V determined in a typical half-bridge circuit configuration (refer to Figure 9). Operational voltage in other circuit configurations may vary

### Figure 1. Typical Circuit Connection

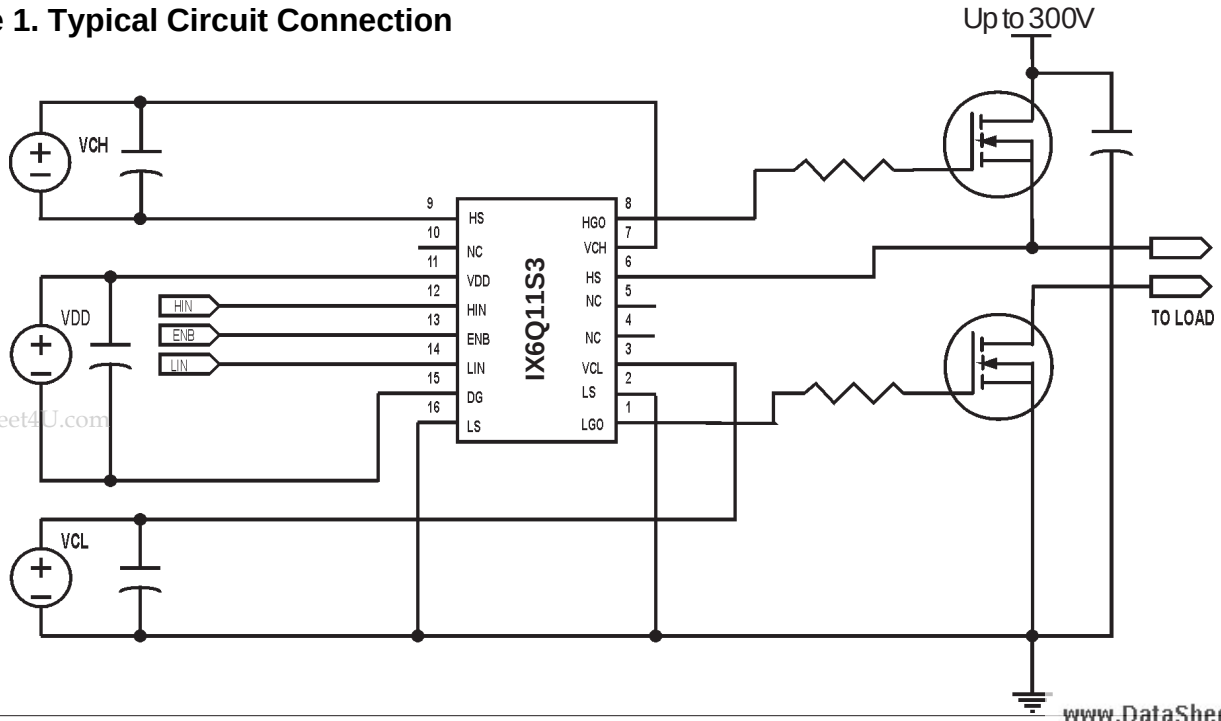
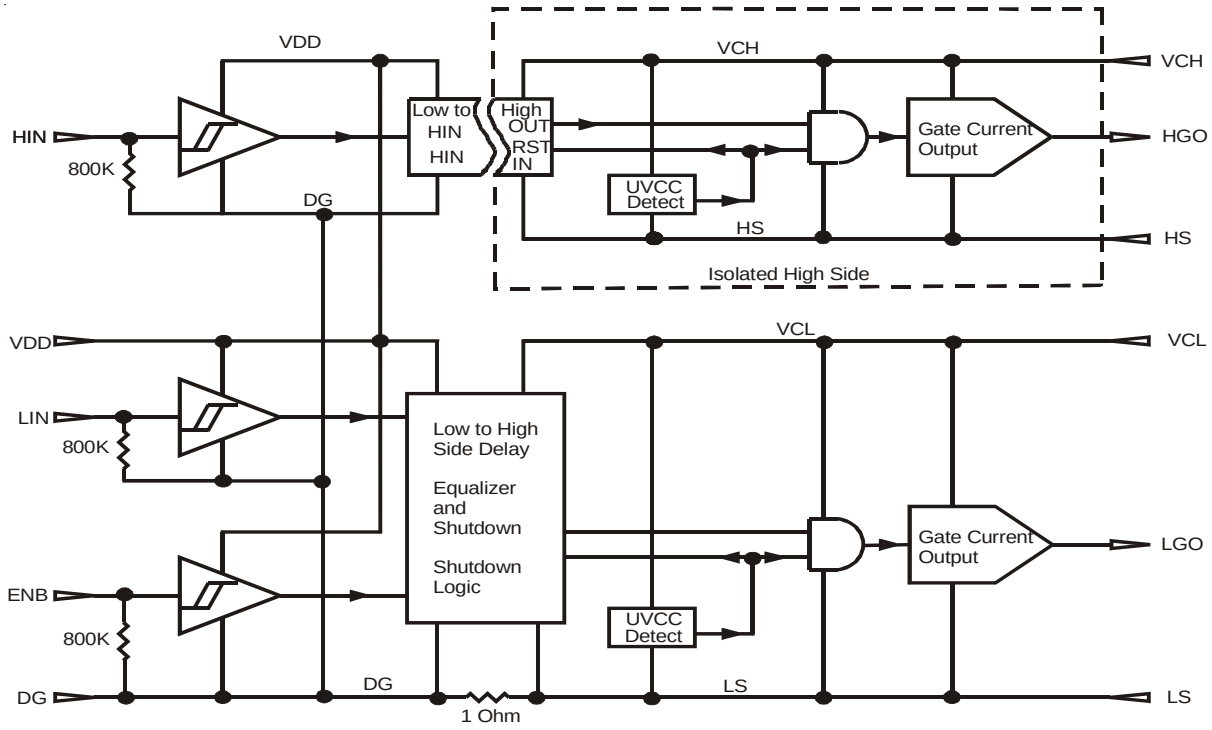
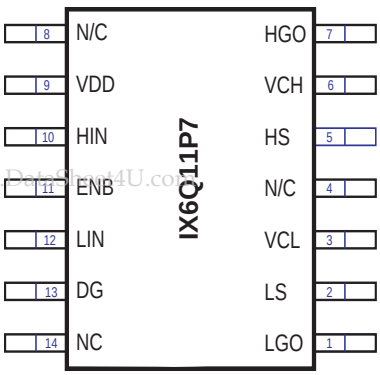


**Figure 2 - IX6Q11 Functional Block Diagram**

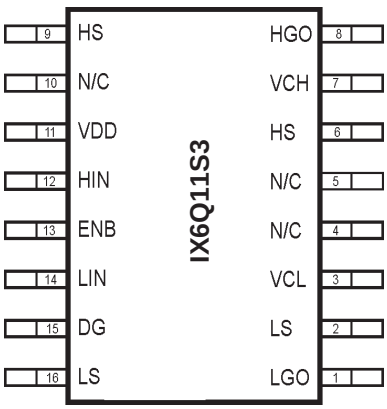



| Pin Description and Configuration | | |
|---|---|---|
| **SYMBOL** | **FUNCTION** | **DESCRIPTION** |
| VDD | Logic Supply | Positive power supply for chip CMOS functions |
| HIN | HS Input | High side input signal, TTL or CMOS compatible; HGO in phase |
| LIN | LS Input | Low side input signal, TTL or CMOS compatible; LGO in phase |
| ENB | Enable | Chip enable, active low. When driven high, both outputs go low |
| DG | Ground | Logic reference ground |
| VCH | Supply Voltage | High side power supply, referenced to HS |
| HGO | Output | High side driver output |
| HS | Return | High side voltage return pin |
| VCL | Supply Voltage | Low side power supply, referenced to LS |
| LGO | Output | Low side driver output |
| LS | Ground | Low side voltage return pin |

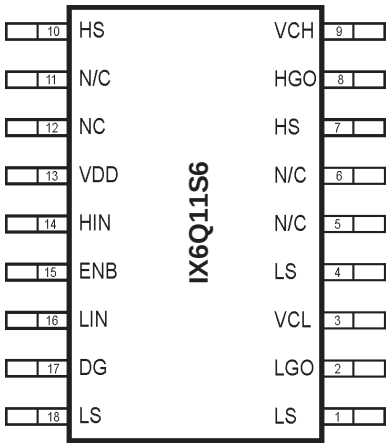
**14-PIN DIP**




**16-PIN SOIC**




**18-PIN SOIC w/Cooltab™**






Cooltab is a trademark of IXYS Corporation

## Absolute Maximum Ratings

| Symbol | Definition | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CH}$ | High side floating supply voltage | | -0.3 | +35 | V |
| $V_{HS}$ | High side floating supply offset voltage | | -200 | +300 | V |
| $V_{HGO}$ | High side floating output voltage | | $V_{HS}$-0.3 | $V_{CH}$+0.3 | V |
| $V_{CL}$ | Low side fixed supply voltage | | -0.3 | 35 | V |
| $V_{LGO}$ | Low side output voltage | | -0.3 | $V_{CL}$+0.3 | V |
| $V_{DD}$ | Logic supply voltage | | -0.3 | $V_{CL}$+0.3 | V |
| $V_{DG}$ | Logic supply offset voltage | | $V_{LS}$-3.8 | $V_{LS}$+3.8 | V |
| $V_{IN}$ | Logic input voltage(HIN & LIN) | | $V_{LS}$-0.3 | $V_{CL}$+0.3 | V |
| $dV_S/dt$ | Allowable offset supply voltage transient | | | 50 | V/ns |
| $P_D$ | Package power dissipation @ $T_A \leq 25C$ | (IX6Q11S3/P7) | | 1.25 | W |
| | | (IX6Q11S6) | | 1.4 | W |
| $P_D$ | Package power dissipation @ $T_C \leq 25C$ | (IX6Q11S3/P7) | | 2.5 | W |
| | | (IX6Q11S6) | | 43 | W |
| $R_{THJA}$ | Thermal resistance, junction-to-ambient | (IX6Q11S3/P7) | | 100 | K/W |
| | | (IX6Q11S6) | | 90 | K/W |
| $R_{THJc}$ | Thermal resistance, junction-to-case | (IX6Q11S3/P7) | | 50 | K/W |
| | | (IX6Q11S6) | | 3 | K/W |
| $T_J$ | Junction Temperature | | | 150 | °C |
| $T_S$ | Storage temperature | | -55 | 150 | °C |
| $T_L$ | Lead temperature (soldering, 10 s) | | | 300 | °C |

## Recommended Operating Conditions

| Symbol | Definition | Min | Max | Units |
|---|---|---|---|---|
| $V_{CH}$ | High side floating supply absolute voltage | $V_{HS}$+10 | $V_{HS}$+20 | V |
| $V_{HS}$ | High side floating supply offset voltage | -20 | +300 | V |
| $V_{HGO}$ | High side floating output voltage | $V_{HS}$ | $V_{CH}$+20 | V |
| $V_{CL}$ | Low side fixed supply voltage | 10 | 20 | V |
| $V_{LGO}$ | Low side output voltage | 0 | $V_{CC}$ | V |
| $V_{DD}$ | Logic supply voltage | $V_{DG}$+3 | $V_{DG}$+$V_{CL}$ | V |
| $V_{DG}$ | Logic supply offset voltage | $V_{LS}$-0.5 | $V_{LS}$+0.5 | V |
| $V_{IN}$ | Logic input voltage(HIN, LIN, ENbar) | $V_{DG}$ | $V_{DD}$ | V |
| $T_A$ | Ambient Temperature | -40 | 125 | °C |

## Dynamic Electrical Characteristics*

$V_{CL}$ = $V_{CH}$ = $V_{DD}$ = +15V, $C_{load}$ = 5nF, and $V_{DG}$ = $V_{LS}$ unless otherwise specified. The dynamic electrical characteristics are measured using Figure 7.

| Symbol | Definition | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{on}$ | Turn-on propagation delay | $V_{HS}$= 0V | | 110 | 130 | ns |
| $t_{off}$ | Turn-off propagation delay | $V_{HS}$= 300V | | 94 | 125 | ns |
| $t_{enb}$ | Device not enable delay | | | 110 | 140 | ns |
| $t_r$ | Turn-on rise time | | | 25 | 35 | ns |
| $t_f$ | Turn-off fall time | | | 17 | 25 | ns |
| $t_{dm}$ | Delay matching, HS & LS turn-on/off | | | 10 | 30 | ns |

## Static Electrical Characteristics

| Symbol | Definition | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{INH}$ | Logic “1” input voltage, HIN, LIN, ENB | $V_{DD}$= $V_{CL}$= 15V | 9.5 | | | V |
| $V_{INL}$ | Logic “0” input voltage, HIN, LIN, ENB | $V_{DD}$= $V_{CL}$= 15V | 0 | | 6 | V |
| $V_{HLGO}$ / $V_{HHGO}$ | High level output voltage, $V_{CH}$-$V_{HGO}$ or $V_{CL}$-$V_{LGO}$ | $I_O$= 0A | | | 0.1 | V |
| $V_{LLGO}$ / $V_{LHGO}$ | Low level output voltage, $V_{HGO}$ or $V_{LGO}$ | $I_O$= 0A | | | 0.1 | V |
| $I_{HL}$ | HS to LS bias current. | $V_{HS}$= $V_{CH}$= 300V | | 170 | | µA |
| $I_{QHS}$ | Quiescent $V_{CH}$ supply current | $V_{IN}$= 0V or $V_{DD}$ = 15V | | 1 | 3 | mA |
| $I_{QLS}$ | Quiescent $V_{CL}$ supply current | $V_{IN}$= 0V or $V_{DD}$ = 15V | | 1 | 3 | mA |
| $I_{QDD}$ | Quiescent $V_{DD}$ supply current | $V_{IN}$= 0V or $V_{DD}$ = 15V | | 15 | 30 | µA |
| $I_{IN}$+ | Logic “1” input bias current | $V_{IN}$= $V_{DD}$ | | 20 | 40 | µA |
| $I_{IN}$- | Logic “0” input voltage | $V_{IN}$= 0V | | | 1 | µA |
| $V_{CHUV}$+ | $V_{CH}$ supply undervoltage positive going threshold. | | 7.5 | 8.6 | 9.7 | V |
| $V_{CHUV}$- | $V_{CH}$ supply undervoltage negative going threshold. | | 7 | 8.2 | 9.4 | V |
| $V_{CLUV}$+ | $V_{CL}$ supply undervoltage positive going threshold | | 7.4 | 8.5 | 9.6 | V |
| $V_{CLUV}$- | $V_{CL}$ supply undervoltage negative going threshold. | | 7 | 8.2 | 9.4 | V |
| $I_{GO}$+ | HS or LS Output high short circuit current; | $V_{GO}$= 15V, $V_{IN}$= 15V, PW<10us | 4 | 6 | | A |
| $I_{GO}$- | HS or LS Output low short circuit current; | $V_{GO}$= 0V, $V_{IN}$=0V, PW<10us | | -7 | -5 | A |



* These characteristics are guaranteed by design only. Tested on a sample basis.

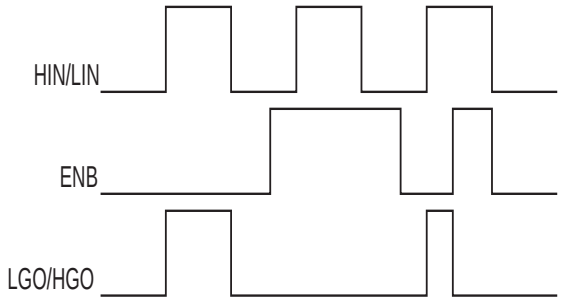



Figure 3. INPUT/OUPUT Timing Diagram

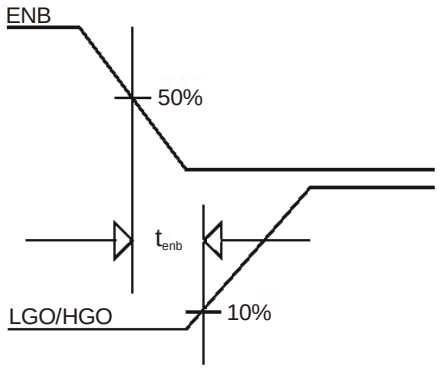



Figure 4. ENABLE Waveform Definitions

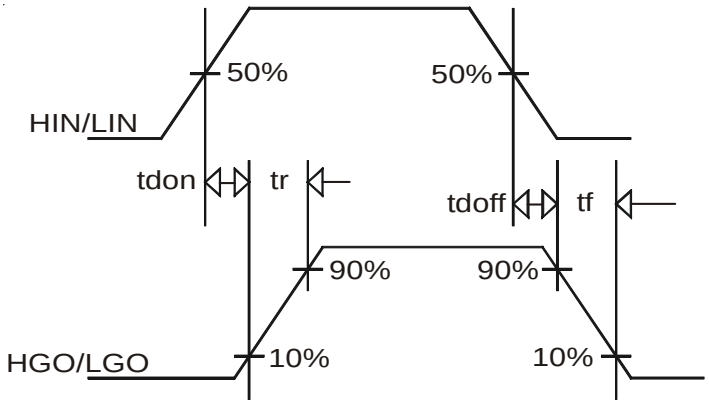



Figure 5. Definitions of Switching Time Waveforms

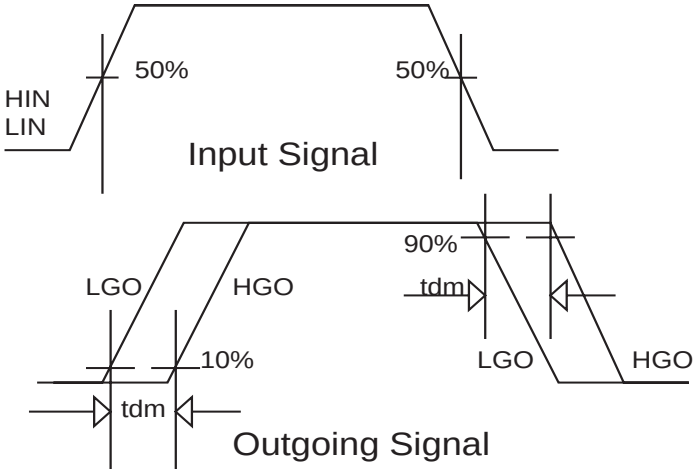



Figure 6. Definitions of Delay Matching Waveforms

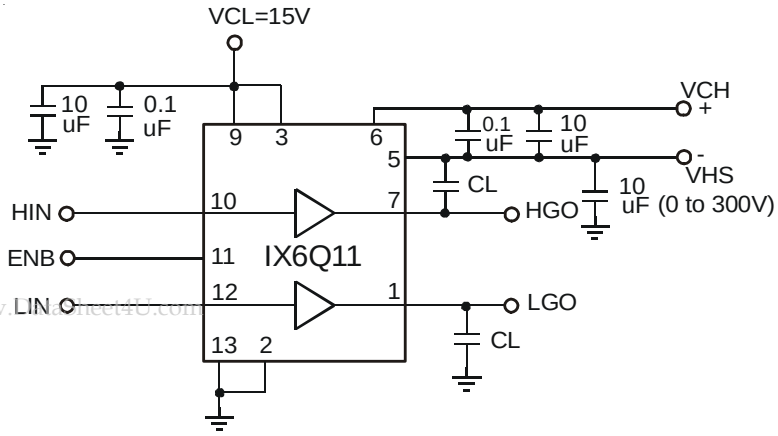





Figure 7. Switching Time Test Circuit

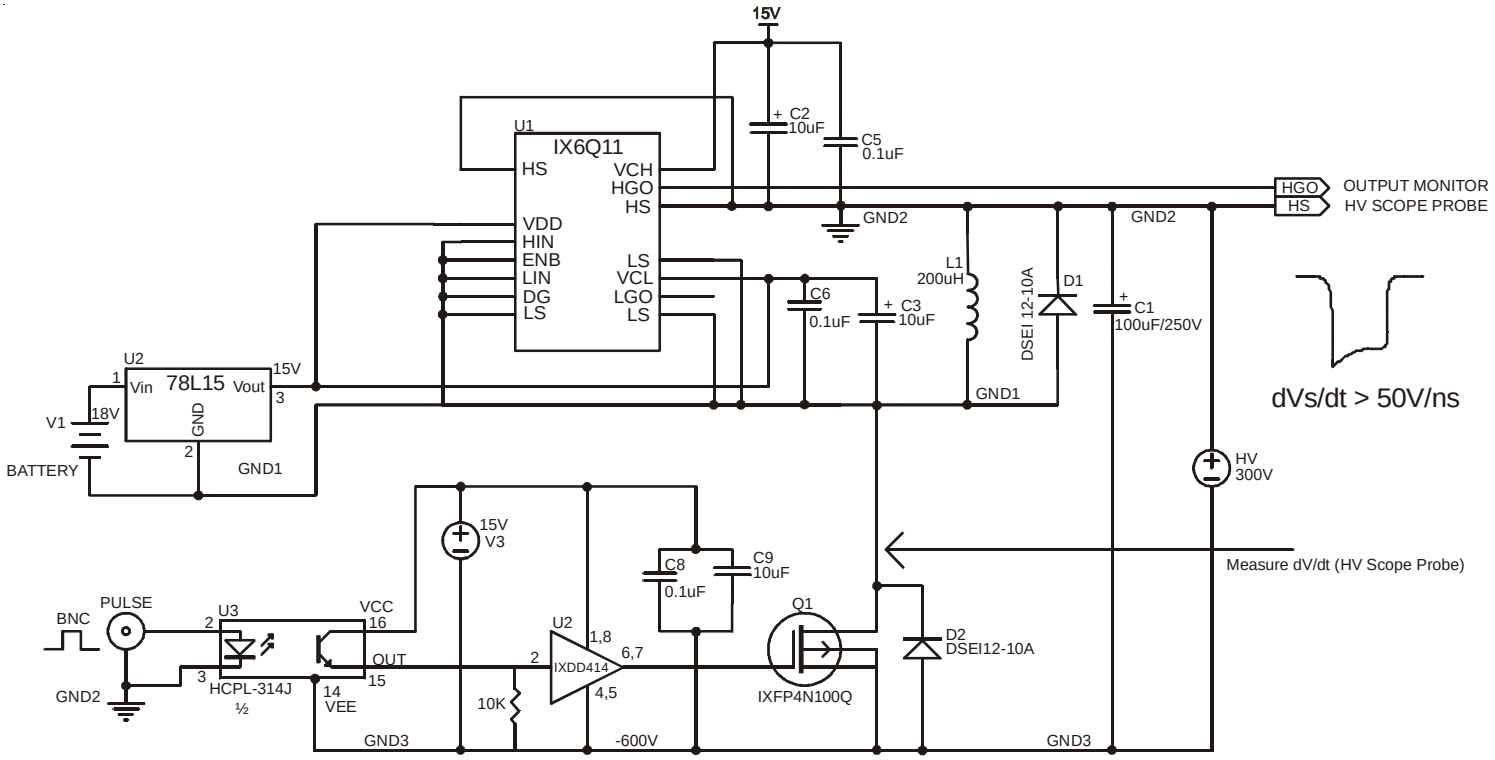



Figure 8. Test circuit for allowable offset supply voltage transient.

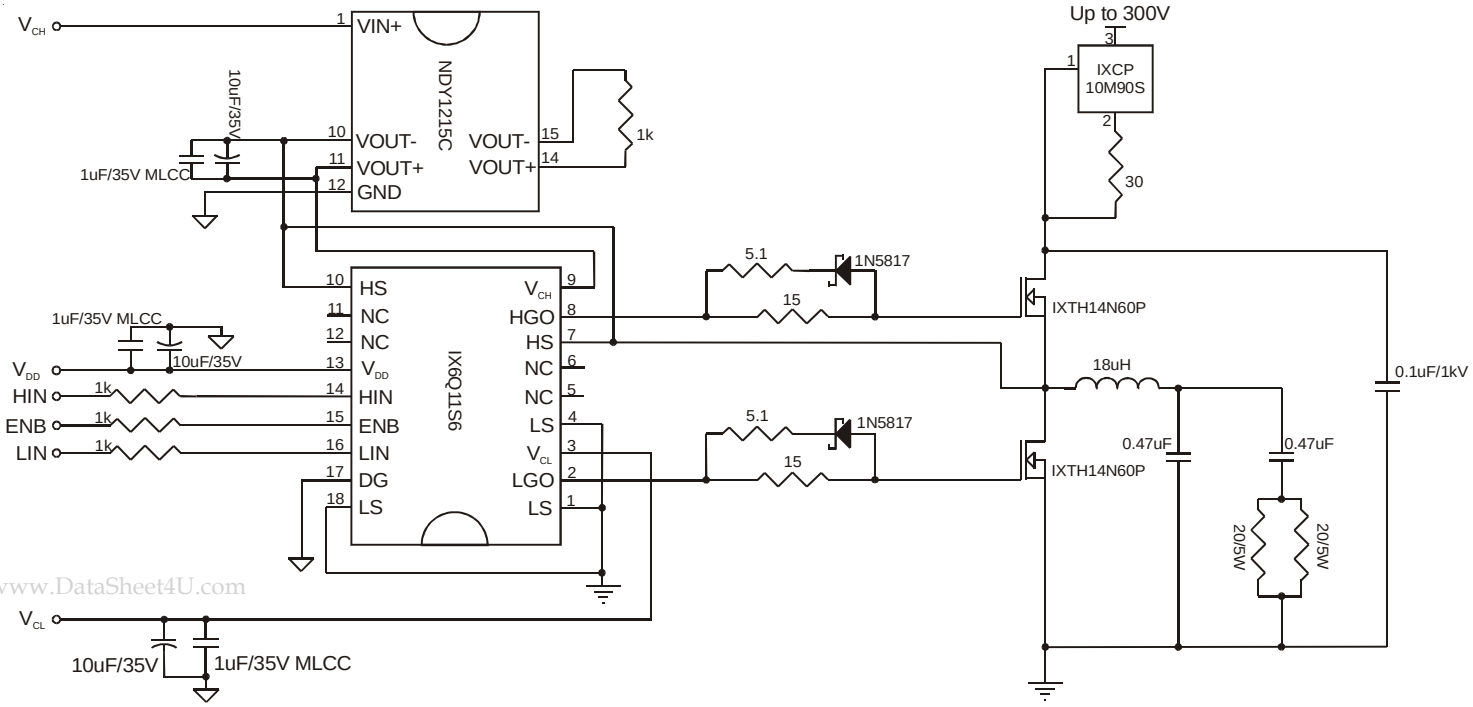



Figure 9. Test circuit for high frequency, 750kHz, operation.
$V_{DD}$, $V_{CH}$, $V_{CL}$ = 15V

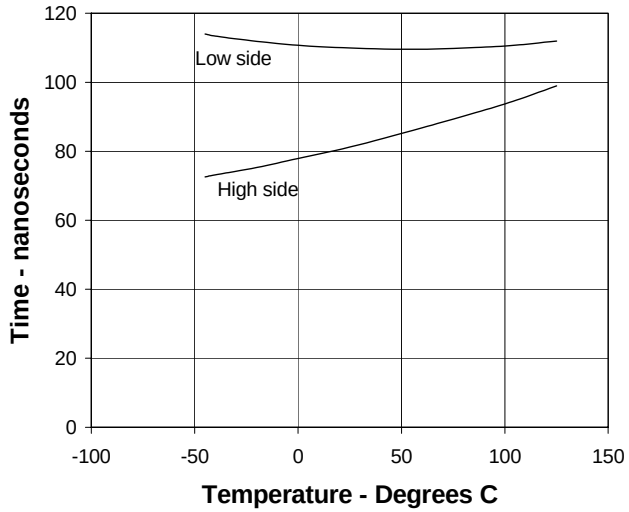



Fig. 10a. High and Low side turn-on delay times

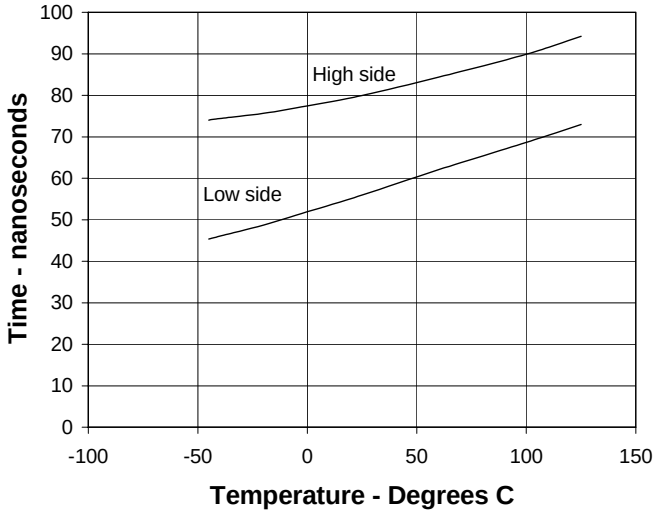



Fig. 10b. High and Low side turn-off delay times

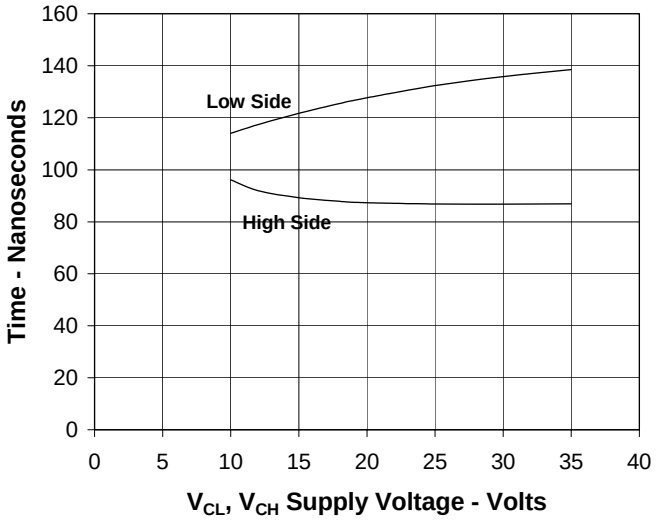



Fig. 11a. High and Low side turn-on delay vs. $V_{CL}$, $V_{CH}$

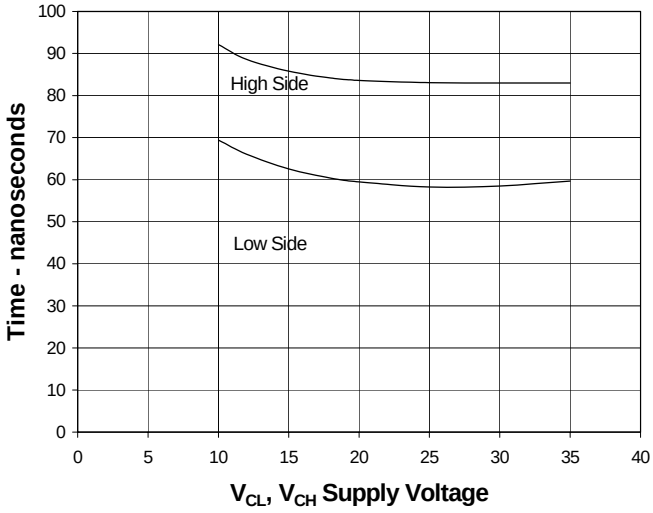



Fig. 11b. High and Low side turn-off delay vs. $V_{CL}$, $V_{CH}$

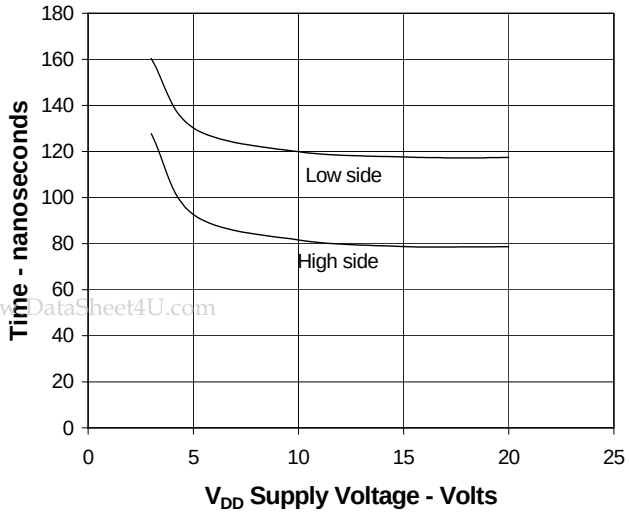





Fig. 12a. High and Low side turn-on delay vs $V_{DD}$

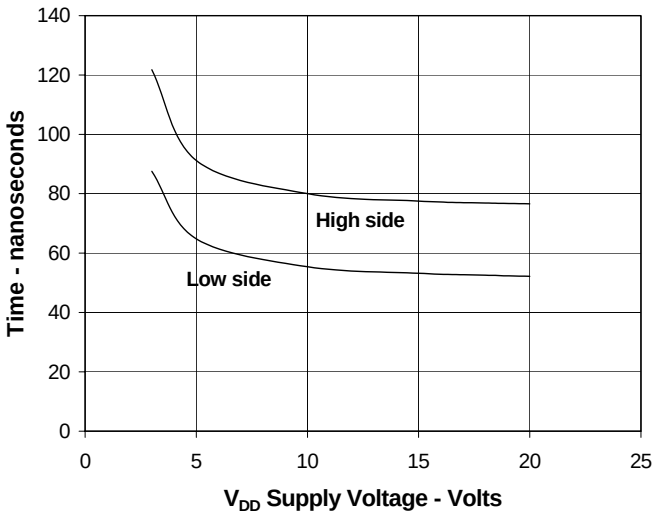



Fig. 12b. High and Low side turn-off delay vs. $V_{DD}$

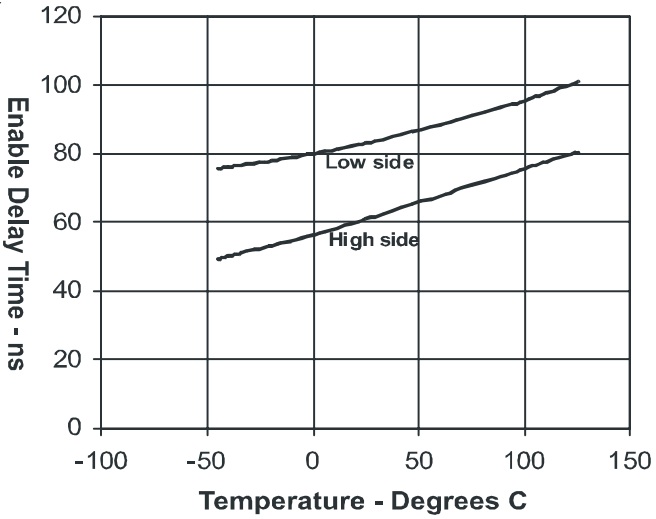



Fig. 13a. High and Low side ENABLE (Shutdown) times vs. temperature.

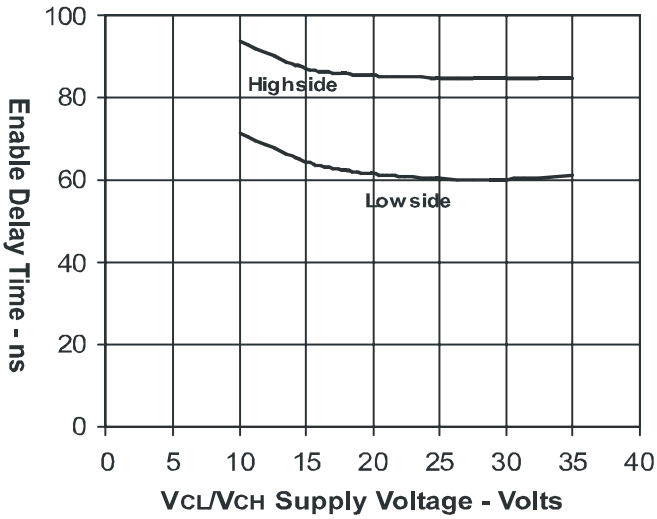



Fig.13b. High and Low side ENABLE (Shutdown) times vs. supply voltage.

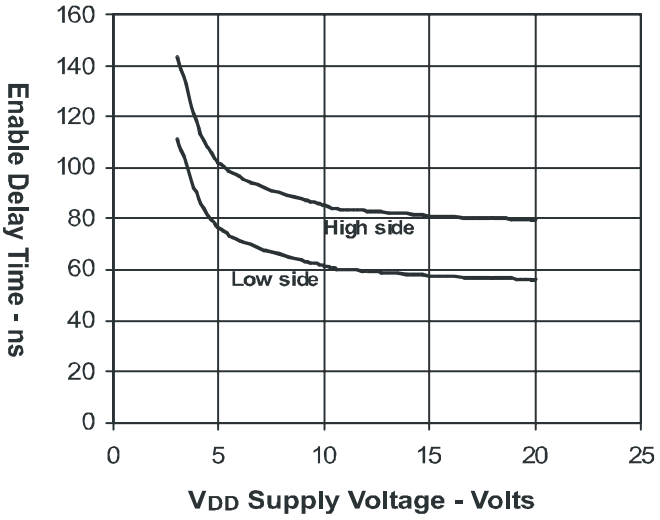



Fig. 13c. High and Low side ENABLE (Shutdown) times versus supply voltage.

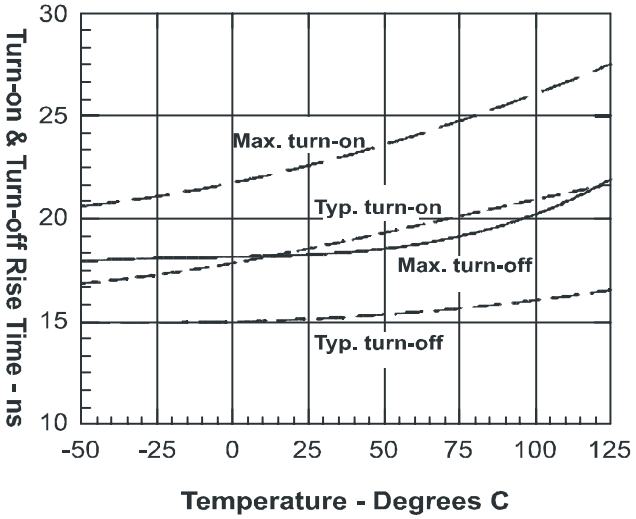



Fig. 14a. Turn-on and turn-off rise times vs. temperature.

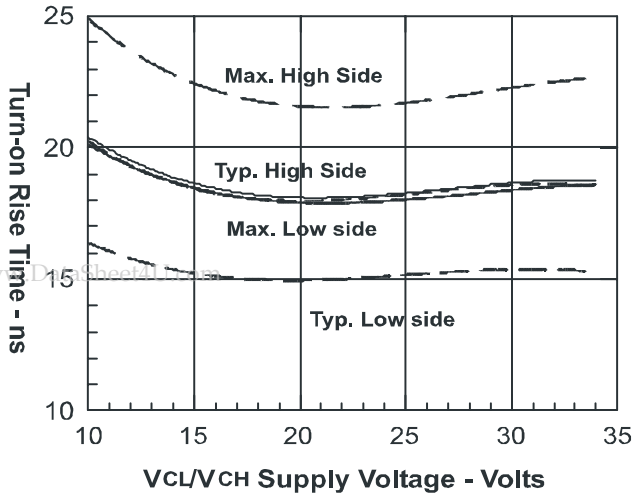



Fig. 14b. Turn-on rise times vs. bias supply voltages

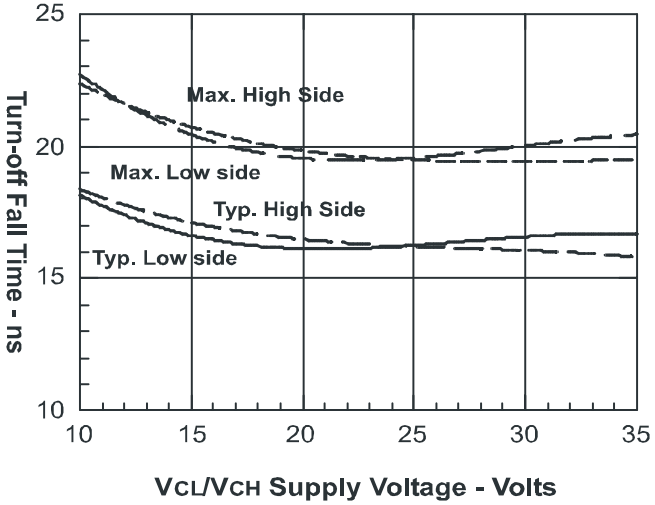



Fig. 14c. Turn-off delay times vs. bias supply voltages.

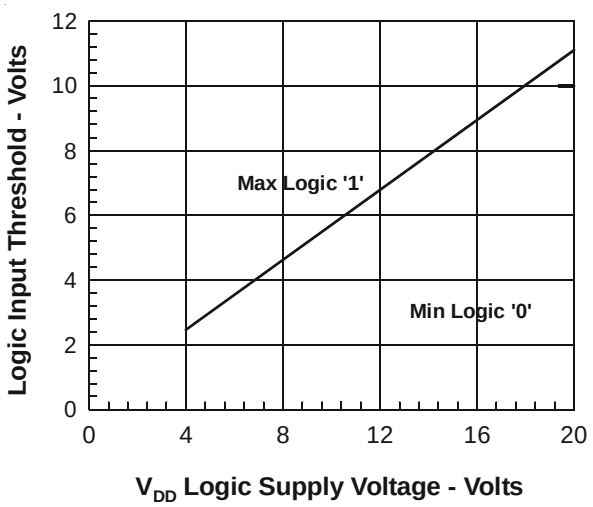



Fig. 15. Logic input threshold voltage vs bias supply voltage.

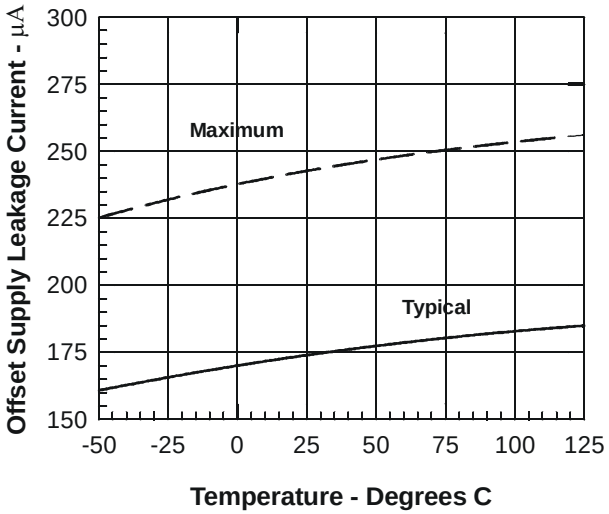



Fig. 16. Offset supply leakage current vs. temperature.

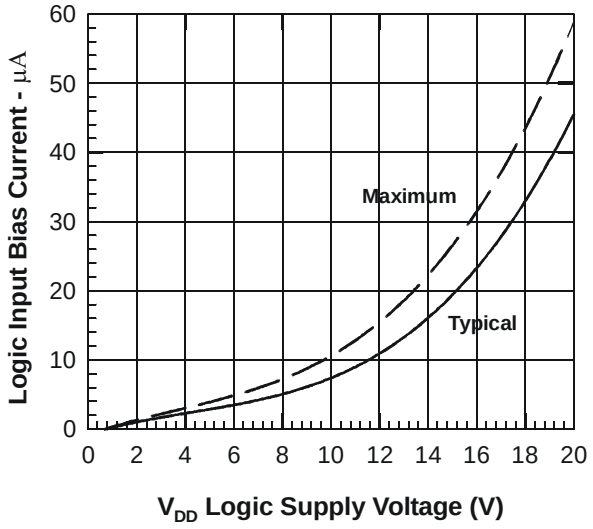



Fig. 17. Logic input current vs. bias voltage.

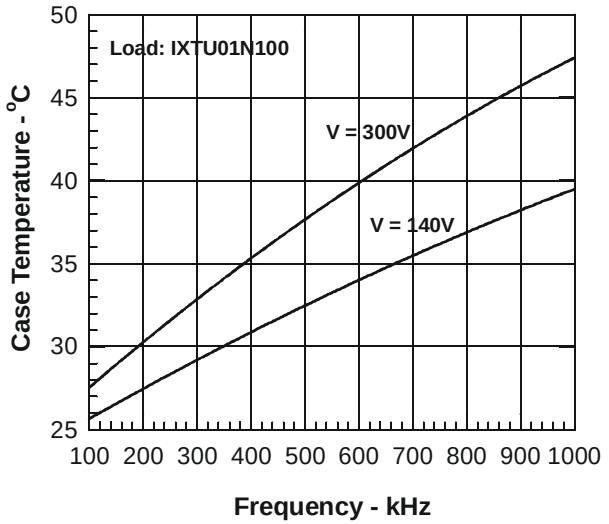



Fig. 18. IX6Q11S3 Case temperature rise vs. operating frequency

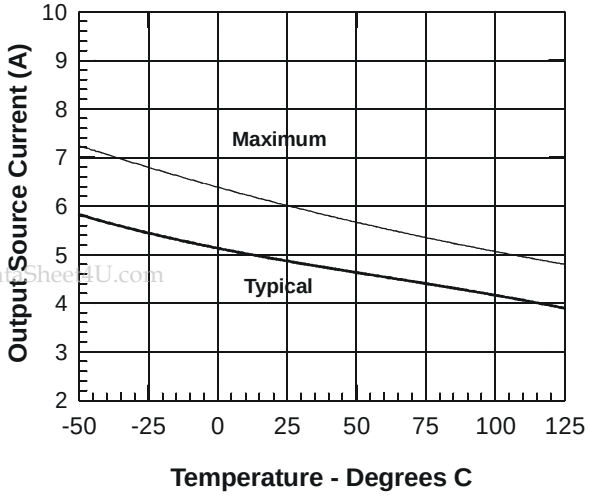



Fig. 19a. Output source current vs. temperature

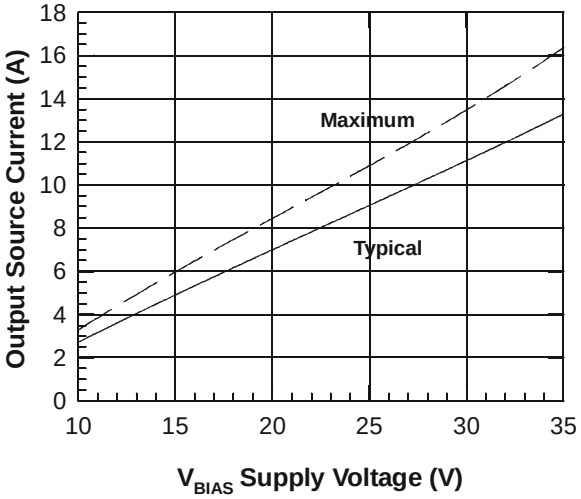



Fig. 19b. Output source current vs supply voltage

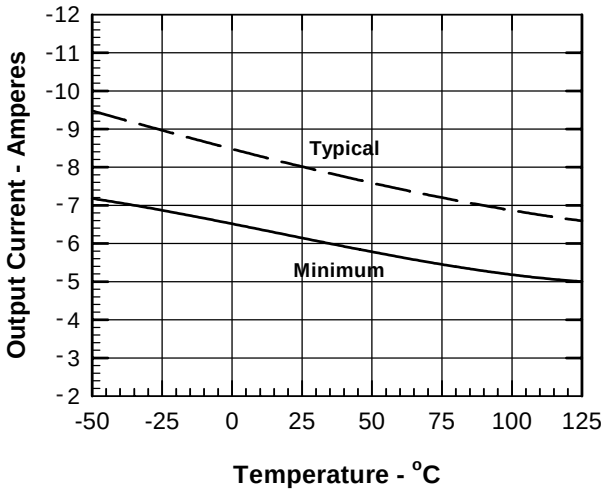



Fig. 20a. Output sink current vs. temperature

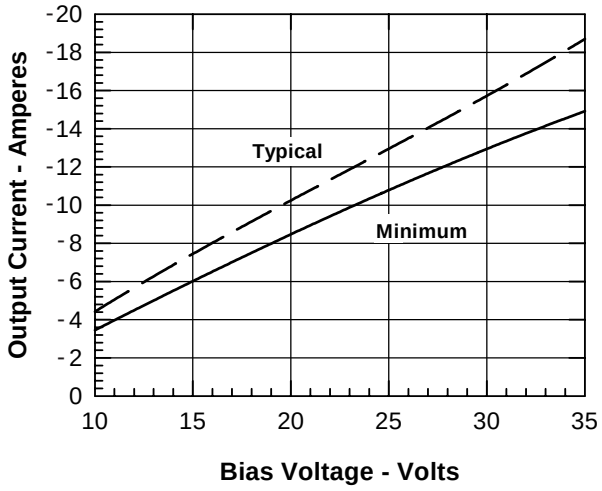



Fig. 20b. Output sink current vs. bias voltage

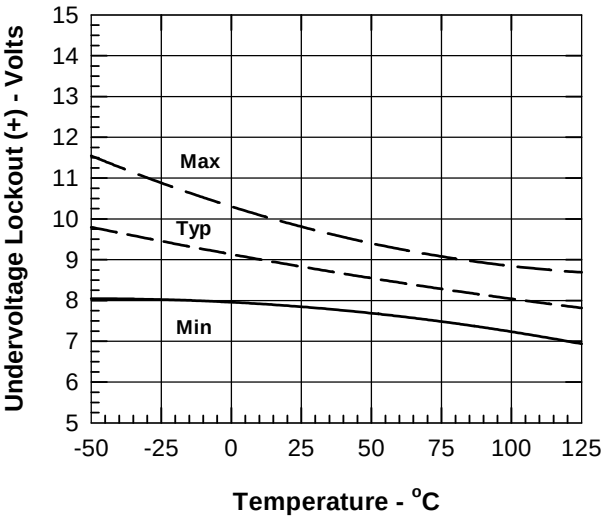



Fig. 21a. $V_{CH}$ Undervoltage positive trip vs. temperature.

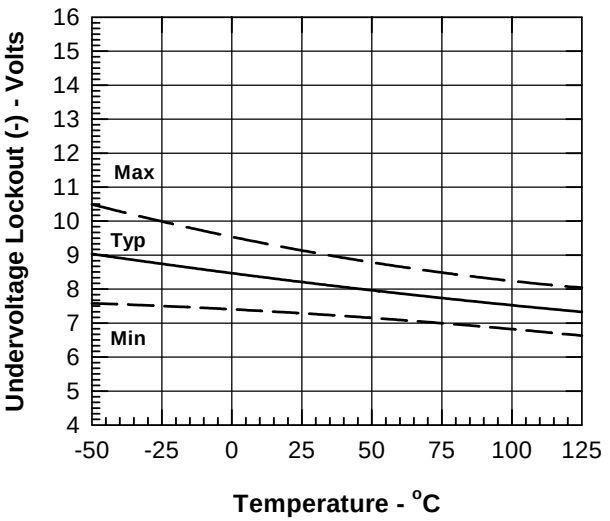



Fig. 21b. $V_{CH}$ Undervoltage negative trip vs. temperature

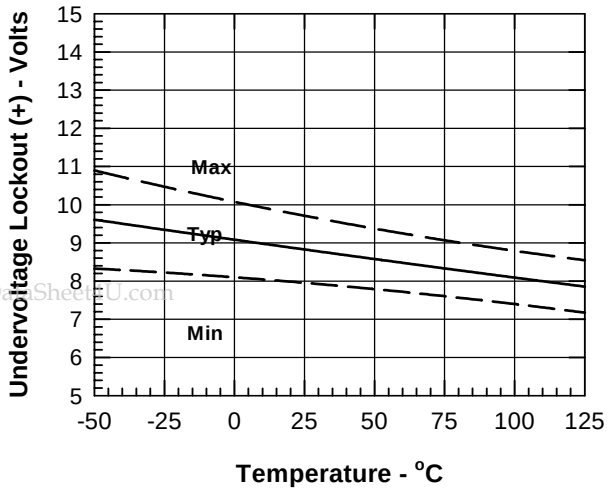





Fig. 22a. $V_{CL}$ Undervoltage positive trip vs. temperature

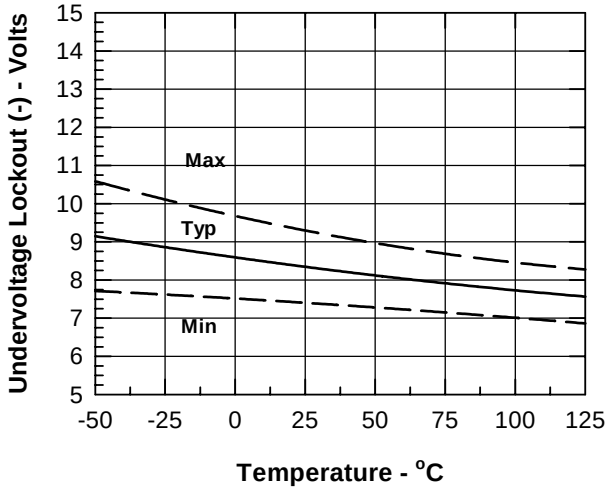



Fig. 22b. $V_{CL}$ Undervoltage negative trip vs. temperature

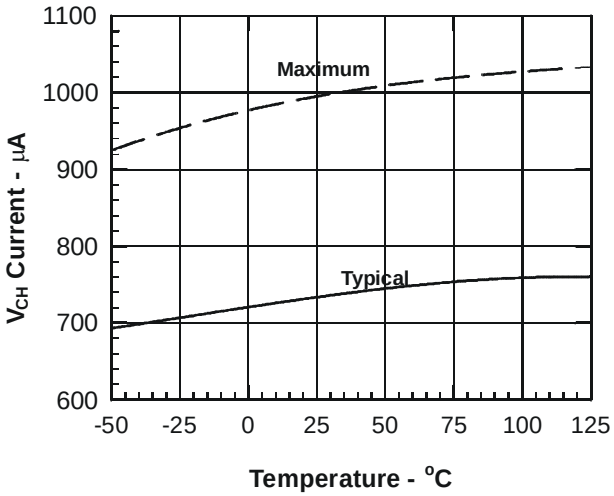



Fig. 23a. Quiescent current vs. temperature for the high side power supply.

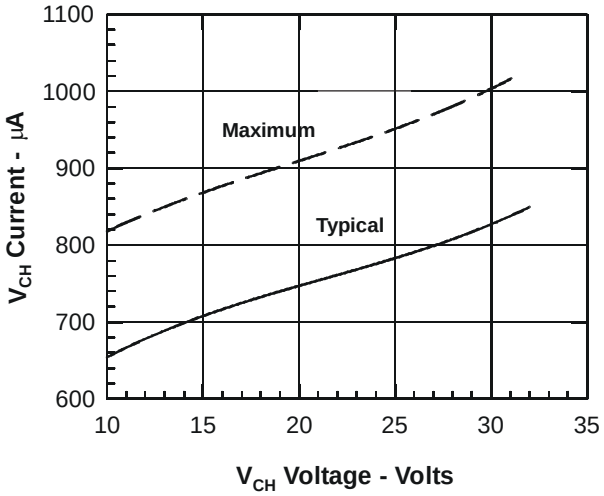



Fig. 23b. Quiescent current vs. voltage for the high side power supply.

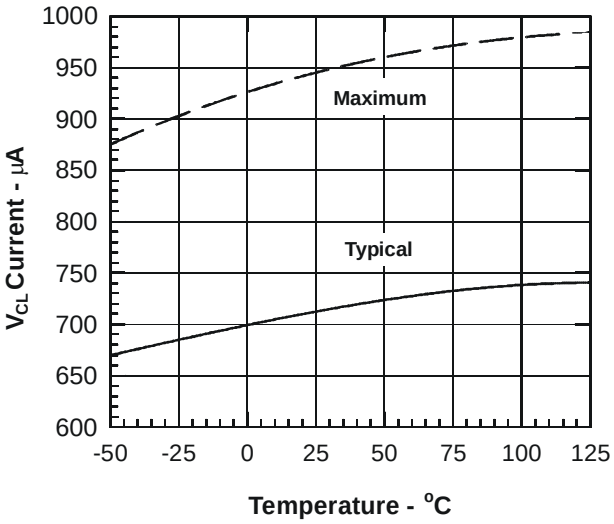



Fig. 24. Quiescent current vs. temperature for the low side power supply

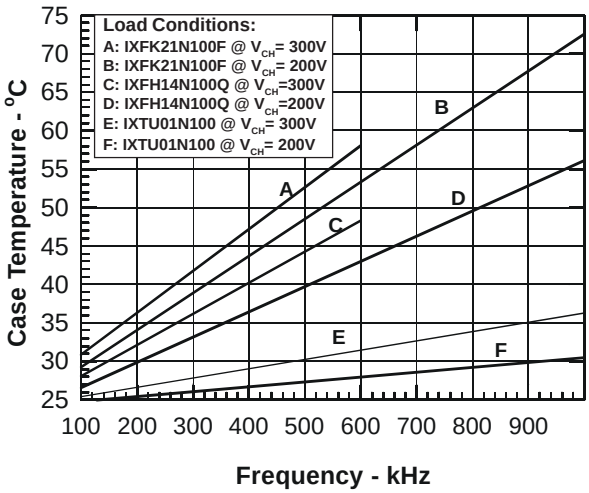



Fig. 25. Case temperature rise vs. switching frequency for IX6Q11S6

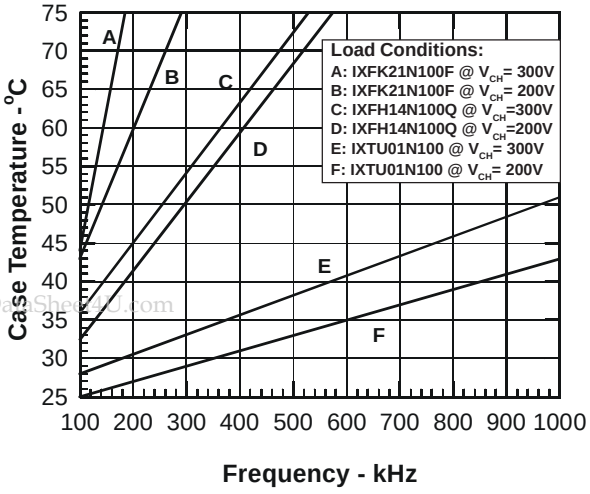
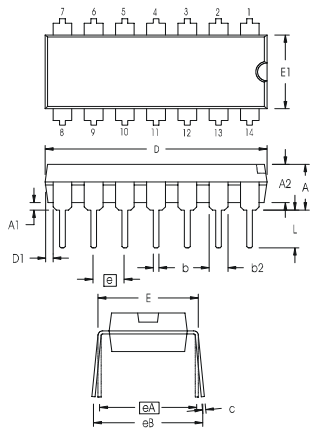



Fig. 26. Case temperature rise vs. switching frequency for IX6Q11S3

| REV | DATE | ECN NO | DESCRIPTION | APPROVAL |
|---|---|---|---|---|
| | | | | |

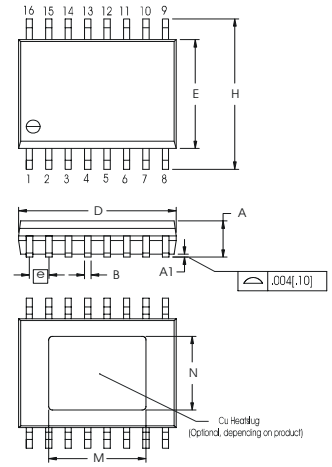



| SYM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .140 | .180 | 3.56 | 4.57 |
| A1 | .015 | .040 | 0.38 | 1.02 |
| A2 | .125 | .145 | 3.18 | 3.68 |
| b | .015 | .020 | 0.38 | 0.51 |
| b2 | .055 | .065 | 1.40 | 1.65 |
| c | .009 | .012 | 0.23 | 0.30 |
| D | .735 | .775 | 18.67 | 19.69 |
| D1 | .005 | .040 | 0.13 | 1.02 |
| E | .300 | .325 | 7.62 | 8.26 |
| E1 | .240 | .270 | 6.10 | 6.86 |
| e | .100 BSC | | 2.54 BSC | |
| eA | .300 BSC | | 7.62 BSC | |
| eB | .300 | .430 | 7.62 | 10.92 |
| L | .120 | .140 | 3.05 | 3.56 |

NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 AA.

| IXYS Corporation | TOLERANCE | DATE: 2/25/99 | DWN: K. R. Choi | TITLE: CASE OUTLINE OF 14 LEAD 0.3"W P-DIP | DRAWING NO: CO 0066 | REV: D |
|---|---|---|---|---|---|---|
| | | UNIT: Inch(mm) | APR: | | | |
| | | SCALE: 4 X | FILE: | | SHEET NO: OF 1 | 1 |

| REV | DATE | ECN NO | DESCRIPTION | APPROVAL |
|---|---|---|---|---|
| A | 11/1/2 | | Added bottom heatslug requirement collar. | K. R. Choi |

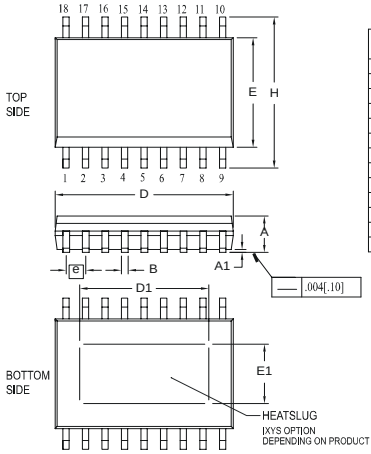



| SYM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .093 | .104 | 2.35 | 2.65 |
| A1 | .004 | .012 | 0.10 | 0.30 |
| B | .013 | .020 | 0.33 | 0.51 |
| C | .009 | .013 | 0.23 | 0.32 |
| D | .398 | .413 | 10.10 | 10.50 |
| E | .291 | .299 | 7.40 | 7.60 |
| e | .050 BSC | | 1.27 BSC | |
| H | .394 | .419 | 10.00 | 10.65 |
| h | .010 | .029 | 0.25 | 0.75 |
| L | .016 | .050 | 0.40 | 1.27 |
| M | .240 | .260 | 6.10 | 6.60 |
| N | .190 | .210 | 4.83 | 5.33 |
| α | 0° | 8° | 0° | 8° |

NOTE: 1. This drawing will meet all dimensions requirement of JEDEC MS-013 AA case outline.
2. Cu heatslug is attached to the die attach pad.

| IXYS Corporation | TOLERANCE | DATE: 12/7/92 | DWN: K. R. Choi | MATERIAL: | TITLE: CASE OUTLINE SOP-16 (.300"W) | DWG NO: CO 0016 | REV: A |
|---|---|---|---|---|---|---|---|
| | | UNIT: Inch (mm) | APR: | | | | |
| | | SCALE: 5X | FILE: | | | SHEET NO: OF 1 | 1 |

| REV | DATE | ECN NO | DESCRIPTION | APPROVAL |
|---|---|---|---|---|
| A | 1/07/02 | | Added bottom side dimensions. | K. R. Choi |




| SYM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .093 | .104 | 2.35 | 2.65 |
| A1 | .004 | .012 | .10 | .30 |
| B | .013 | .020 | .33 | .51 |
| C | .009 | .013 | .23 | .32 |
| D | .447 | .462 | 11.35 | 11.73 |
| D1 | .310 | .350 | 7.87 | 8.89 |
| E | .291 | .299 | 7.40 | 7.60 |
| E1 | .140 | .180 | 3.56 | 4.57 |
| e | .050 BSC | | 1.27 BSC | |
| H | .394 | .419 | 10.00 | 10.65 |
| h | .010 | .029 | .25 | .75 |
| L | .016 | .050 | .40 | 1.27 |
| α | 0° | 8° | 0° | 8° |

NOTE: This drawing will meet all dimensions requirement of JEDEC MS-013 AB.

| IXYS Corporation | TOLERANCE | DATE: 1/04/02 | DWN: K. R. Choi | TITLE: CASE OUTLINE SOIC-18 (MS-013AB) | DRAWING NO: CO 0145 | REV: A |
|---|---|---|---|---|---|---|
| | | UNIT: mm [Inch] | APR: | | | |
| | | SCALE: 5 X | FILE: | | SHEET NO: OF 1 | 1 |