

HD29050

Dual Differential Line Drivers / Receivers With 3 State Outputs

The HD29050 features differential line drivers / receivers with three state output designed to meet the spec of EIA RS – 422A and 423A. Each device has two drivers / receivers in a 16 pin package. The device becomes in enable state when active high for a driver and active low for a receiver.

Features

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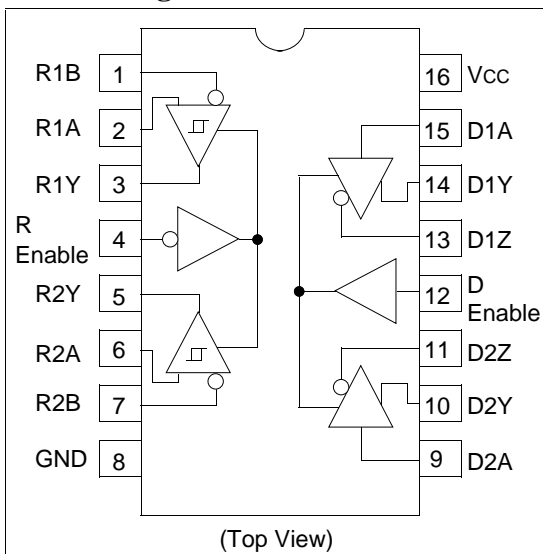
Driver

- Built in current restriction when short circuit
- Power up / down protection.
- High output current $I_{OH} = -40 \text{ mA}$
 $I_{OL} = 40 \text{ mA}$

Receiver

- Input hysteresis (Typ. 50 mV)
- In phase input voltage $\pm 200 \text{ mV}$ of input sensitivity in the range -7 to $+12 \text{ V}$.

Pin Arrangement



Function Table

Drivers			
Input A	Enable	Output Y	Output Z
L	H	L	H
H	H	H	L
X	L	Z	Z

Receivers		
Differential Input A – B	Enable	Output Y
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z

H : High level
 L : Low level
 Z : High impedance
 X : Immaterial
 ? : Irrelevant

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage ^{*1}	VCC	7	V
Input Voltage A , B ^{*3}	VIN	±25	V
Differential Input Voltage ^{*2} ^{*3}	VID	±25	V
Output Current ^{*3}	IO	50	mA
Enable Input Voltage	VIE	5.5	V
Input Voltage ^{*4}	VIN	5.5	V
Output Applied Voltage ^{*4} ^{*5}	VO	-1.0 to 7.0	V
Operating Temperature Range	T _{opr}	0 to 70	°C
Storage Temperature Range	T _{stg}	-65 to 150	°C

Notes: 1. All voltage values except for differential input voltage are with respect to network ground terminal.

2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

3. Only receiver

4. Only driver

5. Z state

6. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.75	5.0	5.25	V
In Phase Input Voltage ^{*1}	VIC	-7.0	—	12	V
Differential Input Voltage ^{*1}	VID	-6.0	—	6.0	V
Enable Input Voltage	VIE	0	—	5.25	V
Input Voltage ^{*2}	VIN	0	—	5.25	V
Operating Temperature	T _{opr}	0	25	70	°C

Notes: 1. Only receiver

2. Only driver

Electrical Characteristics (Ta = 0 to +70°C)

Driver

Item	Symbol	Min	Typ	Max	Unit	Conditions
Input Voltage	V _{IHD}	2.0	—	—	V	
	V _{I LD}	—	—	0.8	V	
Input Clamp Voltage	V _{IKD}	—	—	-1.5	V	V _{CC} = 4.75 V I _I = -18 mA
Output Voltage	V _{OHD}	2.5	—	—	V	V _{CC} = 4.75 V I _{OH} = -20 mA
		2.4	—	—	V	V _{CC} = 4.75 V I _{OH} = -40 mA
	V _{OLD}	—	—	0.45	V	V _{CC} = 4.75 V I _{OL} = 20 mA
		—	—	0.5	V	V _{CC} = 4.75 V I _{OL} = 40 mA
Output Leak Current	I _{OZD}	-100	—	100	μA	V _{CC} = 5.25 V, V _O = 0.5 V Enable = 0.8 V
		-100	—	100	μA	V _{CC} = 5.25 V, V _O = 2.7 V Enable = 0.8 V
	I _{O(Off)}	—	—	-100	μA	V _{CC} = 0 V V _O = -0.25 V
		—	—	100	μA	V _{CC} = 0 V V _O = 6.0 V
Input Current	I _{ID}	—	—	100	μA	V _{CC} = 5.25 V V _I = 5.25 V
	I _{IHD}	—	—	20	μA	V _{CC} = 5.25 V V _I = 2.7 V
	I _{IHD}	—	—	-360	μA	V _{CC} = 5.25 V V _I = 0.4 V
Differential Output Voltage	Δ V _{OC}	—	—	0.4	V	
	V _{OD2}	2.0	—	—	V	
	Δ V _{OD}	—	—	0.4	V	
Short Circuit Output Current ^{*1}	I _{OSD}	-30	—	-150	mA	V _{CC} = 5.25 V V _O = 0 V

Electrical Characteristics (Ta = 0 to +70°C)

Receiver

Item	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input Threshold Voltage ^{*2}	V _{THR}	—	—	0.2	V	V _O ≥ 2.7 V -7.0 V < V _{IC} < 12 V
		-0.2	—	—	V	V _O ≤ 0.45 V -7.0 V < V _{IC} < 12 V
Input Current	I _{IBR}	—	—	1.0	mA	V _{IN} = 12 V 0 V ≤ V _{CC} ≤ 5.25 V
		—	—	-0.8	mA	V _{IN} = -7 V 0 V ≤ V _{CC} ≤ 5.25 V
Output Voltage	V _{OHR}	2.7	—	—	V	V _{CC} = 4.75 V, I _O = -400 μA V _{ID} = 0.4 V, -7.0 V < V _{ICM} < 12 V
	V _{OLR}	—	—	0.45	V	V _{CC} = 4.75 V, I _O = 8.0 mA V _{ID} = -0.4 V, -7.0 V < V _{ICM} < 2 V
Output Leak Current	I _{OZR}	-100	—	100	μA	V _{CC} = 5.25 V, V _O = 0.4 V V _{ID} = 3.0 V, Enable = 2.0 V
		-100	—	100	μA	V _{CC} = 5.25 V, V _O = 2.4 V V _{ID} = -3.0 V, Enable = 2.0 V
Short Circuit Output Current ^{*1}	I _{OSR}	-15	—	-85	mA	V _{CC} = 5.25 V, V _O = 0 V V _{ID} = 3.0 V
Input Voltage	V _{IHE}	2.0	—	—	V	
	V _{ILE}	—	—	0.8	V	
Input Current	I _{ILE}	—	—	-100	μA	V _{CC} = 5.25 V, V _{IL} = 0.4 V
	I _{IHE}	—	—	20	μA	V _{CC} = 5.25 V, V _{IH} = 2.7 V
	I _{IE}	—	—	100	μA	V _{CC} = 5.25 V, V _{IH} = 5.25 V
Input Clamp Voltage	V _{IKL}	—	—	-1.5	V	V _{CC} = 4.75 I _I = -18 mA

Supply

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply Current	I _{CC}	—	55 ^{*3}	80	mA	V _{CC} = 5.25 V

Notes: 1. Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

2. In this table, only the threshold voltage is expressed in algebra.

3. All typical values are at V_{CC} = 5 V, Ta = 25°C.

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Switching Characteristics (Ta = 25°C, Vcc = 5 V)

Driver

Item	Symbol	Min	Typ	Max	Unit	Conditions
Propagation Delay Time	tPLHD	—	—	20	ns	CL = 30 pF, RL = 75 Ω to GND RL = 180 Ω to Vcc
	tPHLD	—	—	20	ns	CL = 30 pF, RL = 75 Ω to GND RL = 180 Ω to Vcc
Propagation Delay Time Difference	tSKD ^{*1}	—	—	4	ns	CL = 30 pF, RL = 75 Ω to GND RL = 180 Ω to Vcc
Output Enable Time	tzHD	—	—	20	ns	CL = 30 pF RL = 75 Ω to GND
	tzLD	—	—	35	ns	CL = 30 pF RL = 180 Ω to Vcc
Output Disable Time	thZD	—	—	20	ns	CL = 10 pF RL = 75 Ω to GND
	tlZD	—	—	25	ns	CL = 10 pF

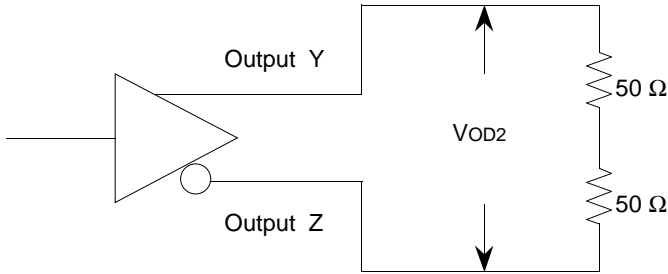
Receiver

Item	Symbol	Min	Typ	Max	Unit	Conditions
Propagation Delay Time	tPLHR	—	—	40	ns	CL = 15 pF
	tPHLR	—	—	40	ns	CL = 15 pF
Output Enable Time	tzHR	—	—	20	ns	CL = 15 pF RL = 5 KΩ to GND
	tzLR	—	—	25	ns	CL = 15 pF RL = 2 KΩ to Vcc
Output Disable Time	thZR	—	—	30	ns	CL = 15 pF, RL = 5 KΩ to GND RL = 2 KΩ to Vcc
	tlZR	—	—	30	ns	

Note: 1. tSKD = |tPLHD - tPHLD|

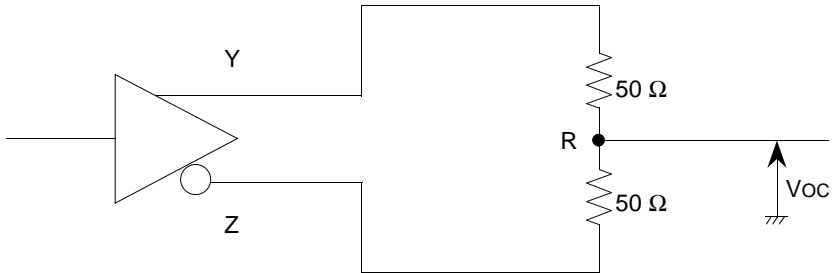
DC Test ($|V_{OD2}|$, $\Delta |V_{OD}|$, V_{OC} , $\Delta |V_{OC}|$)

$|V_{OD2}|$, $\Delta |V_{OD}|$ Test



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V_{OC} , $\Delta |V_{OC}|$ Test



$\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ indicate the differences of voltage from the former states when Y and Z outputs are inverted.

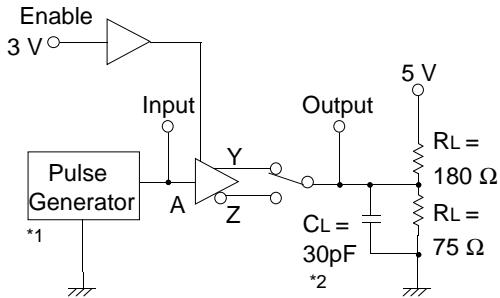
$$\Delta |V_{OD}| = ||V_{OD2}| - \overline{|V_{OD2}}||$$

$$\Delta |V_{OC}| = |V_{OC} - \overline{V_{OC}}|$$

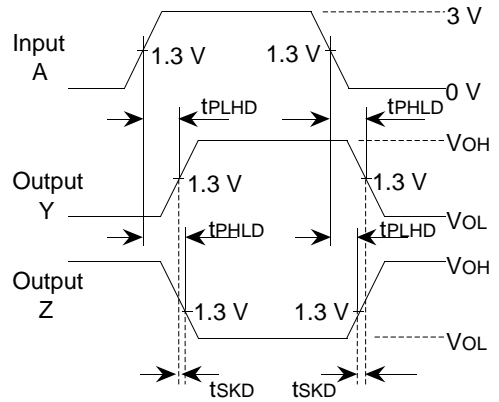
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1. tPLHD, tPHLD

Test circuit

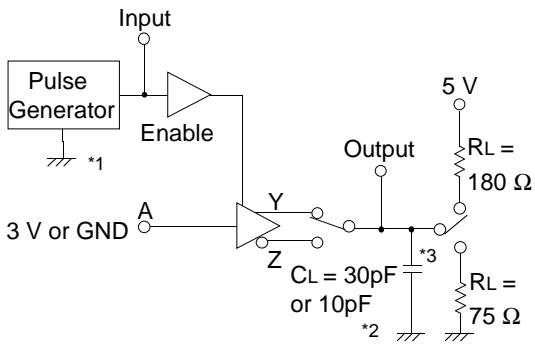


Waveforms

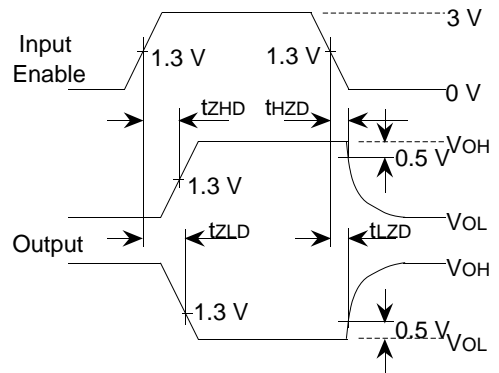


2. tzHD, tzLD, thZD, tlZD

Test circuit

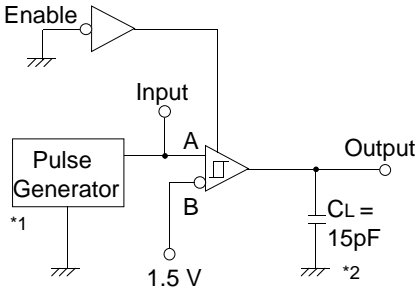


Waveforms

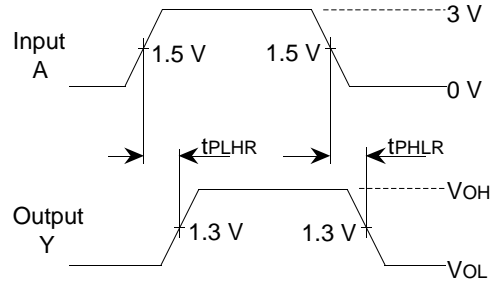


3. tPLHR, tPHLR

Test circuit



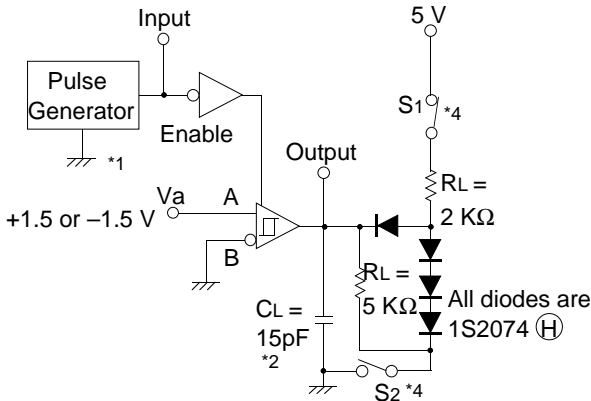
Waveforms



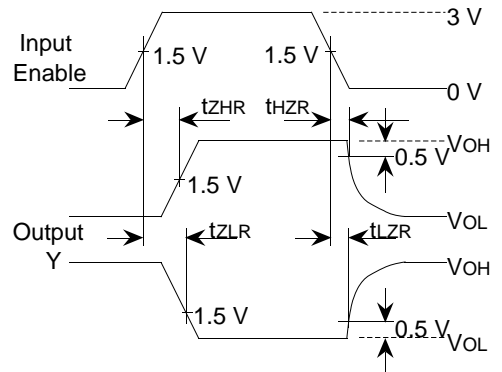
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4. tZHR, tZLR, tHZR, tLZR

Test circuit



Waveforms

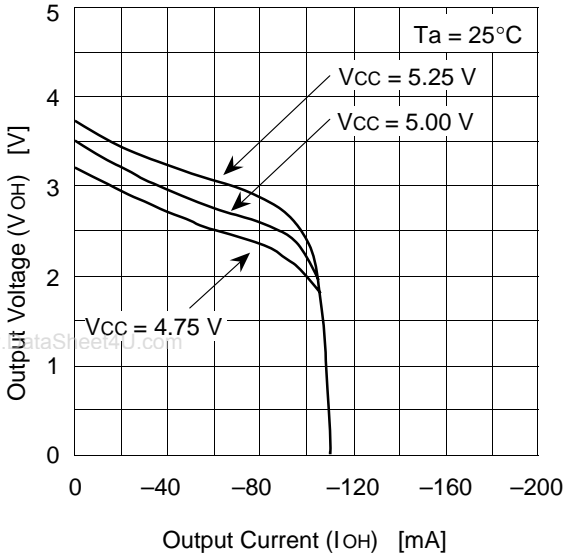


- Notes:
- The pulse generator has the following characteristics:
 PRR = 1 MHz, 50 % duty cycle, $t_r = t_f = 6.0$ ns.
 - CL includes probe and jig capacitance.
 - 75 Ω connected between the pin and GND at tZHD tHZD test.
 180 Ω connected between the pin and GND at tZHD tHZD test.
 - At tHZR, tLZR test, S1 and S2 are closed.
 At tZHR test, S1 is open and S2 is closed.
 At tZLR test, S1 is closed and S2 is open.

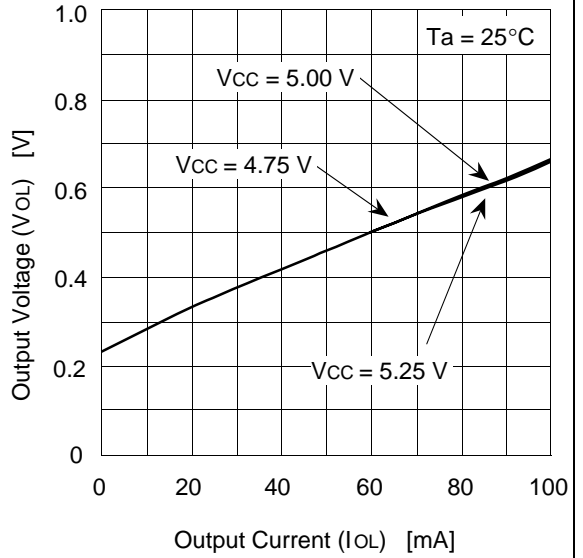
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Main Characteristics

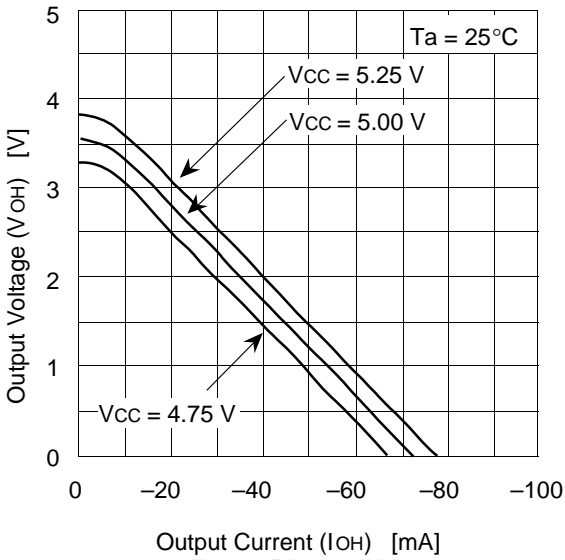
• Output Characteristics (High level)
[Driver]



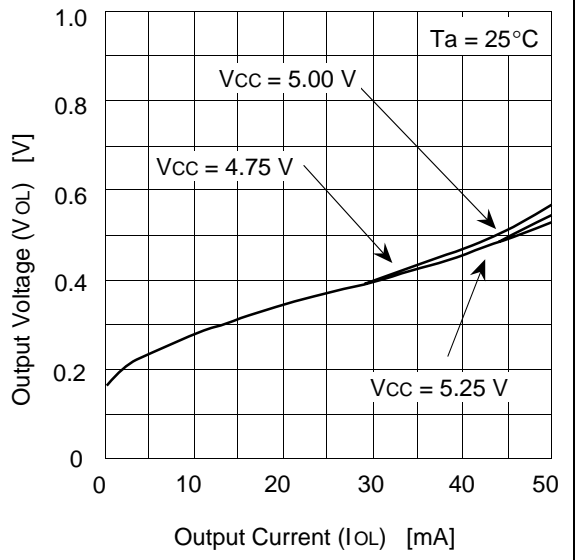
• Output Characteristics (Low level)
[Driver]



• Output Characteristics (High level)
[Receiver]

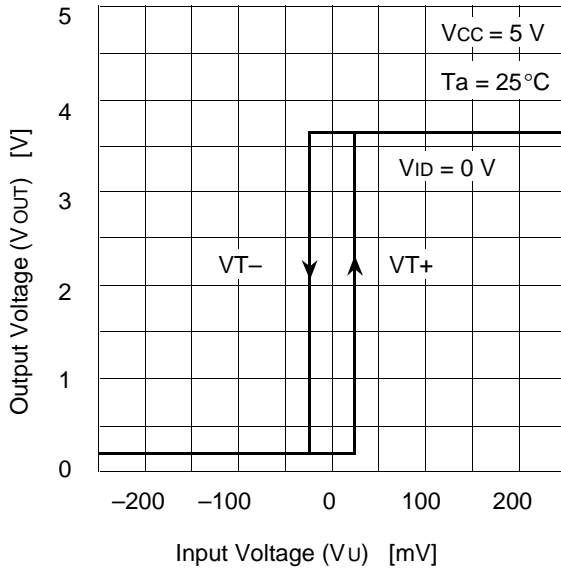


• Output Characteristics (Low level)
[Receiver]



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• Input / Output Characteristics
[Receiver]



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