FLASH-ROM MODULE 8MByte (8M x 8-Bit) , SMM 80Pin
Part No. HMF8M8F4VS

GENERAL DESCRIPTION

The HMF8M8F4VS is a high-speed flash read only memory (FROM) module containing 8,388,608 bytes organized in an x8bit configuration. The module consists of four 2M x 8 FROM mounted on a 80-pin, SMM connector FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.
Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.
Output enable (/OE) and write enable (/WE) can set the memory input and output. The host system can detect a program or erase operation is complete by observing the Ready Pin, or reading the DQ7(Data # Polling) and DQ6(Toggle) status bits.
When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +3V DC power supply and all inputs and outputs are LVTTL-compatible.

FEATURES

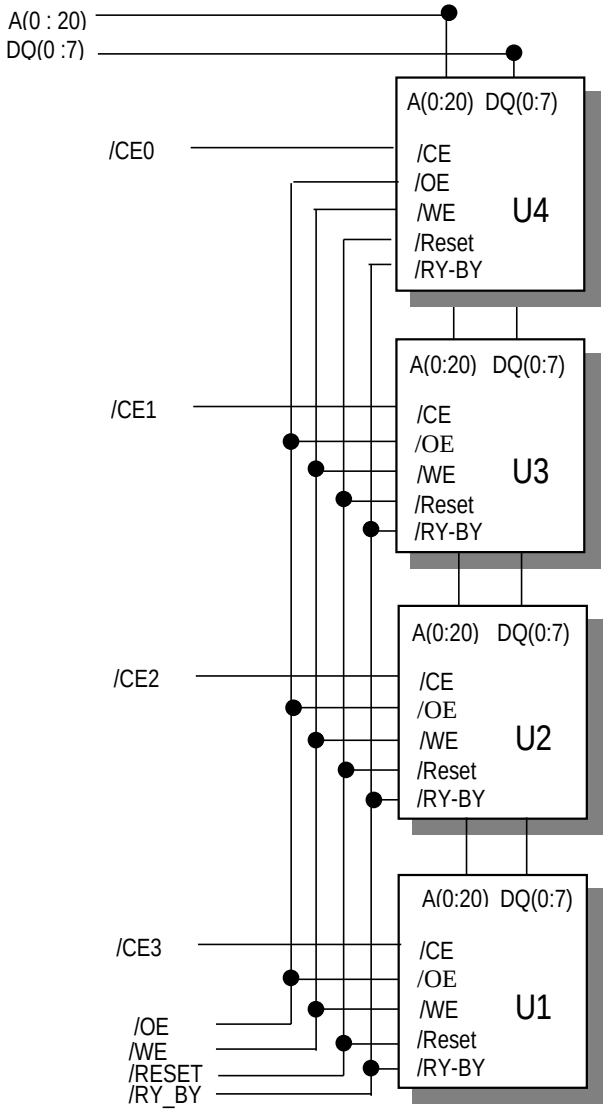
- Part identification
  HMF8M8F4VS(Bottom boot block configuration)
- Access time: 90, 100, 120ns
- High-density 8MByte design
- High-reliability, low-power design
- Single + 3V to 3.6V power supply
- 80-Pin Designed
  40-Pin, 0.8mm Fine Pitch Connector P1,P2
- Minimum 100,000 write cycle guarantee
  per sector
- 10-year data retention at 85 ^{O}C
- Flexible sector architecture
- Embedded algorithms
- Erase suspend / Erase resume

OPTIONS	MARKING
Timing	
90ns access	- 90
100ns access	-100
120ns access	-120
Packages	
SMM 80-pin	F

PIN ASSIGNMENT

P1				P2			
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vcc	21	Vcc	1	Vcc	21	Vcc
2	A20	22	NC	2	/CE1	22	NC
3	NC	23	DQ7	3	/CE2	23	NC
4	NC	24	NC	4	/CE3	24	NC
5	NC	25	DQ6	5	NC(/CE4)	25	/OE
6	/RY_BY	26	NC	6	NC(/CE5)	26	/CE0
7	Vss	27	Vss	7	Vss	27	Vss
8	/RESET	28	DQ5	8	NC(/CE6)	28	A16
9	/WE	29	NC	9	NC(/CE7)	29	A0
10	A19	30	DQ4	10	NC	30	A18
11	A8	31	NC	11	NC	31	A17
12	A9	32	DQ3	12	NC	32	A7
13	A10	33	NC	13	NC	33	A6
14	Vss	34	Vss	14	Vss	34	Vss
15	A11	35	DQ2	15	NC	35	A5
16	A12	36	NC	16	NC	36	A4
17	A13	37	DQ1	17	NC	37	A3
18	A14	38	NC	18	NC	38	A2
19	A15	39	DQ0	19	NC	39	A1
20	Vcc	40	Vcc	20	Vcc	40	Vcc

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION	PIN	FUNCTION
A0 – A20	Address Inputs	/BYTE	Word / Byte selection
DQ0 – DQ31	Data Input/Output	Vcc	Power (+3V)
/CE0-/CE3	Chip Enable	Vss	Ground
/OE	Output Enable	/RY_BY	Ready/Busy output
/WE	Read/Write Enable	NC	No Connection
/RESET	Hardware Reset Pin		

TRUTH TABLE

MODE	/CS	/OE	/WE	RESET	DQ
STANDBY	Vcc±0.3V	X	X	Vcc±0.3V	HIGH-Z
RESET	X	X	X	L	HIGH-Z
SECTOR PROTECT	L	H	L	V_{ID}	D_{IN}, D_{OUT}
SECTOR UNPROTECT	L	H	L	V_{ID}	D_{IN}, D_{OUT}
READ	L	L	H	H	D_{OUT}
WRITE	L	H	L	H	D_{OUT}

Note : X means don't care, WE0* Low byte (D0~7) Write enable, WE1* High byte(D8~15) Write enable.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Voltage on Any Pin Relative to Vss	-0.5V to Vcc +0.5V
Voltage on Vcc Supply Relative to Vss	-0.5V to +4.0V
Output Short Circuit Current	1,600mA
Storage Temperature	-65^{O}C to +150^{O}C
Operating Temperature	-0^{O}C to +70^{O}C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RANGE
Vcc for regulated Supply Voltage	+2.0V to 3.6V
Vcc for full voltage	+2.7V to 3.6V

DC AND OPERATING CHARACTERISTICS

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V_{IN}= V_{SS} to V_{CC} , V_{CC}= V_{CC} max	I_{L1}	-4.0	+4.0	µA
Output Leakage Current	V_{OUT}= V_{SS} to V_{CC}, V_{CC}= V_{CC} max	I_{L0}	-4.0	+4.0	µA
Output High Voltage	I_{OH} = -2.0mA, Vcc = Vcc min	V_{OH}	0.85xVcc		V
Output Low Voltage	I_{OL} = 4.0mA, Vcc = Vcc min	V_{OL}		0.4	V
Vcc Active Read Current	/CE = V_{IL}, ,/OE=V_{IL}, f=5MHz	I_{CC1}		64	mA
Vcc Active Write Current	/CE = V_{IL}, /OE=V_{IH}	I_{CC2}		180	mA
Vcc Standby Current	/CE, RESET=V_{CC}±0.3V	I_{CC3}		20	µA
Vcc Reset Current	/RESET=Vss±0.3V,	I_{CC4}		20	µA

Low Vcc Lock-Out Voltage		V_{LKO}	1.5		V

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Block Erase Time	-	0.7	15	Sec	Excludes 00H programming prior to erasure
Byte Programming Time	-	9	270	μS	Excludes system-level overhead
Chip Programming Time	-	18	54	sec	Excludes system-level overhead

CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN.	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		10	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0		10	pF

Notes: Test conditions $T_A = 25^oC$, f=1.0 MHz.

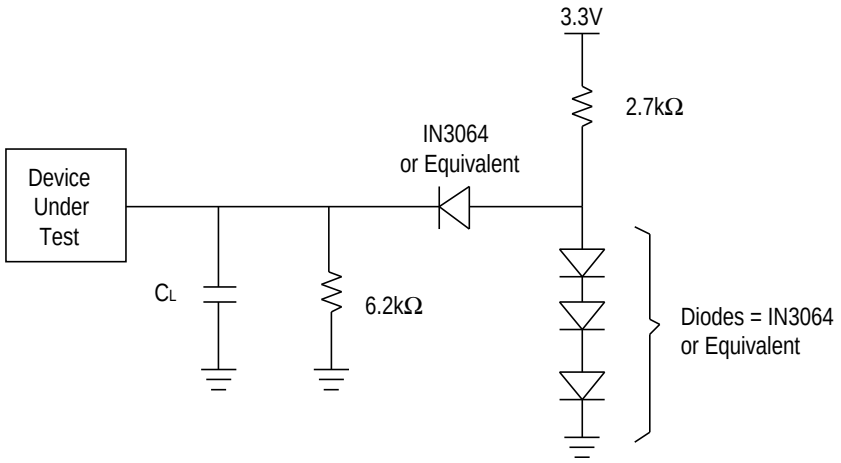
AC CHARACTERISTICS

u Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION	CL=100pF						UNIT
JEDEC	STANDARD		-90		-100		-120		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Read Cycle Time	90		100		120		ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		90		100		120	ns
t_{GLQV}	t_{OE}	Chip Enable to Output Delay		35		40		50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z		30		30		30	ns
t_{AXQX}	t_{QH}	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First	0		0		0		ns

TEST CONDITIONS

TEST CONDITION	VALUE	UNIT
Output load	1TTL gate	
Input rise and full times	5	ns
Input pulse levels	0.0 - 3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V



Note : C_L = 100pF including jig capacitance

u Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION	C_L=100pF						UNIT
JEDEC	STANDARD		-90		-100		-120		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	90		100		120		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{WLAX}	t_{AH}	Address Hold Time	45		45		50		ns
t_{DVWH}	t_{DS}	Data Setup Time	45		45		50		ns
t_{WHDX}	t_{DH}	Data Hold Time	0		0		0		ns
	t_{OES}	Output Enable Setup Time	0		0		0		ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	0		0		0		ns
t_{ELWL}	t_{CS}	/CE Setup Time	0		0		0		ns
t_{WHEH}	t_{CH}	/CE Hold Time	0		0		0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	45		45		50		ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	30		30		30		ns

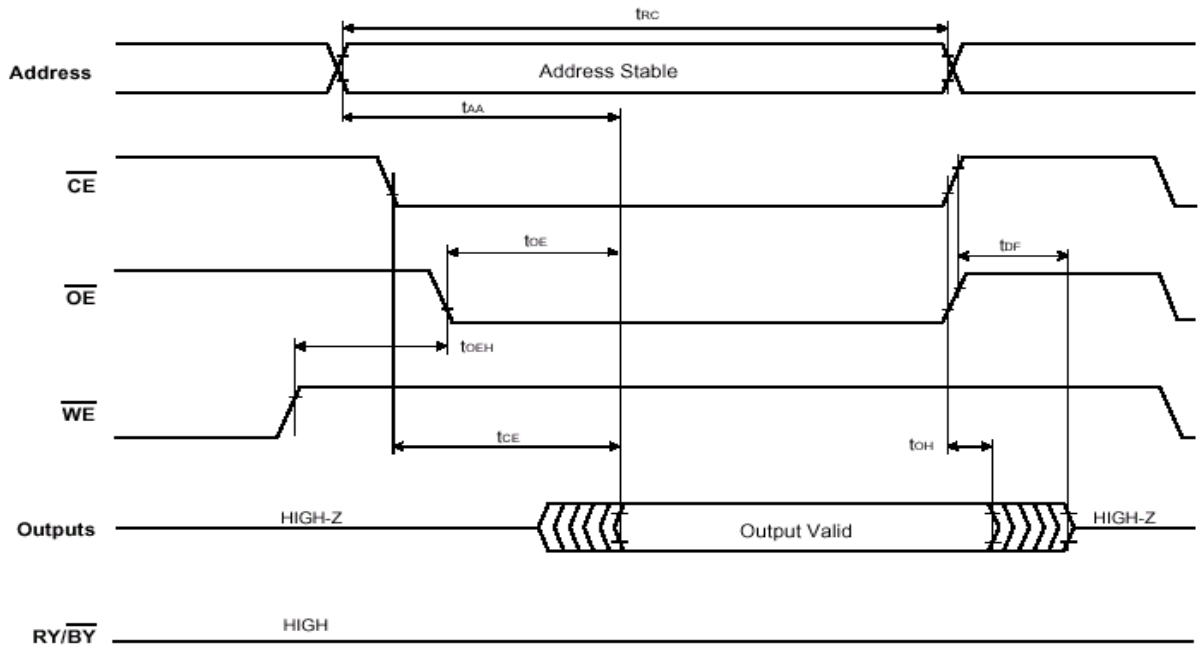
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	9		9		9		μs
t_{WHWH2}	t_{BERS}	Block Erase Operation	0.7		0.7		0.7		sec
	t_{VCS}	Vcc Setup Time	50		50		50		μs
	t_{RB}	Recovery time from RY/BY	0		0		0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY Delay	90		90		90		ns

u Alternate /CE Controlled Erase/Program Operations

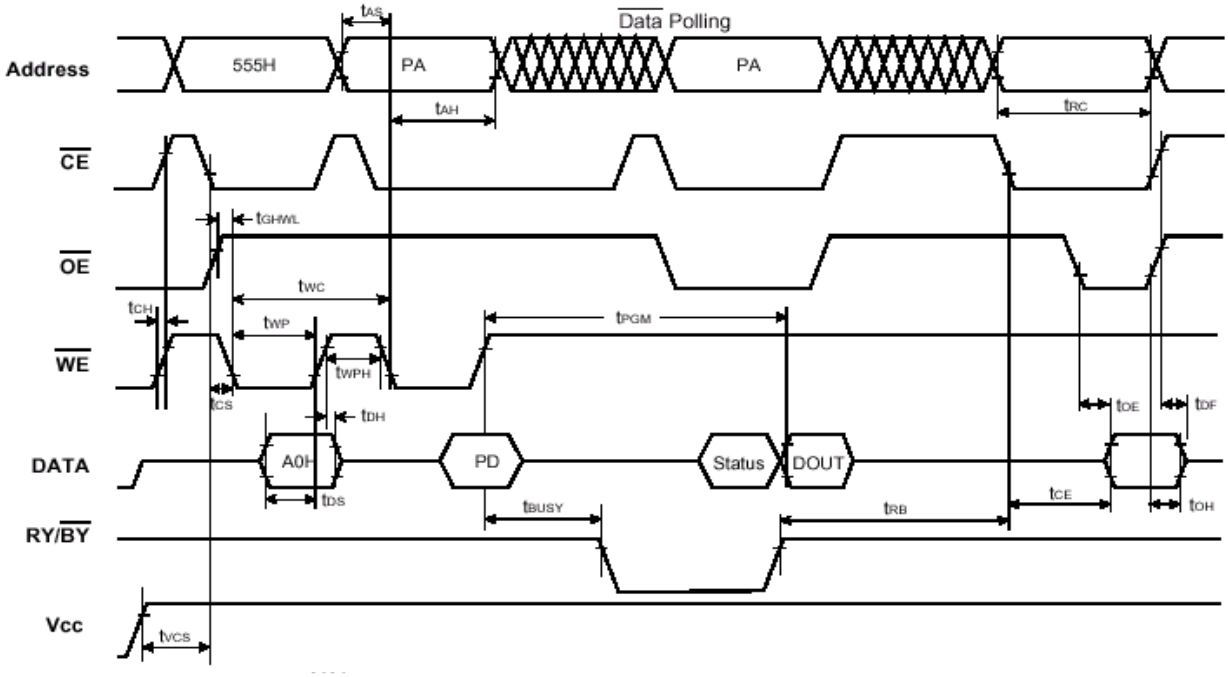
PARAMETER SYMBOLS		DESCRIPTION	C_L=100pF						UNIT
			-90		-100		-120		
JEDEC	STANDARD		Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	90		100		120		ns
t_{AVEL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{ELAX}	t_{AH}	Address Hold Time	45		45		50		ns
t_{DVEH}	t_{DS}	Data Setup Time	45		45		50		ns
t_{EHDX}	t_{DH}	Data Hold Time	0		0		0		ns
	t_{OES}	Output Enable Setup Time	0		0		0		ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write	0		0		0		ns
t_{WLEL}	t_{WS}	/OE High to /WE Low	0		0		0		ns
t_{EHWH}	t_{WH}	/WE Hold Time	0		0		0		ns
t_{ELEH}	t_{CP}	/CE Pulse Width	45		45		50		ns
t_{EHEL}	t_{CPH}	/CE Pulse Width High	30		30		30		ns
	t_{BUSY}	Program/Erase Valid RY//BY Delay	90		90		90		ns
	t_{RB}	Recovery Time from RY//BY	0		0		0		ns

TIMING DIAGRAMS

Read Operations



Alternate WE Controlled Program Operations

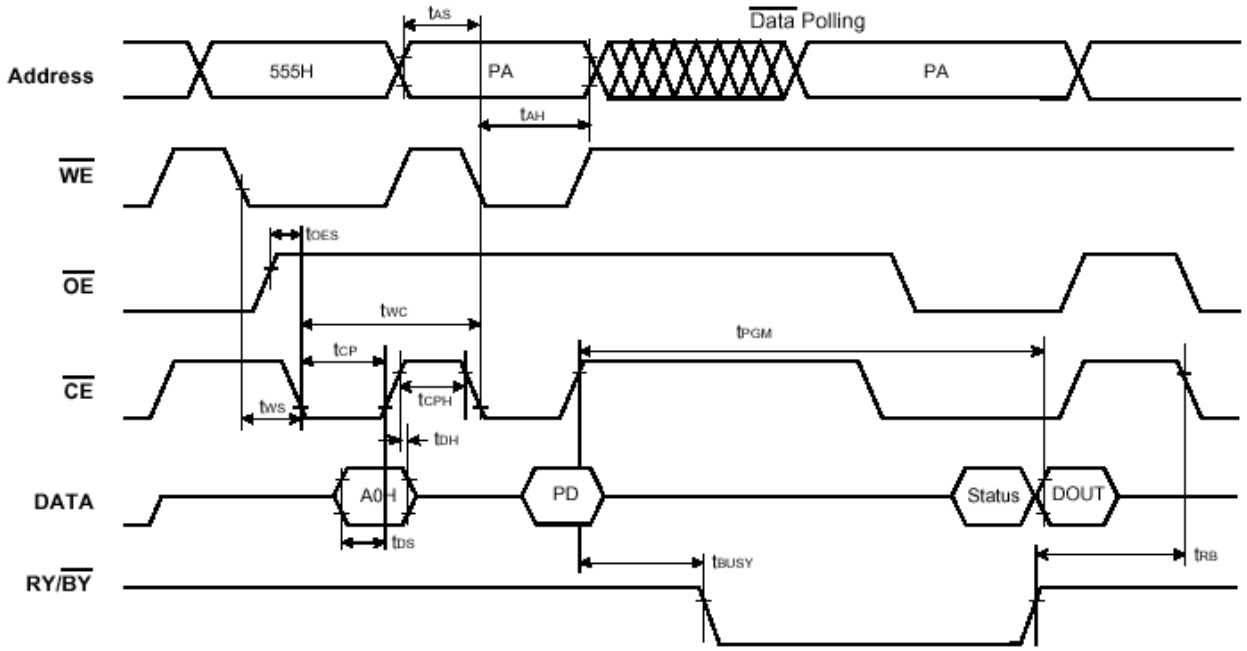


Notes :

1. DQ7 is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data

4. The illustration shows the last two cycles of the program command sequence.

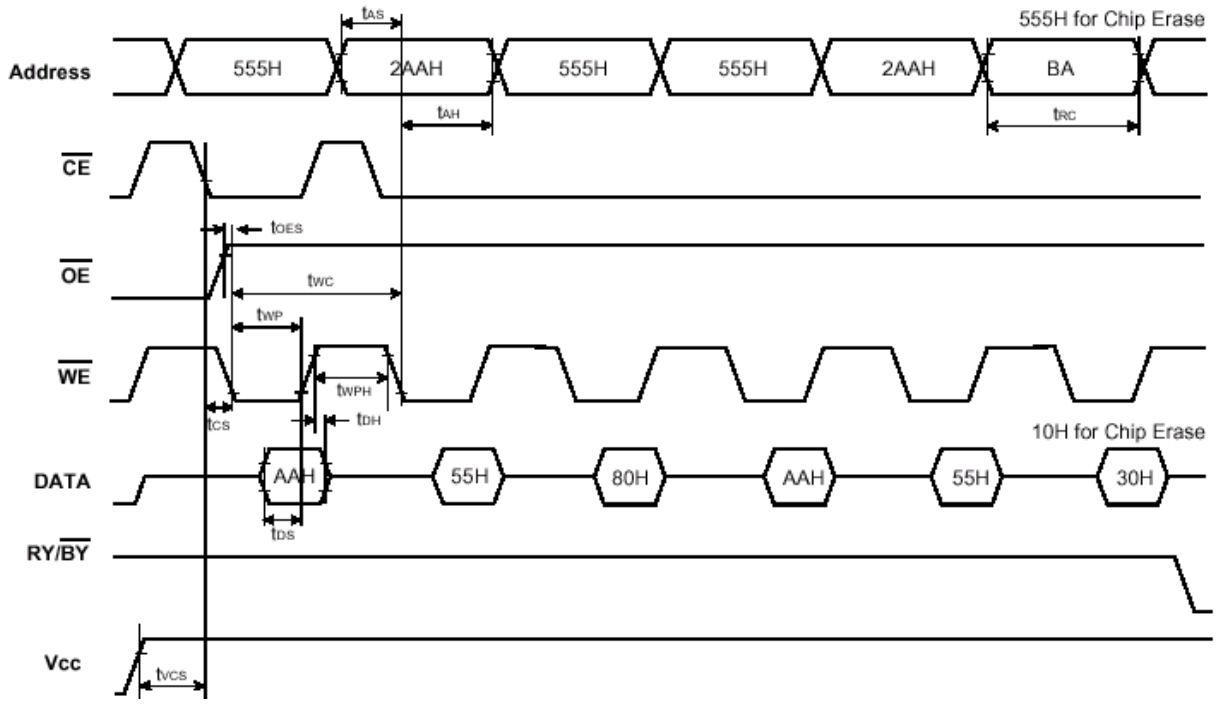
Alternate $\overline{CE}$ Controlled Program Operations



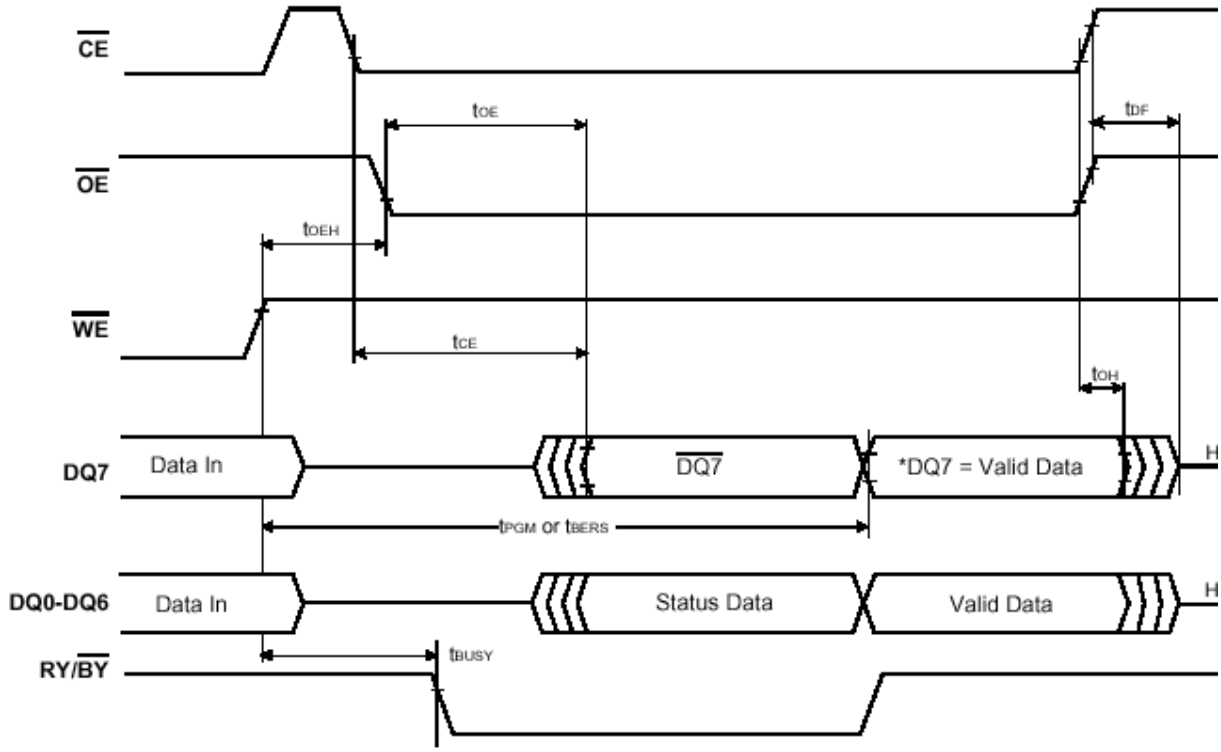
Notes :

1. DQ7 is the output of the complement of the data written to the device.
2. DOUT is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

Chip/Block Erase Operations

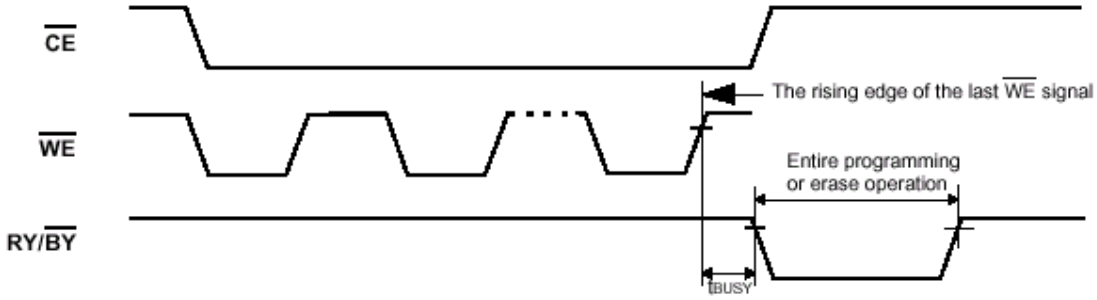


Data Polling During Internal Routine Operation



Note :
*DQ7=Valid Data (The device has completed the internal operation).

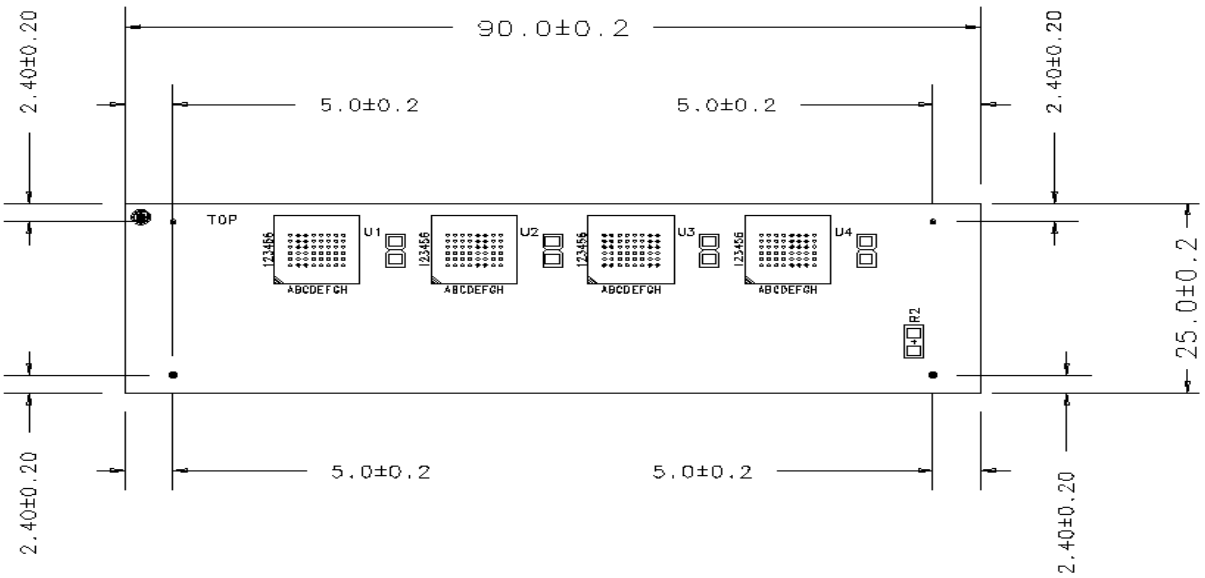
RY/BY Timing Diagram During Program/Erase Operation



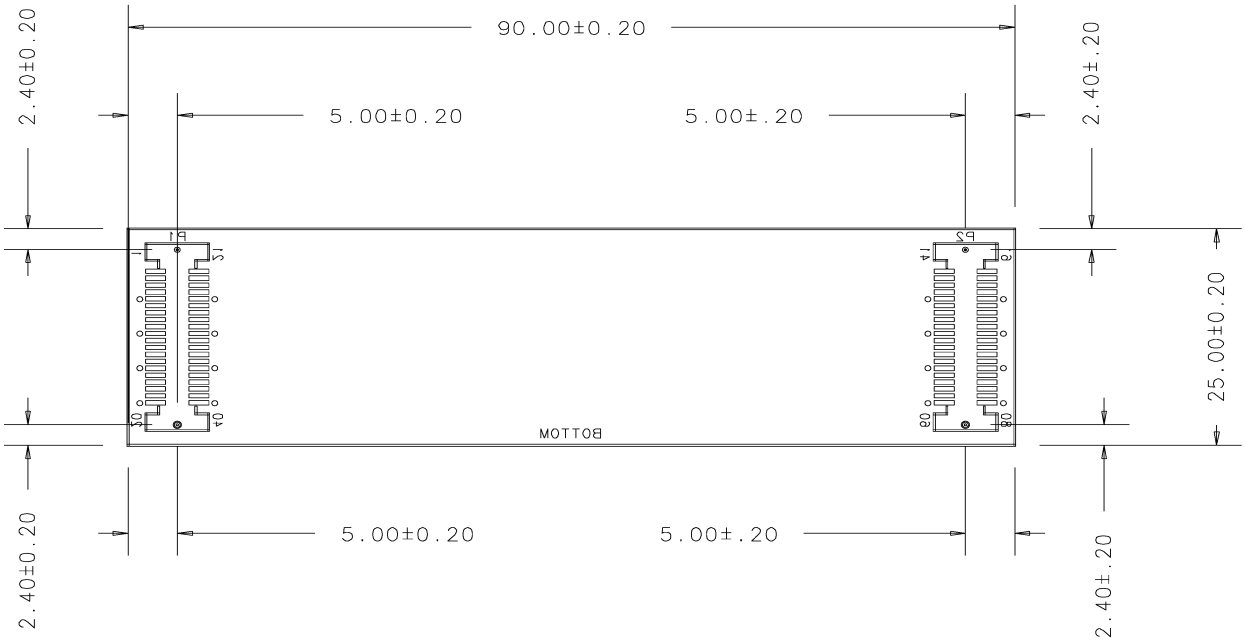
PACKAGE DIMENSIONS

UNIT: mm

Front-Side



Rear-Side



ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMF8M8F4VS-90	8MByte	8M x 8	80Pin -SMM	4EA	3.3V	90ns
HMF8M8F4VS-100	8MByte	8M x 8	80Pin -SMM	4EA	3.3V	100ns
HMF8M8F4VS-120	8MByte	8M x 8	80Pin -SMM	4EA	3.3V	120ns