SSTUH32864

1.8 V high output drive configurable registered buffer for DDR2 RDIMM applications

Rev. 01 — 22 April 2005 Product data sheet

1. General description

The SSTUH32864 is a 25-bit 1 : 1 or 14-bit 1 : 2 configurable registered buffer designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTUH32864 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going HIGH, and $\overline{CK}$ going LOW.

The C0 input controls the pinout configuration of the 1 : 2 pinout from A configuration (when LOW) to B configuration (when HIGH). The C1 input controls the pinout configuration from 25-bit 1 : 1 (when LOW) to 14-bit 1 : 2 (when HIGH).

The device supports low-power standby operation. When the reset input ($\overline{RESET}$) is LOW, the differential input receivers are disabled, and un-driven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when $\overline{RESET}$ is LOW all registers are reset, and all outputs are forced LOW. The LVCMOS $\overline{RESET}$ and Cn inputs must always be held at a valid logic HIGH or LOW level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the LOW state during power-up.

In the DDR2 RDIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the data outputs will be driven LOW quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are LOW, and the clock is stable during the time from the LOW-to-HIGH transition of $\overline{RESET}$ until the input receivers are fully enabled, the design of the SSTUH32864 must ensure that the outputs will remain LOW, thus ensuring no glitches on the output.

The device monitors both $\overline{DCS}$ and $\overline{CSR}$ inputs and will gate the Qn outputs from changing states when both $\overline{DCS}$ and $\overline{CSR}$ inputs are HIGH. If either $\overline{DCS}$ or $\overline{CSR}$ input is LOW, the Qn outputs will function normally. The $\overline{RESET}$ input has priority over the $\overline{DCS}$ and $\overline{CSR}$ control and will force the outputs LOW. If the $\overline{DCS}$-control functionality is not desired, then the $\overline{CSR}$ input can be hardwired to ground, in which case the setup time requirement for $\overline{DCS}$ would be the same as for the other Dn data inputs.

The SSTUH32864 is available in a 96-ball, low profile fine-pitch ball grid array (LFBGA96) package.

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The SSTUH32864 is identical to SSTU32864 in function and performance, with higher-drive outputs optimized to drive heavy load nets (such as stacked DRAMs) while maintaining speed and signal integrity.

2. Features

- Configurable register supporting DDR2 Registered DIMM applications
- Higher output drive strength version of SSTU32864 optimized for high-capacitive load nets
- Configurable to 25-bit 1 : 1 mode or 14-bit 1 : 2 mode
- Controlled output impedance drivers enable optimal signal integrity and speed
- Exceeds JESD82-7 speed performance (1.8 ns max. single-bit switching propagation delay; 2.0 ns max. mass-switching)
- Supports up to 450 MHz clock frequency of operation
- Optimized pinout for high-density DDR2 module design
- Chip-selects minimize power consumption by gating data outputs from changing state
- Supports SSTL_18 data inputs
- Differential clock (CK and $\overline{CK}$) inputs
- Supports LVCMOS switching levels on the control and $\overline{RESET}$ inputs
- Single 1.8 V supply operation
- Available in 96-ball, 13.5 × 5.5 mm, 0.8 mm ball pitch LFBGA package

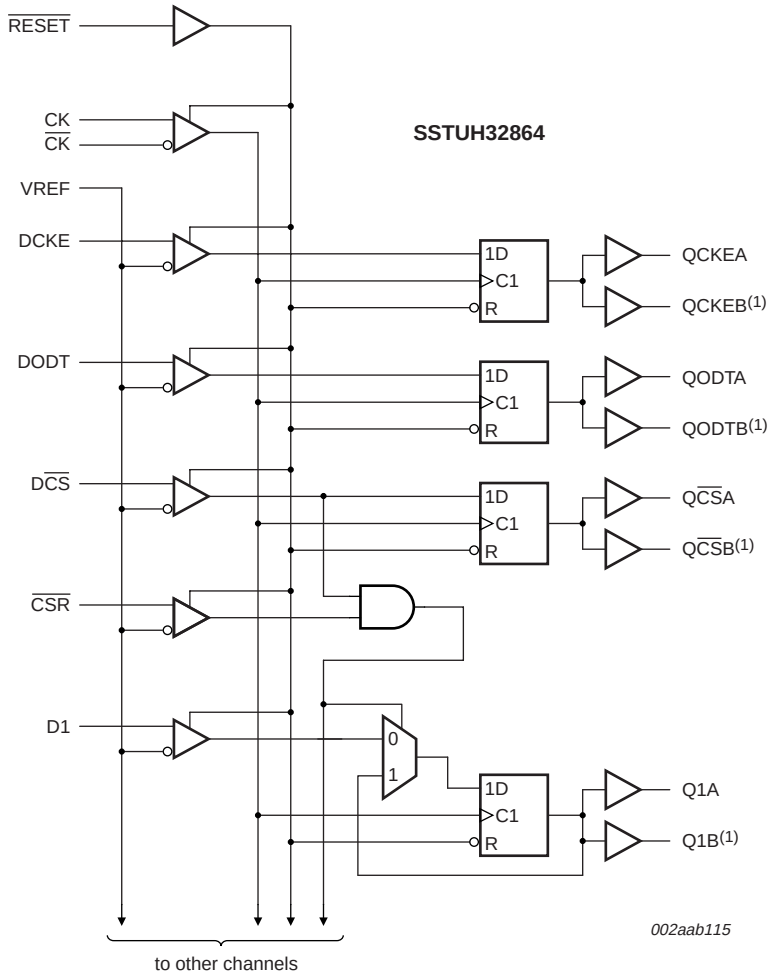
3. Ordering information

Table 1: Ordering information

T_{amb} = 0 °C to +70 °C.

Type number	Solder process	Package		
		Name	Description	Version
SSTUH32864EC/G	Pb-free (SnAgCu solder ball compound)	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1
SSTUH32864EC	SnPb solder ball compound	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

4. Functional diagram



(1) Disabled in 1 : 1 configuration.

Fig 1. Functional diagram of SSTUH32864; 1 : 2 mode (positive logic)

5. Pinning information

5.1 Pinning

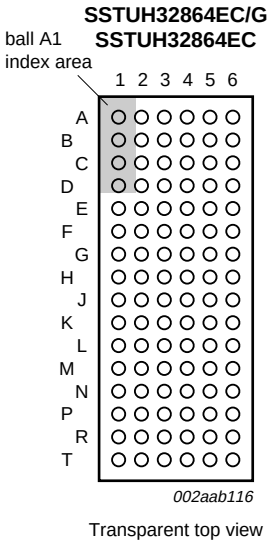


Fig 2. Pin configuration for LFBGA96

	1	2	3	4	5	6
A	DCKE	n.c.	VREF	V_{DD}	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V_{DD}	V_{DD}	Q3	Q16
D	DODT	n.c.	GND	GND	QODT	DNU
E	D5	D17	V_{DD}	V_{DD}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	n.c.	$\overline{\text{RESET}}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$	DNU
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V_{DD}	V_{DD}	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V_{DD}	V_{DD}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V_{DD}	V_{DD}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V_{DD}	V_{DD}	Q13	Q24
T	D14	D25	VREF	V_{DD}	Q14	Q25

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Fig 3. Ball mapping; 1 : 1 register (C0 = 0, C1 = 0); top view

	1	2	3	4	5	6
A	DCKE	n.c.	VREF	V_{DD}	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{DD}	V_{DD}	Q3A	Q3B
D	DODT	n.c.	GND	GND	QODTA	QODTB
E	D5	DNU	V_{DD}	V_{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	n.c.	$\overline{\text{RESET}}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$A	$\overline{\text{QCS}}$B
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V_{DD}	V_{DD}	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{DD}	V_{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V_{DD}	V_{DD}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{DD}	V_{DD}	Q13A	Q13B
T	D14	DNU	VREF	V_{DD}	Q14A	Q14B

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Fig 4. Ball mapping; 1 : 2 register A (C0 = 0, C1 = 1); top view

	1	2	3	4	5	6
A	D1	n.c.	VREF	V_{DD}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{DD}	V_{DD}	Q3A	Q3B
D	D4	n.c.	GND	GND	Q4A	Q4B
E	D5	DNU	V_{DD}	V_{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	n.c.	$\overline{\text{RESET}}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$A	$\overline{\text{QCS}}$B
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V_{DD}	V_{DD}	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{DD}	V_{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	V_{DD}	V_{DD}	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{DD}	V_{DD}	Q13A	Q13B
T	DCKE	DNU	VREF	V_{DD}	QCKEA	QCKEB

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Fig 5. Ball mapping; 1 : 2 register B (C0 = 1, C1 = 1); top view

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Type	Description
GND	B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4	ground input	ground
V_{DD}	A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4	1.8 V nominal	power supply voltage
VREF	A3, T3	0.9 V nominal	input reference voltage
ZOH	J5	input	reserved for future use
ZOL	J6	input	reserved for future use
CK	H1	differential input	positive master clock input
$\overline{CK}$	J1	differential input	negative master clock input
C0, C1	G6, G5	LVCMOS inputs	configuration control inputs
$\overline{RESET}$	G2	LVCMOS input	Asynchronous reset input (active LOW). Resets registers and disables VREF data and clock differential-input receivers.
$\overline{CSR}$, $\overline{DCS}$	J2, H2	SSTL_18 input	Chip select inputs (active LOW). Disables data outputs switching when both inputs are HIGH [2].
D1 to D25	[1]	SSTL_18 input	Data inputs. Clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{CK}$.
DODT	[1]	SSTL_18 input	The outputs of this register will not be suspended by $\overline{DCS}$ and $\overline{CSR}$ control.
DCKE	[1]	SSTL_18 input	The outputs of this register will not be suspended by $\overline{DCS}$ and $\overline{CSR}$ control.
Q1 to Q25, Q1A to Q14A, Q1B to Q14B	[1]	1.8 V CMOS	The outputs that are suspended by $\overline{DCS}$ and $\overline{CSR}$ control [3].
Q$\overline{CS}$, Q$\overline{CS}$A, Q$\overline{CS}$B	[1]	1.8 V CMOS	data outputs that will not be suspended by $\overline{DCS}$ and $\overline{CSR}$ control
QODT, QODTA, QODTB	[1]	1.8 V CMOS	data outputs that will not be suspended by $\overline{DCS}$ and $\overline{CSR}$ control
QCKE, QCKEA, QCKEB	[1]	1.8 V CMOS	data outputs that will not be suspended by $\overline{DCS}$ and $\overline{CSR}$ control
n.c.	A2, D2, G1	-	Not connected. Ball present but no internal connection to the die.
DNU	[1]	-	Do-not-use. Ball internally connected to the die which should be left open-circuit.

[1] Depends on configuration. See Figure 3, Figure 4, and Figure 5 for ball number.

[2] Configurations:
Data inputs = D2, D3, D5, D6, D8 to D25 when C0 = 0 and C1 = 0.
Data inputs = D2, D3, D5, D6, D8 to D14 when C0 = 0 and C1 = 1.
Data inputs = D1 to D6, D8 to D10, D12, D13 when C0 = 1 and C1 = 1.

[3] Configurations:
Data outputs = Q2, Q3, Q5, Q6, Q8 to Q25 when C0 = 0 and C1 = 0.
Data outputs = Q2, Q3, Q5, Q6, Q8 to Q14 when C0 = 0 and C1 = 1.
Data outputs = Q1 to Q6, Q8 to Q10, Q12, Q13 when C0 = 1 and C1 = 1.

6. Functional description

6.1 Function table

Table 3: Function table (each flip-flop)

L = LOW voltage level; H = HIGH voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition

Inputs						Outputs [1]		
$\overline{RESET}$	$D\overline{CS}$	$\overline{CSR}$	CK	$\overline{CK}$	Dn, DODT, DCKE	Qn	$Q\overline{CS}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	H	↑	↓	L	Q_0	H	L
H	H	H	↑	↓	H	Q_0	H	H
H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L

[1] Q_0 is the previous state of the associated output.

7. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+2.5	V
V_I	receiver input voltage		–0.5 [1]	+2.5 [2]	V
V_O	driver output voltage		–0.5 [1]	V_{DD} + 0.5 [2]	V
I_{IK}	input clamp current	$V_I < 0$ V or $V_I > V_{DD}$	-	±50	mA
I_{OK}	output clamp current	$V_O < 0$ V or $V_O > V_{DD}$	-	±50	mA
I_O	continuous output current	$0 V < V_O < V_{DD}$	-	±50	mA
I_{CCC}	continuous current through each V_{DD} or GND pin		-	±100	mA
T_{stg}	storage temperature		–65	+150	°C

[1] The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

[2] This value is limited to 2.5 V maximum.

8. Recommended operating conditions

Table 5: Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			1.7	-	1.9	V
V_{ref}	reference voltage			$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_{TT}	termination voltage			$V_{ref} - 0.040$	V_{ref}	$V_{ref} + 0.040$	V
V_I	input voltage			0	-	V_{DD}	V
$V_{IH(AC)}$	AC HIGH-level input voltage	data inputs (Dn), $\overline{CSR}$		$V_{ref} + 0.250$	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage	data inputs (Dn), $\overline{CSR}$		-	-	$V_{ref} - 0.250$	V
$V_{IH(DC)}$	DC HIGH-level input voltage	data inputs (Dn), $\overline{CSR}$		$V_{ref} + 0.125$	-	-	V
$V_{IL(DC)}$	DC LOW-level input voltage	data inputs (Dn), $\overline{CSR}$		-	-	$V_{ref} - 0.125$	V
V_{IH}	HIGH-level input voltage	$\overline{RESET}$, Cn	[1]	$0.65 \times V_{DD}$	-	V_{DD}	V
V_{IL}	LOW-level input voltage	$\overline{RESET}$, Cn	[1]	-	-	$0.35 \times V_{DD}$	V
V_{ICR}	common mode input voltage range	CK, $\overline{CK}$	[2]	0.675	-	1.125	V
V_{ID}	differential input voltage	CK, $\overline{CK}$	[2]	600	-	-	mV
I_{OH}	HIGH-level output current			-	-	–12	mA
I_{OL}	LOW-level output current			-	-	12	mA
T_{amb}	ambient temperature	operating in free air		0	-	+70	°C

[1] The $\overline{RESET}$ and Cn inputs of the device must be held at valid logic levels (not floating) to ensure proper device operation.

[2] The differential inputs must not be floating, unless $\overline{RESET}$ is LOW.

9. Characteristics

Table 6: Characteristics

Recommended operating conditions; T_{amb} = 0 °C to +70 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = –12 mA; V_{DD} = 1.7 V	1.2	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 12 mA; V_{DD} = 1.7 V	-	-	0.5	V
I_I	input current	all inputs; $V_I = V_{DD}$ or GND; V_{DD} = 1.9 V	–5	-	+5	µA
I_{DD}	static standby current	$\overline{RESET}$ = GND; I_O = 0 mA; V_{DD} = 1.9 V	-	-	100	µA
	static operating current	$\overline{RESET} = V_{DD}$; I_O = 0 mA; V_{DD} = 1.9 V; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	40	mA
I_{DDD}	dynamic operating current per MHz, clock only	$\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle. I_O = 0 mA; V_{DD} = 1.9 V	-	16	-	µA
	dynamic operating current per MHz, per each data input, 1 : 1 mode	$\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle. One data input switching at half clock frequency, 50 % duty cycle. I_O = 0 mA; V_{DD} = 1.9 V	-	11	-	µA
	dynamic operating current per MHz, per each data input, 1 : 2 mode	$\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle. One data input switching at half clock frequency, 50 % duty cycle. I_O = 0 mA; V_{DD} = 1.9 V	-	19	-	µA
C_i	input capacitance, data inputs, $\overline{CSR}$	$V_I = V_{ref} \pm 250$ mV; V_{DD} = 1.8 V	2.5	-	3.5	pF
	input capacitance, CK and $\overline{CK}$	V_{ICR} = 0.9 V; V_{ID} = 600 mV; V_{DD} = 1.8 V	2	-	3	pF
	input capacitance, $\overline{RESET}$	$V_I = V_{DD}$ or GND; V_{DD} = 1.8 V	2	-	4	pF

Table 7: Timing requirements

Recommended operating conditions; T_{amb} = 0 °C to +70 °C; V_{DD} = 1.8 V ± 0.1 V; unless otherwise specified. See Figure 6 through Figure 11.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clock}	clock frequency			-	-	450	MHz
t_W	pulse duration, CK, $\overline{CK}$ HIGH or LOW			1	-	-	ns
t_{ACT}	differential inputs active time		[1] [2]	-	-	10	ns
t_{INACT}	differential inputs inactive time		[1] [3]	-	-	15	ns
t_{su}	setup time	$\overline{DCS}$ before CK ↑, $\overline{CK}$ ↓, $\overline{CSR}$ HIGH		0.7	-	-	ns
		$\overline{DCS}$ before CK ↑, $\overline{CK}$ ↓, $\overline{CSR}$ LOW		0.5	-	-	ns
		$\overline{CSR}$, DODT, DCKE, and data before CK ↑, $\overline{CK}$ ↓		0.5	-	-	ns
t_h	hold time	$\overline{DCS}$, $\overline{CSR}$, DODT, DCKE, and data after CK ↑, $\overline{CK}$ ↓		0.5	-	-	ns

[1] This parameter is not necessarily production tested.

[2] Data inputs must be active below a minimum time of $t_{ACT(max)}$ after $\overline{RESET}$ is taken HIGH.

[3] Data and clock inputs must be held at valid levels (not floating) a minimum time of $t_{INACT(max)}$ after $\overline{RESET}$ is taken LOW.

Table 8: Switching characteristics

Recommended operating conditions; T_{amb} = 0 °C to +70 °C; V_{DD} = 1.8 V ± 0.1 V; Class I, $V_{ref} = V_{TT} = V_{DD} \times 0.5$ and C_L = 10 pF; unless otherwise specified. See Figure 6 through Figure 11.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MAX}	maximum input clock frequency			450	-	-	MHz
t_{PDM}	propagation delay	CK and $\overline{CK}$ to output	[1]	1.41	-	1.8	ns
t_{PDMSS}	propagation delay, simultaneous switching	CK and $\overline{CK}$ to output	[1] [2]	-	-	2.0	ns
t_{PHL}	propagation delay	$\overline{RESET}$ to output		-	-	3	ns

[1] Includes 350 ps of test-load transmission line delay.

[2] This parameter is not necessarily production tested.

Table 9: Output edge rates

Recommended operating conditions, unless otherwise specified. V_{DD} = 1.8 V ± 0.1 V

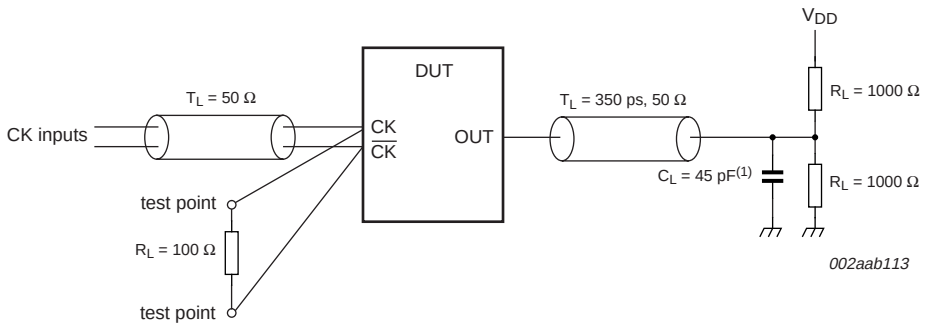
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV/dt_r	rising edge slew rate		1	-	4	V/ns
dV/dt_f	falling edge slew rate		1	-	4	V/ns
dV/dt_Δ	absolute difference between dV/dt_r and dV/dt_f		-	-	1	V/ns

10. Test information

10.1 Test circuit

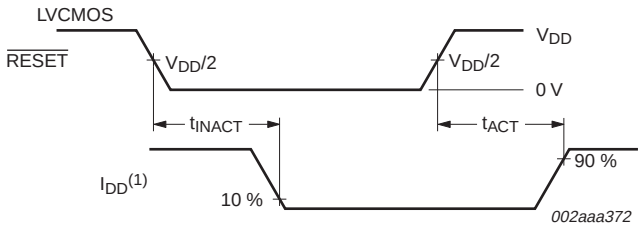
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_0 = 50 Ω; input slew rate = 1 V/ns ± 20 %, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



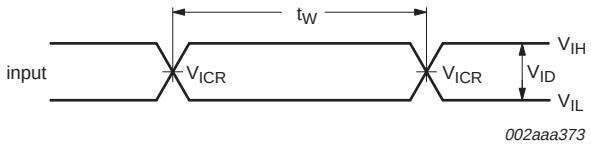
(1) C_L includes probe and jig capacitance.

Fig 6. Load circuit



(1) I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

Fig 7. Voltage and current waveforms; inputs active and inactive times

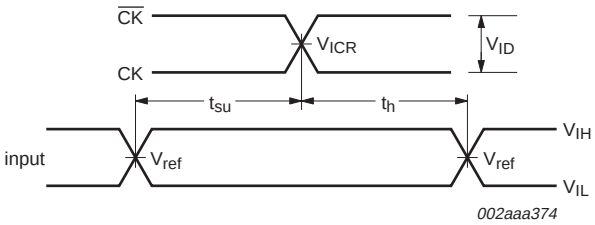


V_{ID} = 600 mV

$V_{IH} = V_{ref}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

$V_{IL} = V_{ref}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 8. Voltage waveforms; pulse duration



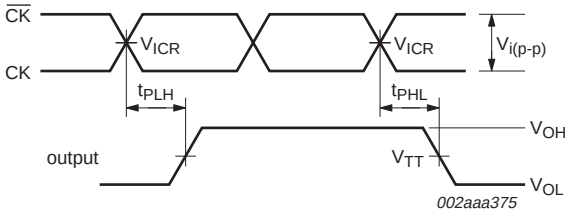
V_{ID} = 600 mV

$V_{ref} = V_{DD}/2$

$V_{IH} = V_{ref}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

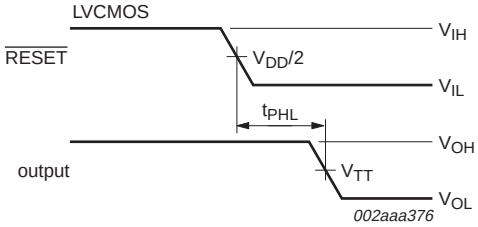
$V_{IL} = V_{ref}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 9. Voltage waveforms; setup and hold times



t_{PLH} and t_{PHL} are the same as t_{PD}.

Fig 10. Voltage waveforms; propagation delay times (clock to output)



t_{PLH} and t_{PHL} are the same as t_{PD}.

$V_{IH} = V_{ref}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

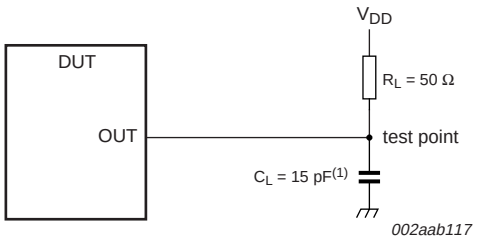
$V_{IL} = V_{ref}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 11. Voltage waveforms; propagation delay times (reset to output)

10.2 Output slew rate measurement

V_{DD} = 1.8 V ± 0.1 V.

All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz; Z_0 = 50 Ω; input slew rate = 1 V/ns ± 20 %, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Fig 12. Load circuit, HIGH-to-LOW slew measurement

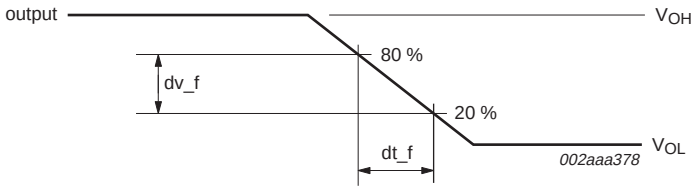
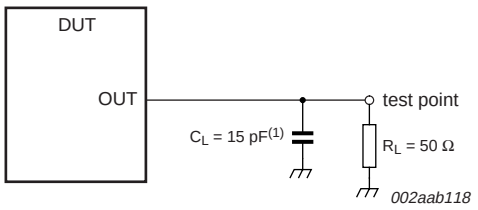


Fig 13. Voltage waveforms, HIGH-to-LOW slew rate measurement



(1) C_L includes probe and jig capacitance.

Fig 14. Load circuit, LOW-to-HIGH slew measurement

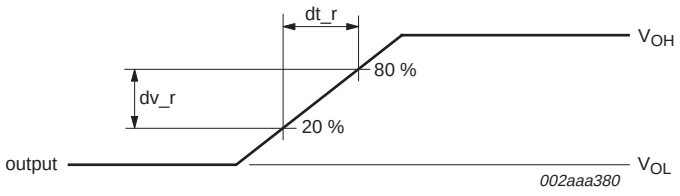
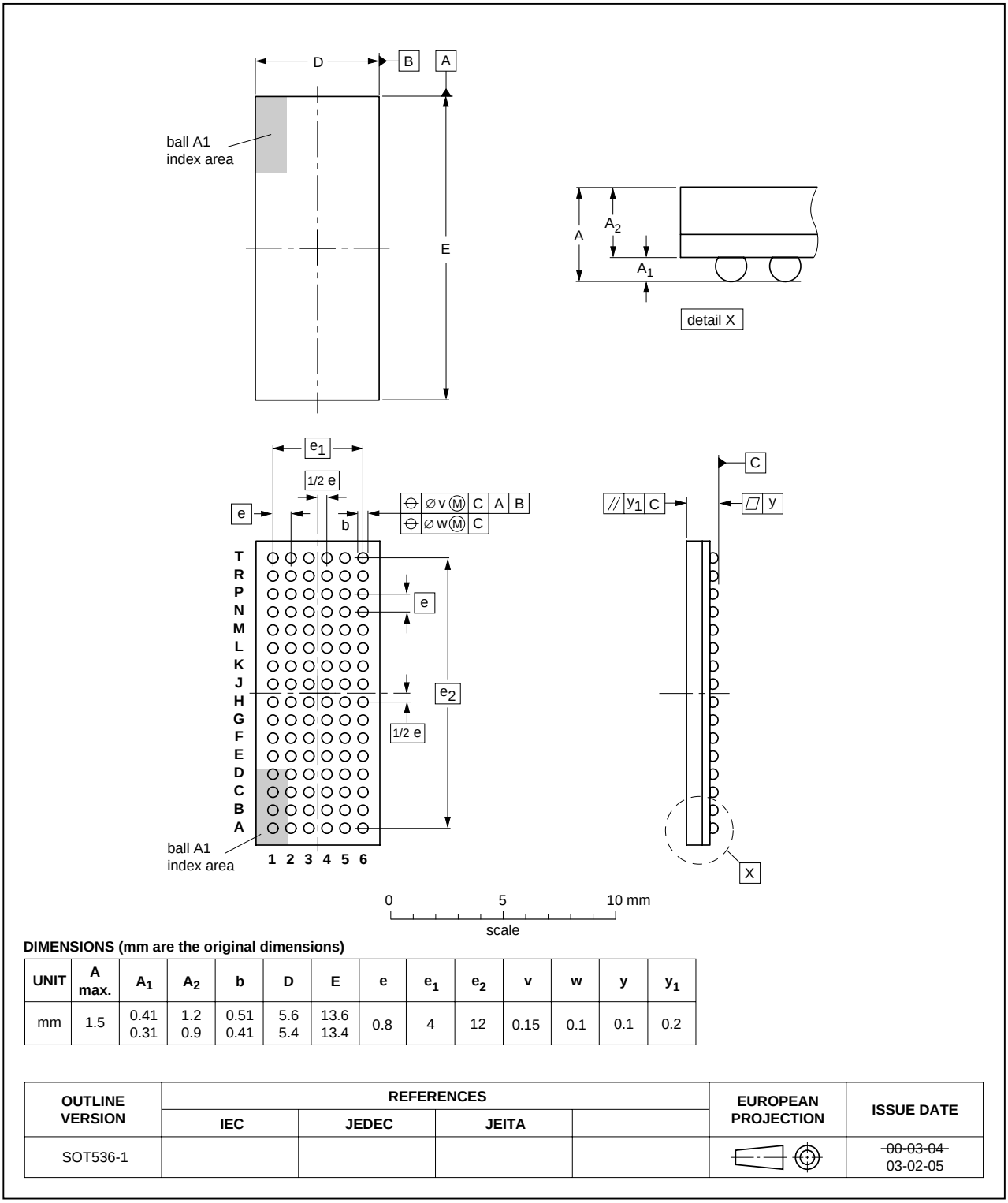


Fig 15. Voltage waveforms, LOW-to-HIGH slew rate measurement

11. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						~~00-03-04~~ 03-02-05

Fig 16. Package outline SOT536-1 (LFBGA96)

12. Soldering

12.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

12.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

12.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

12.5 Package related soldering information

Table 10: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

13. Abbreviations

Table 11: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Silicon
DDR	Double Data Rate
DIMM	Dual In-line Memory Module
LFBGA	Low profile Fine-pitch Ball Grid Array
LVCMOS	Low Voltage Complementary Metal Oxide Silicon
PRR	Pulse Repetition Rate
RDIMM	Registered Dual In-line Memory Module
SSTL	Stub Series Terminated Logic

14. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
SSTUH32864_1	20050422	Product data sheet	-	9397 750 14137	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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19. Contents

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