DESCRIPTION

PT6965 is an LED Controller driven on a 1/5 to 1/8 duty factor. 11 segment output lines, 4 grid output lines, 3 segment/grid output lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Serial data is fed to PT6965 via a four-line serial interface. Housed in a 30-pin SSOP and TSSOP, PT6965 pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

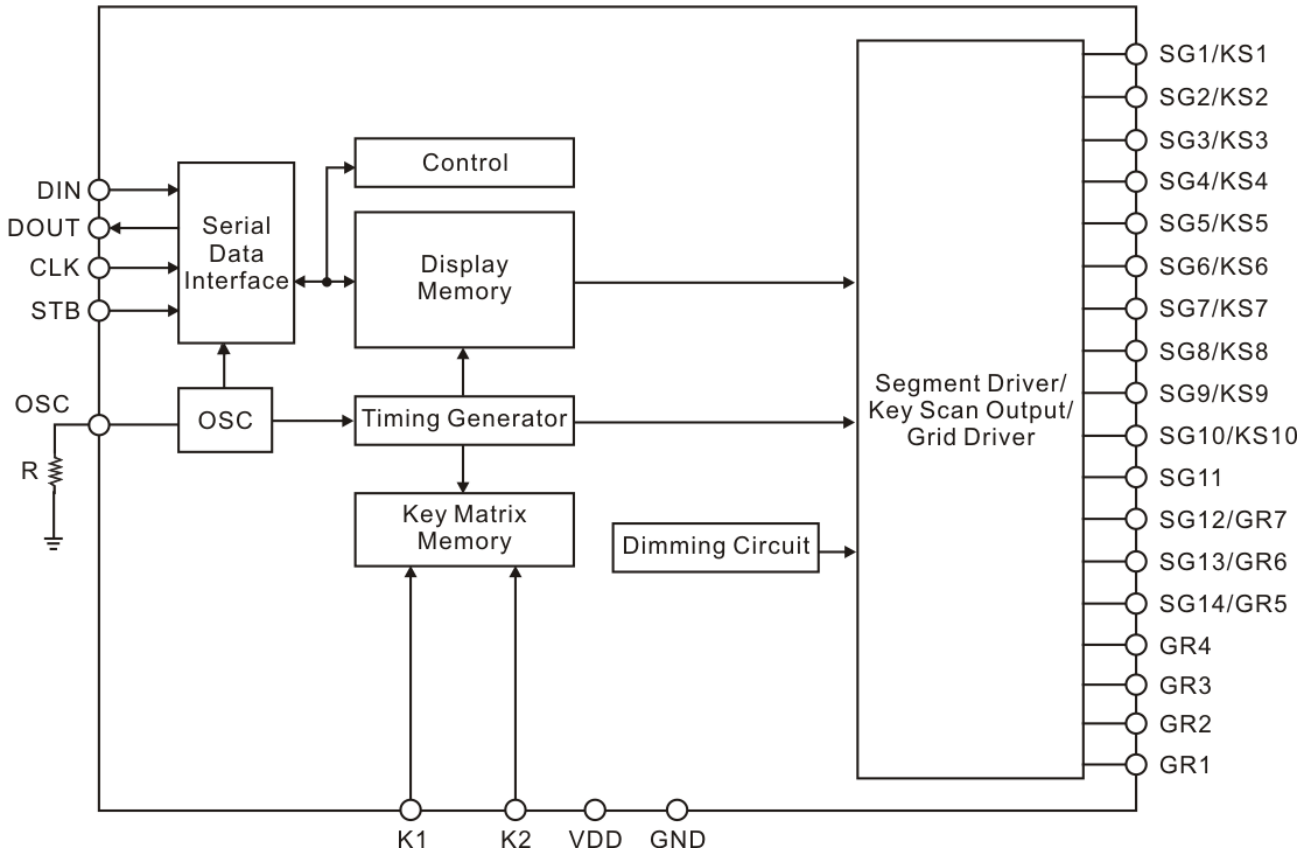
FEATURES

- CMOS technology
- Low power consumption
- Multiple display modes (14 segment, 4 Grid to 11 segment, 7 Grid)
- Key scanning (10 x 2 Matrix)
- 8-Step dimming circuitry
- Serial Interface for clock, data input, data output, strobe pins and low voltage operation ability when user's MCU power supply is 3.3 V
- Available in 30-pin, SSOP and TSSOP

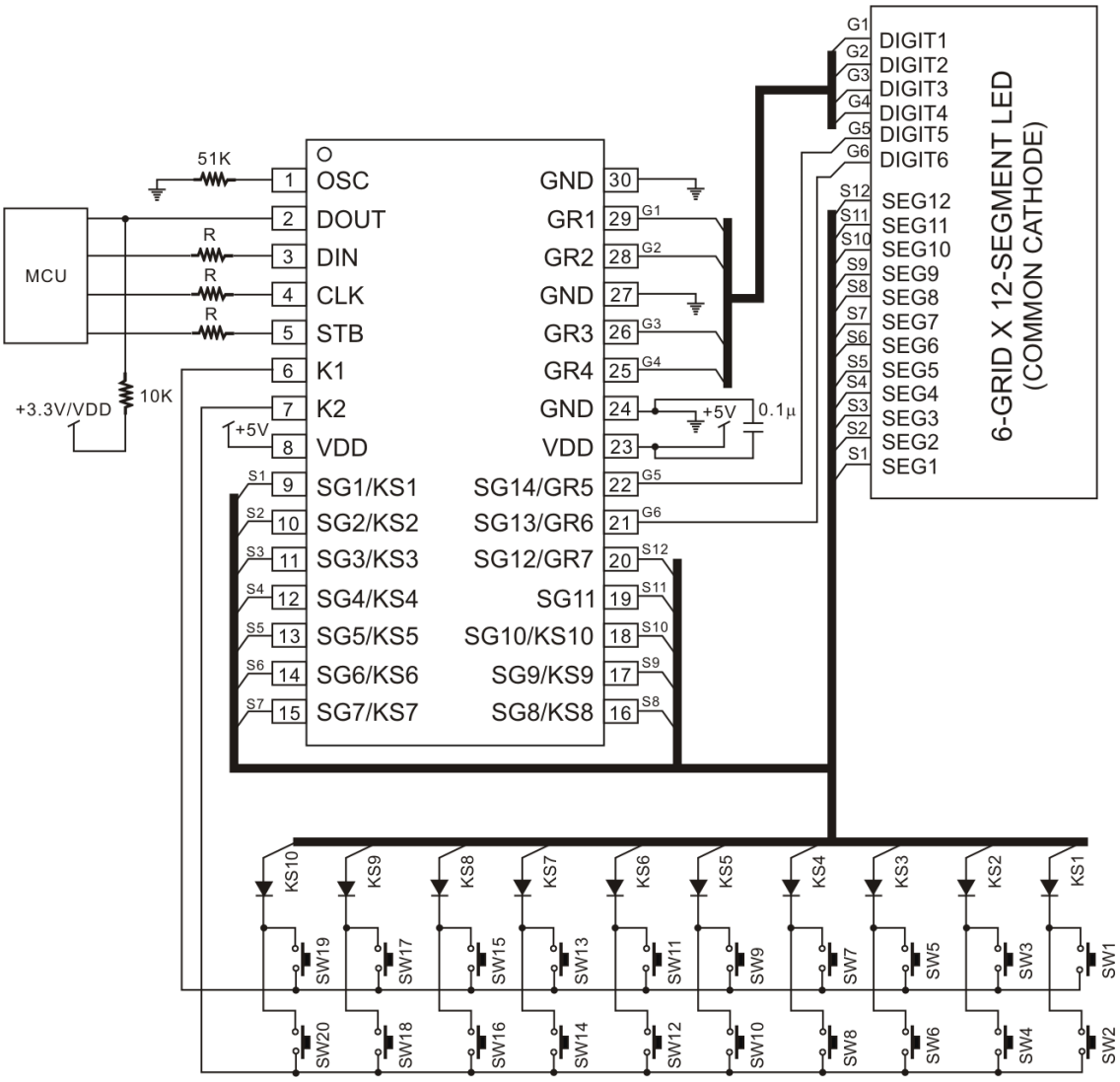
APPLICATIONS

- Micro-computer peripheral device
- VCR set
- Combo set

BLOCK DIAGRAM

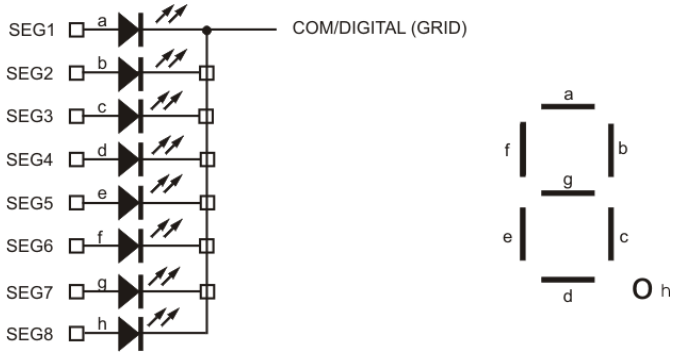


APPLICATION CIRCUIT



Notes:
1. The capacitor (0.1 µF) connected between the GND and the VDD pins must be located as close as possible to the PT6965 chip.
2. The PT6965 power supply is separate from the application system power supply.
3. 10 KΩ ≧ R ≧ 1 KΩ

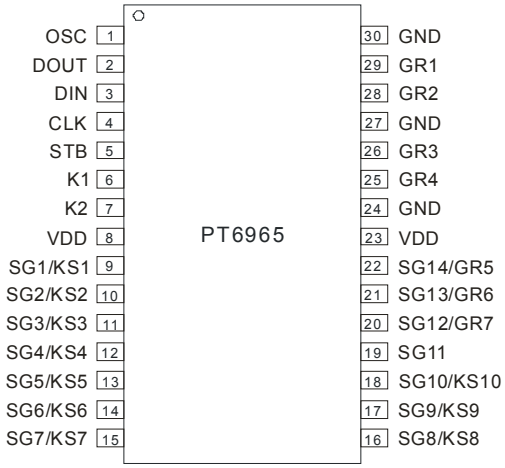
COMMON CATHODE TYPE LED PANEL



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6965-X	30-pin, SSOP, 209mil	PT6965-X
PT6965-TX	30-pin, TSSOP, 173mil	PT6965-TX

PIN CONFIGURATION



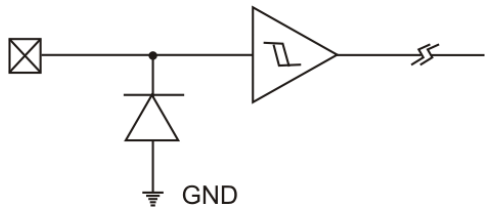
PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	1
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock.	2
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	3
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	4
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is HIGH", CLK is ignored.	5
K1, K2	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor)	6, 7
VDD	-	Power Supply	8, 23
SG1/KS1 ~ SG10/KS10	O	Segment Output Pins (p-channel, open drain) Also acts as the Key Source	9 ~ 18
SG11	O	Segment Output pins (P-Channel, open drain)	19
SG12/GR7 ~ SG14/GR5	O	Segment / Grid Output Pins	20 ~ 22
GND	-	Ground Pin	24, 27, 30
GR4 ~ GR1	O	Grid Output Pins	25, 26, 28, 29

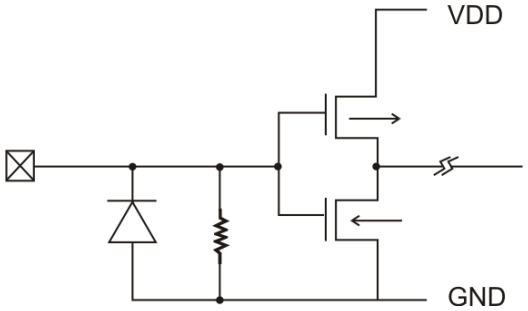
INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.

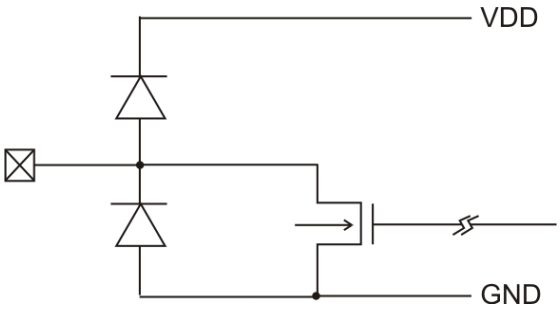
Input Pins: CLK, STB & DIN



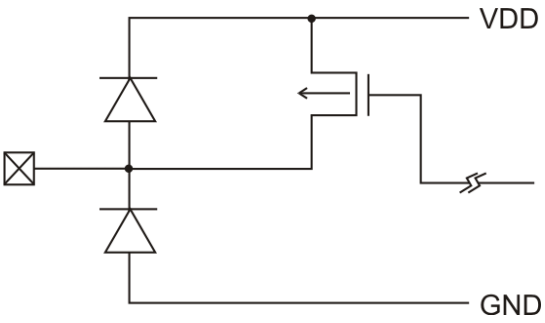
Output Pins: K1 to K2



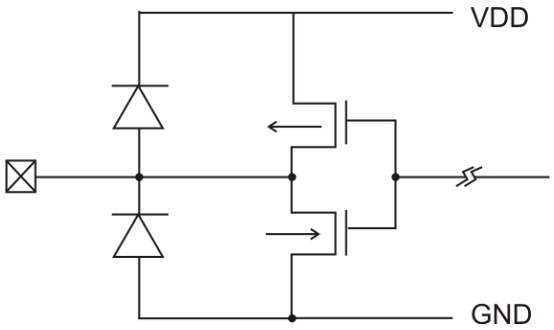
Output Pins: DOUT, GR1 to GR4



Output Pins: SG1 to SG11



Output Pins: SG14/GR5, SG13/GR6 and SG12/GR7



FUNCTION DESCRIPTION

COMMANDS

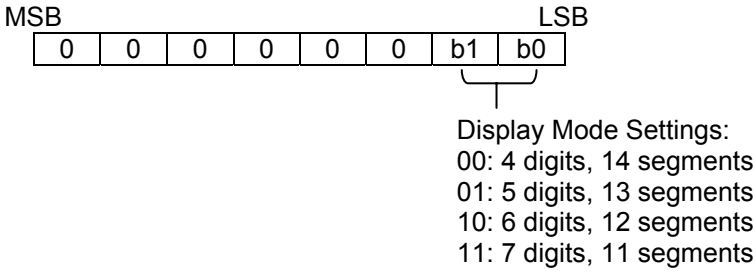
A command is the first byte (b0 to b7) inputted to PT6965 via the DIN Pin after STB Pin has changed from HIGH to LOW State. If for some reason the STB Pin is set to HIGH while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMANDS 1: DISPLAY MODE SETTING COMMANDS

PT6965 provides 4 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6965 via the DIN Pin when STB is LOW. However, for these commands, the bit 3 & bit 8 (b2 to b7) are given a value of 0.

The Display Mode Setting Commands determine the number of segments and grids to be used (14 to 11 segments, 4 to 7 grids). A display command ON must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

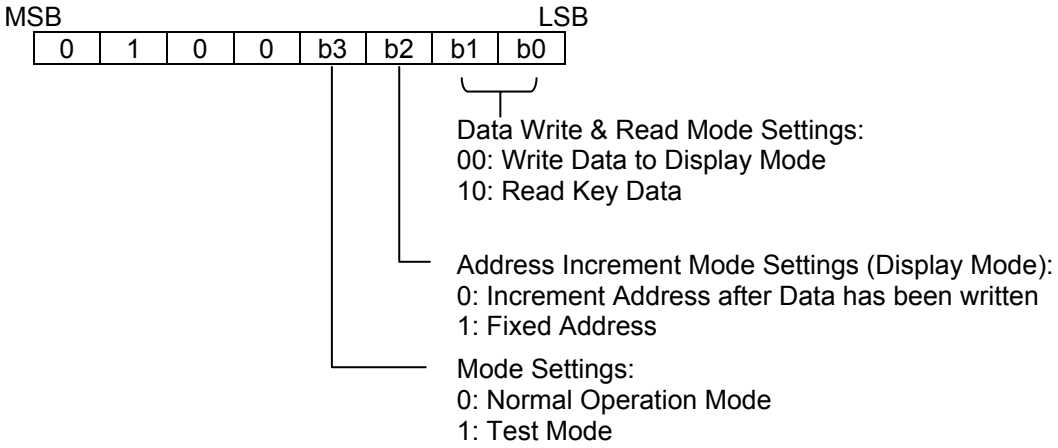
When Power is turned ON, the 7-grid, 11-segment modes is selected.



COMMANDS 2: DATA SETTING COMMANDS

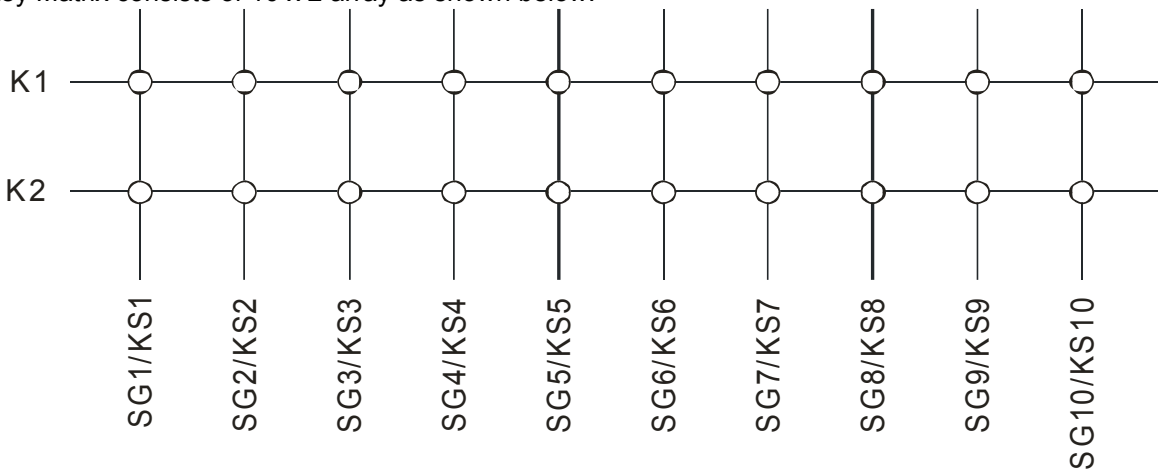
The Data Setting Commands executes the Data Write or Data Read Modes for PT6965. The data Setting Command, the bits 5 and 6 (b4, b5) are given the value of 0, bit 7 (b6) is given the value of 1 while bit 8 (b7) is given the value of 0. Please refer to the diagram below.

When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of 0.



PT6965 KEY MATRIX & KEY INPUT DATA STORAGE RAM

PT6965 Key Matrix consists of 10 x 2 array as shown below:



Each data entered by each key is stored as follows and read by a READ Command, starting from the last significant bit. When the most significant bit of the data (b0) has been read, the least significant bit of the next data (b7) is read.

K1……K2		K1……K2		
SG1/KS1	x	SG2/KS2	x	x
SG3/KS3	x	SG4/KS4	x	x
SG5/KS5	x	SG6/KS6	x	x
SG7/KS7	x	SG8/KS8	x	x
SG9/KS9	x	SG10/KS10	x	x
b0……b1	b2	b3……b4	b5	b6……b7

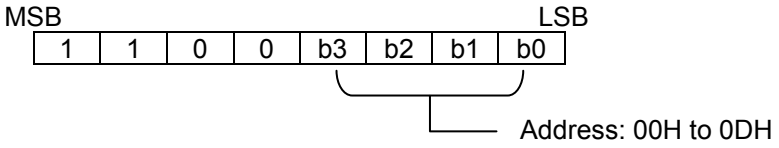
Reading Sequence

Note: b2, b5, b6 and b7 do not care.

COMMANDS 3: ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of 00H to 0DH. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at 00H.

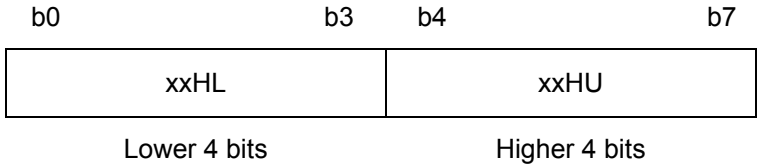
Please refer to the diagram below.



DISPLAY MODE AND RAM ADDRESS

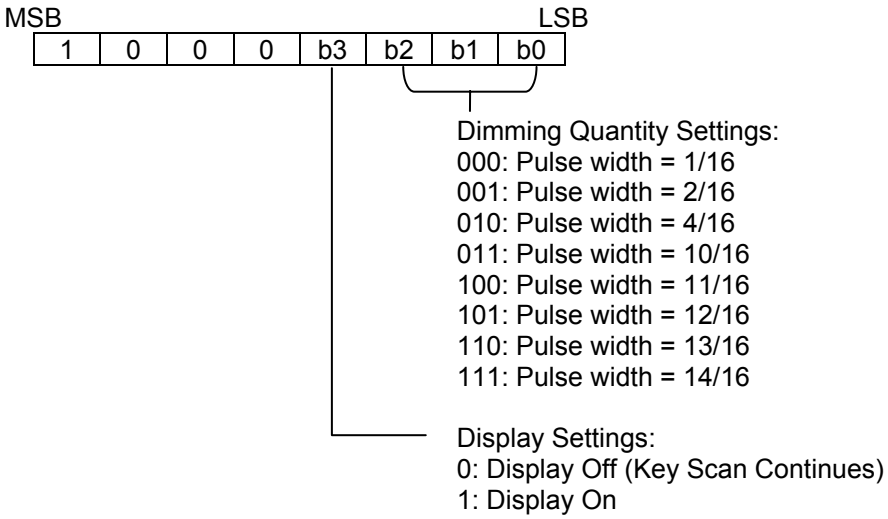
Data transmitted from an external device to PT6965 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM addresses of PT6965 are given below in 8 bits unit.

SG1 SG4	SG5 SG8	SG9 SG12	SG13 SG14	
00HL	00HU	01HL	01HU	DIG1
02HL	02HU	03HL	03HU	DIG2
04HL	04HU	05HL	05HU	DIG3
06HL	06HU	07HL	07HU	DIG4
08HL	08HU	09HL	09HU	DIG5
0AHL	0AHU	0BHL	0BHU	DIG6
0CHL	0CHU	0DHL	0DHU	DIG7

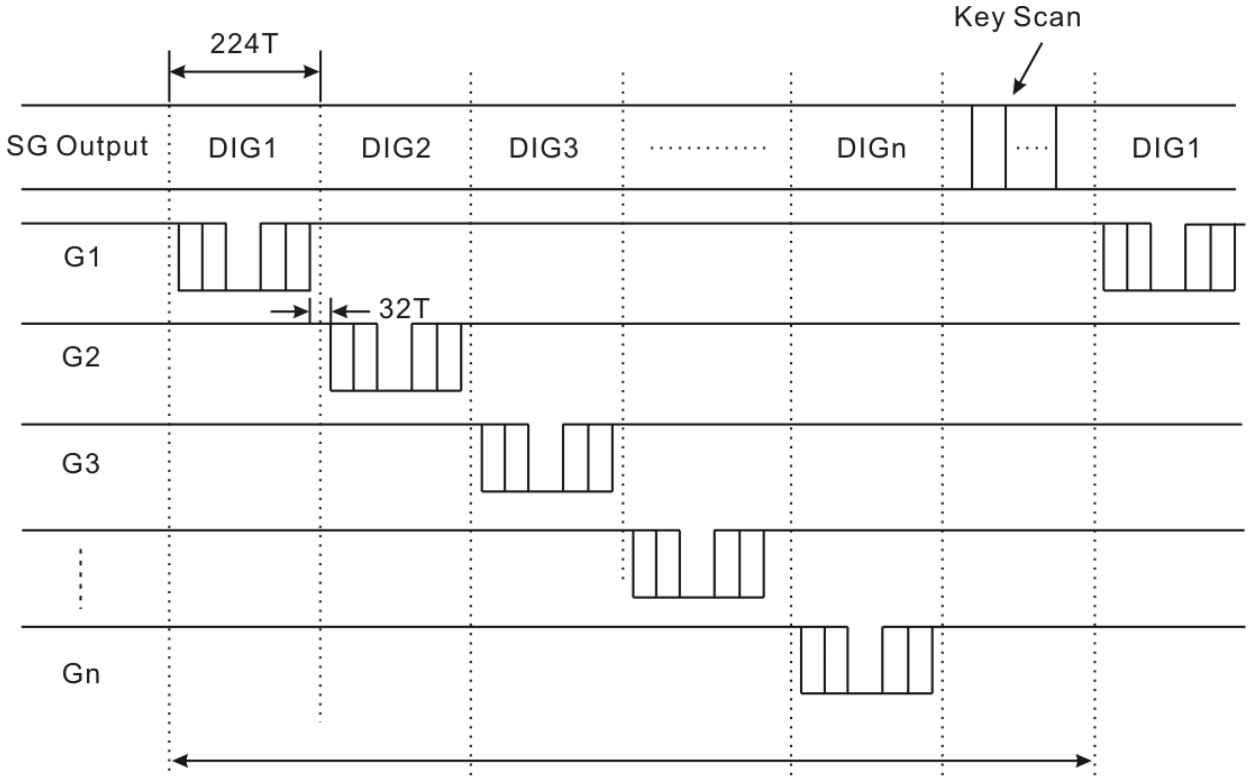


COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF (the key scanning is started).



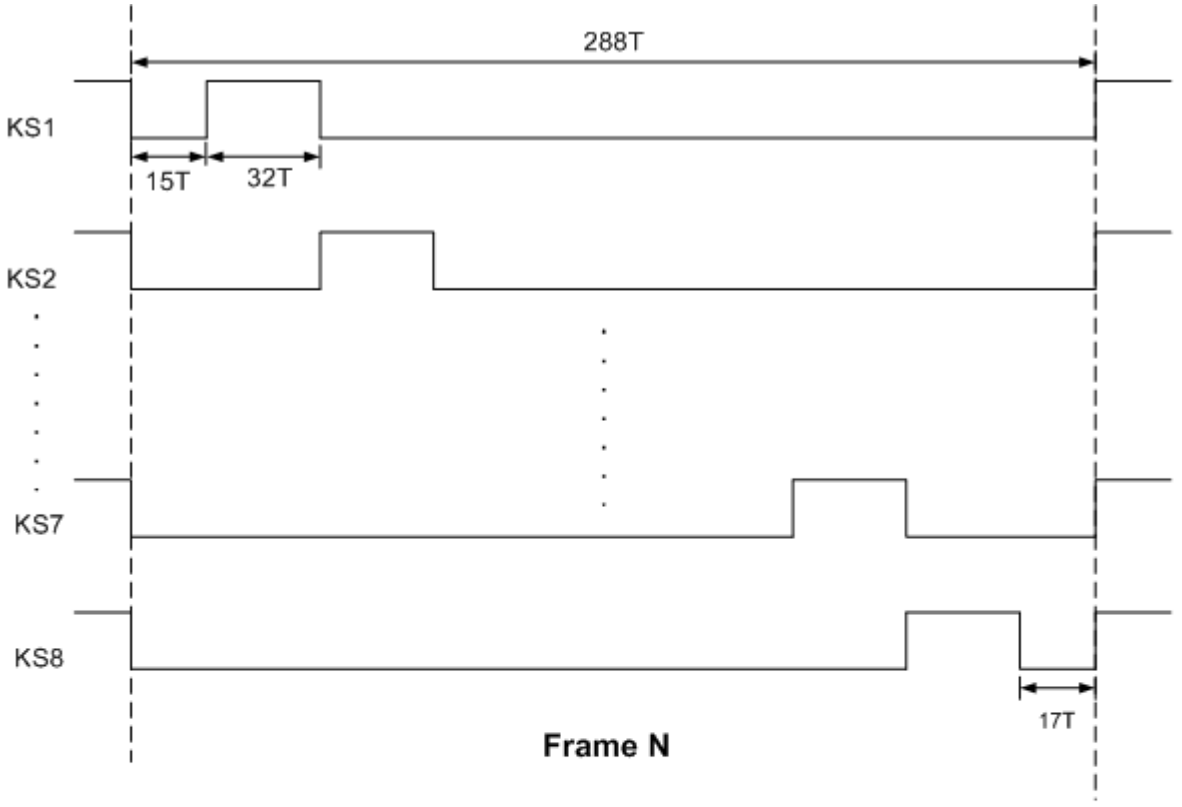
SCANNING AND DISPLAY TIMING

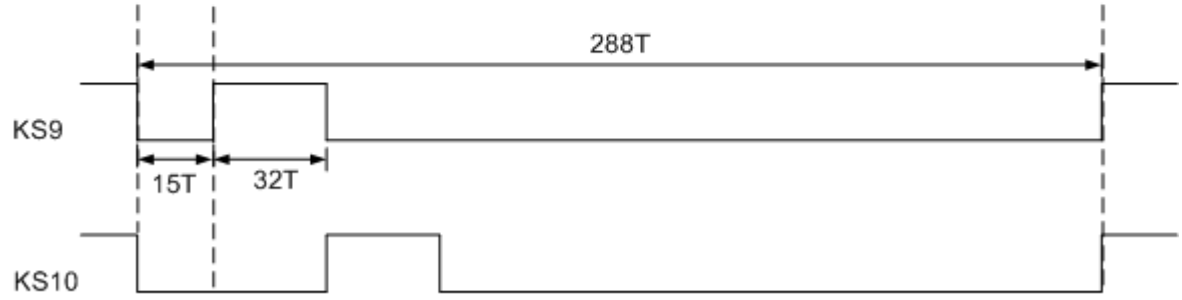


1 Frame = $T_{DISPLAY}$ x (n +1)

T = 1/fosc

KEY SCAN TIMING





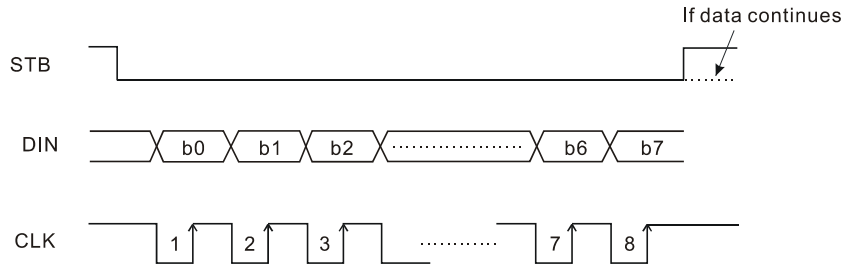
Note: T=1/fosc

Frame (N+1)

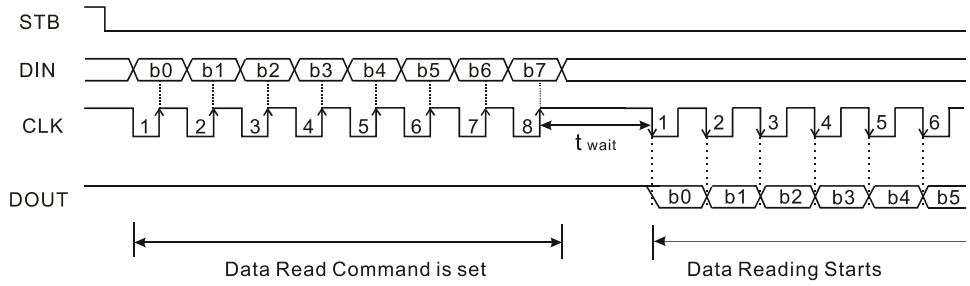
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6965 serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1 KΩ to 10 KΩ) must be connected to DOUT.

Reception (Data/Command Write)



Transmission (Data Read)

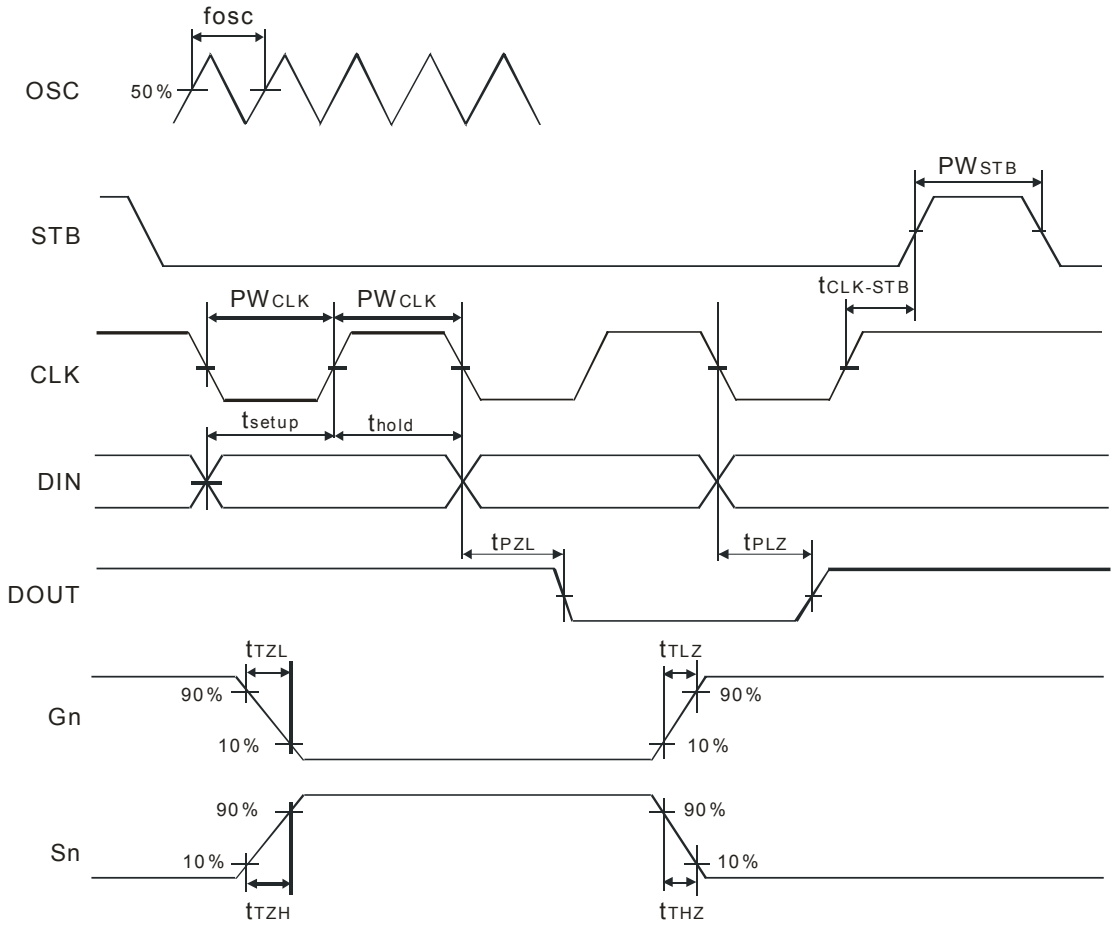


where: twait (waiting time) ≥ 1 μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1 μs.

SWITCHING CHARACTERISTIC WAVEFORM

PT6961 Switching Characteristics Waveform is given below.



where:

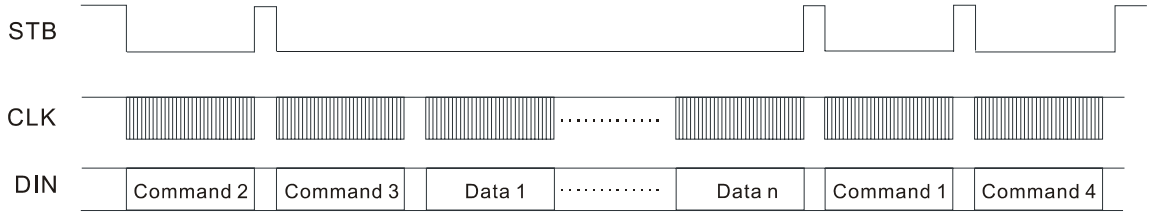
PW_{CLK} (Clock Pulse Width) ≥ 400 ns
t_{setup} (Data Setup Time) ≥ 100 ns
$t_{CLK-STB}$ (Clock - Strobe Time) ≥ 1 µs
t_{TZH} (Rise Time) ≤ 1 µs
fosc = Oscillation Frequency
t_{TZL} ≤ 1 µs (VDD = 5 V)
t_{TZL} ≤ 2 µs (VDD = 3 V)
t_{TLZ} ≤ 10 µs (VDD = 5 V)

PW_{STB} (Strobe Pulse Width) ≥ 1 µs
t_{hold} (Data Hold Time) ≥ 100 ns
t_{THZ} (Fall Time) ≤ 10 µs
t_{PZL} (Propagation Delay Time) ≤ 100 ns (5 V)
t_{PZL} (Propagation Delay Time) ≤ 200 ns (3 V)
t_{PLZ} (Propagation Delay Time) ≤ 300 ns (5 V)
t_{PLZ} (Propagation Delay Time) ≤ 600 ns (3 V)
t_{TLZ} ≤ 20 µs (VDD = 3 V)

Note:
Test Condition Under
t_{THZ} (Pull low resistor = 10 KΩ, Loading capacitor = 300 pF
t_{TLZ} (Pull high resistor = 10 KΩ, Loading capacitor = 300 pF

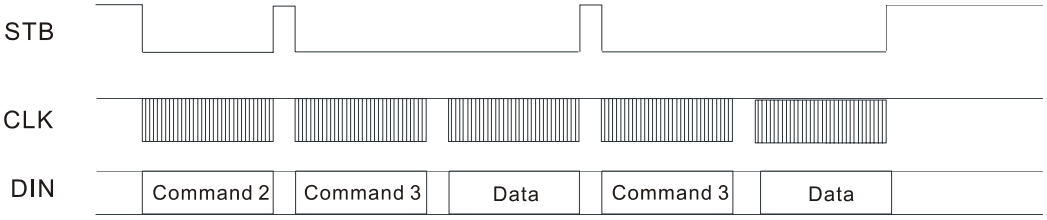
APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.



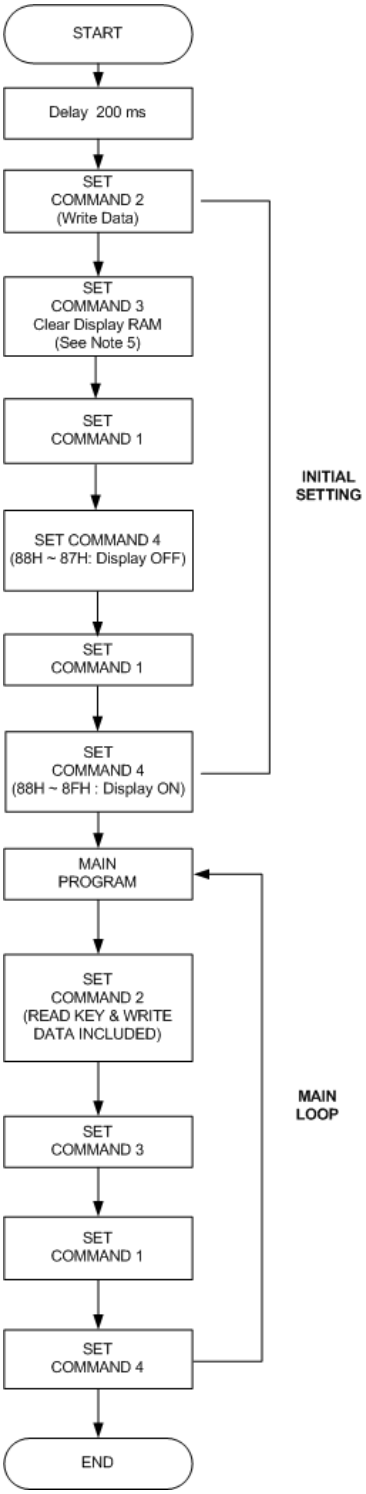
where: Command 1: Display Mode Setting Command
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to n : Transfer Display Data (14 Bytes max.)
Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.



where: Command 2: Data Setting Command
Command 3: Address Setting Command
Data: Display Data

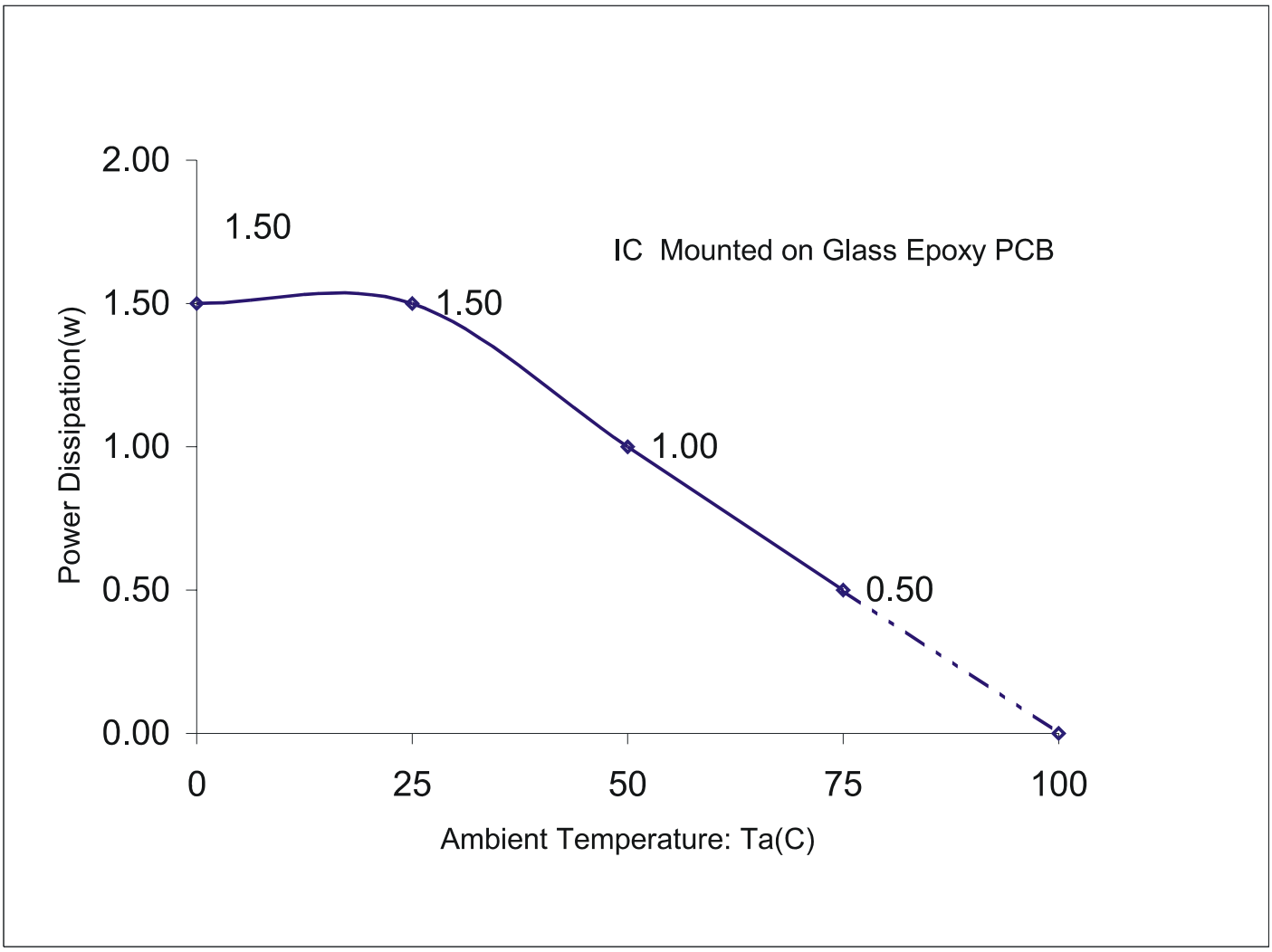
RECOMMENDED SOFTWARE FLOWCHART



Notes:
1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the content of the Display RAM is not defined; thus, it is strongly suggested that the contents of the Display RAM be cleared during the initial setting.

SSOP 30 (300MIL) THERMAL PERFORMANCE IN STILL AIR

JUNCTION TEMPERATURE: 100℃



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta = 25℃, GND = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5 to +7	V
Logic input voltage	VI	-0.5 to VDD+0.5	V
Driver output current	IOLGR	+250	mA
	IOHSG	-50	mA
Maximum driver output current/total	ITOTAL	400	mA
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstg	-65 ~ +150	℃

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Topr = -40 ~ +85℃, GND = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD	3	5	5.5	V
Dynamic Current (see Note1)	IDDdyn	-	-	5	mA
High-level input voltage	VIH	2.4	-	VDD	V
Low-level input voltage	VIL	0	-	1	V

Note:
1. Test Condition: Set Display Control Commands = 80 H (Display Turn OFF State & under no load).

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD = 5 V, GND = 0 V, Ta = 25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-level output current	IOHSG(1)	VO = VDD -2 V SG1 to SG11, SG12/GR7	-20	-25	-40	mA
	IOHSG(2)	VO = VDD -3 V SG1 to SG11, SG12/GR7	-25	-30	-50	mA
Low-level output current	IOLGR	VO = 0.3 V GR1 to GR6, SG12/GR7	100	140	-	mA
Low-level output current	IOLDOUT	VO = 0.4V	4	-	-	mA
Segment high-level output current tolerance	ITOLSG	VO = VDD -3 V SG1 to SG11, SG12/GR7	-	-	±5	%
High-level input voltage	VIH	-	2.4	-	3.3/VDD	V
Low-level input voltage	VIL	-	0	-	0.8	V
Oscillation frequency	fosc	R = 51 KΩ	350	500	650	KHz
K1 to K2 pull down resistor	RKN	K1 to K2 VDD = 5 V	40	-	100	KΩ

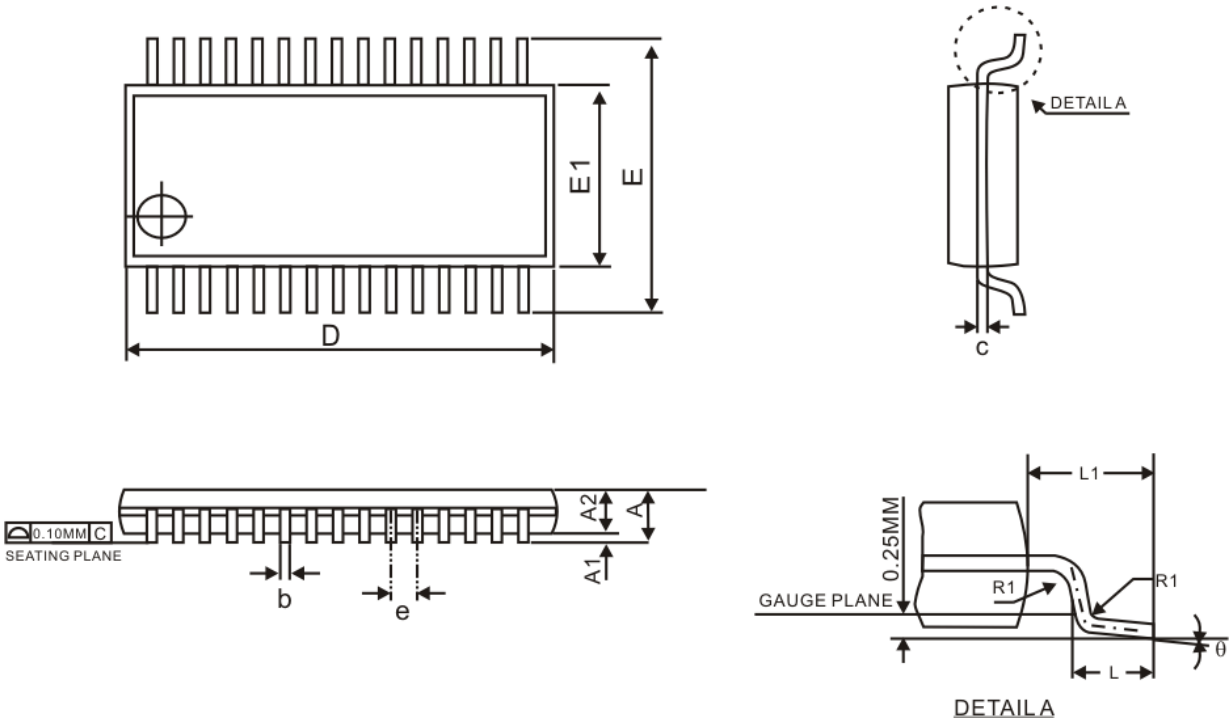
ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD = 3 V, GND = 0 V, Ta = 25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
High-level output current	IOHSG	VO = VDD -2V SG1 to SG11, SG12/GR7	-9	-12	-20	mA
Low-level output current	IOLGR	VO = 0.3 V GR1 to GR6, SG12/GR7	80	100	-	mA
Low-level output current	IOLDOUT	VO = 0.4 V	2	-	-	mA
Segment high-level output current tolerance	ITOLSG	VO = VDD -2 V SG1 to SG11, SG12/GR7	-	-	±5	%
High-level input voltage	VIH	-	0.8VDD	-	VDD	V
Low-level input voltage	VIL	-	0	-	0.3	V
Oscillation frequency	fosc	R = 33 KΩ	350	500	650	KHz
K1 to K2 pull down resistor	RKN	K1 to K2 VDD = 3 V	90	-	180	KΩ

PACKAGE INFORMATION

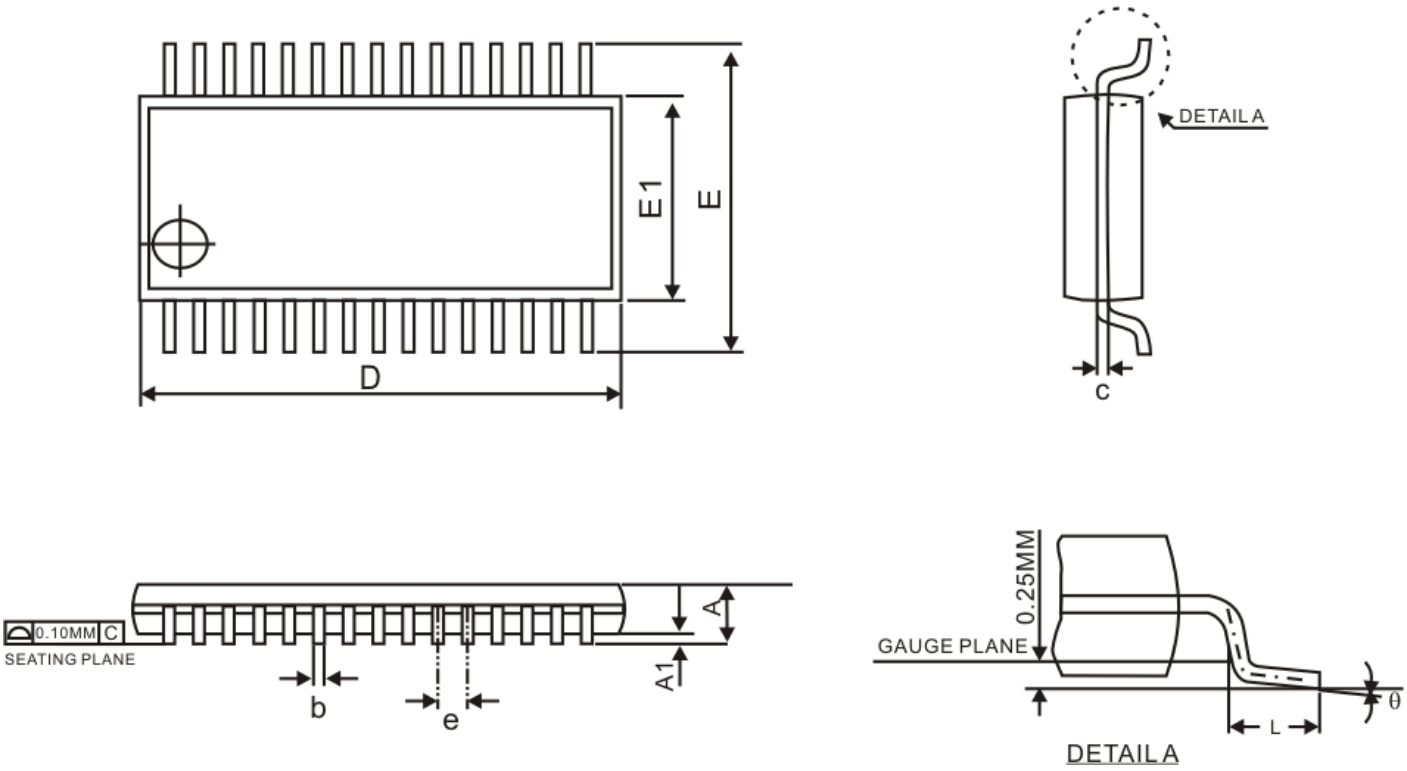
30 PINS, SSOP, 209 MIL



Symbol	Min.	Nom.	Max.
A	-	-	2.0
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	0.15	0.25
e		0.65 BSC	
D	9.90	10.20	10.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
L	0.55	0.75	0.95
L1		1.25 REF	
R1	0.09	-	-
θ	0°	4°	8°

Notes:
1. All dimensions are in MILLMETERS.
2. Refer to JEDEC MO-150 AJ.

30PINS, TSSOP, 173MIL



Symbol	Min.	Nom.	Max.
A	-	-	1.20
A1	0.05	-	-
b	0.15	0.20	0.25
c	0.09	-	0.20
e		0.50 BSC	
D	7.70	7.80	8.15
E		6.40 BSC	
E1	4.20	4.40	4.60
L	0.55	0.75	0.95
θ	0°	4°	8°

Notes:
1. All dimensions are in MILLMETERS.
2. Refer to JEDEC MO-153 BC-1.

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
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