

## Features

- Low  $R_{DS(ON)}$ :
  - $65m\Omega$  @  $V_{GS} = -10V$
  - $115m\Omega$  @  $V_{GS} = -4.5V$
- Low Input/Output Leakage
- **Lead Free By Design/RoHS Compliant (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **"Green" Device (Note 4)**

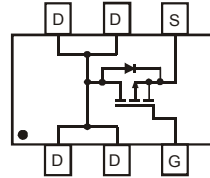
## Mechanical Data

- Case: SOT-26
- Case Material - Molded Plastic. UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020D
- Terminals: Finish - Matte Tin Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Marking Information: See Page 4
- Ordering Information: See page 4
- Weight: 0.008 grams (approximate)



TOP VIEW

SOT-26


 TOP VIEW  
Internal Schematic

## Maximum Ratings @ $T_A = 25^\circ C$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-30	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (Note 1) Continuous	$I_D$	-4.0 -3.0	A
		$T_A = 25^\circ C$ $T_A = 70^\circ C$	
Pulsed Drain Current (Note 2)	$I_{DM}$	-14	A

## Thermal Characteristics

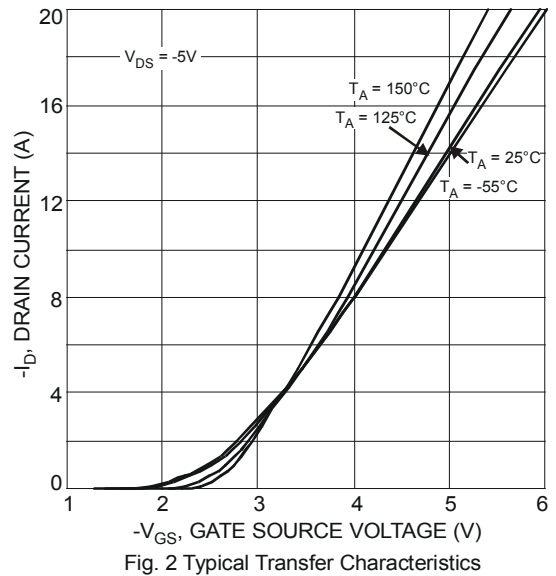
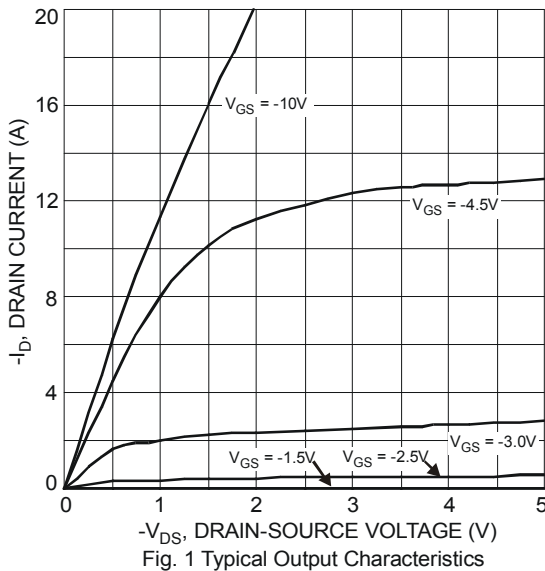
Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 1)	$P_D$	1.25	W
Thermal Resistance, Junction to Ambient (Note 1); Steady-State	$R_{\theta JA}$	100	$^\circ C/W$
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ C$

- Notes:
1. Device mounted on 1"x1", FR-4 PC board on 0.1in.<sup>2</sup> pads on 2 oz. Copper pads and test pulse width  $t \leq 10s$ .
  2. Repetitive Rating, pulse width limited by junction temperature.
  3. No purposefully added lead.
  4. Diodes Inc's "Green" policy can be found on our website at [http://www.diodes.com/products/lead\\_free/index.php](http://www.diodes.com/products/lead_free/index.php).

**Electrical Characteristics** @ $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>STATIC PARAMETERS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	-30	—	—	V	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	-1	$\mu\text{A}$	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}$ $T_J = 25^\circ\text{C}$
Gate-Body Leakage Current	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	—	-2.1	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
On State Drain Current (Note 5)	$I_{D(ON)}$	-15	—	—	A	$V_{GS} = -4.5\text{V}, V_{DS} = -5\text{V}$
Static Drain-Source On-Resistance (Note 5)	$R_{DS(ON)}$	—	56 98	65 115	m $\Omega$	$V_{GS} = -10\text{V}, I_D = -4.0\text{A}$ $V_{GS} = -4.5\text{V}, I_D = -3.0\text{A}$
Forward Transconductance (Note 5)	$g_{FS}$	—	5.3	—	S	$V_{DS} = -10\text{V}, I_D = -4.0\text{A}$
Diode Forward Voltage (Note 5)	$V_{SD}$	—	0.79	-1.2	V	$I_S = -1.7\text{A}, V_{GS} = 0\text{V}$
<b>DYNAMIC PARAMETERS (Note 6)</b>						
Input Capacitance	$C_{iss}$	—	336	—	pF	$V_{DS} = -25\text{V}, V_{GS} = 0\text{V}$ $f = 1.0\text{MHz}$
Output Capacitance	$C_{oss}$	—	70	—	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	49	—	pF	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Gate Resistance	$R_G$	—	4.6	—	$\Omega$	
<b>SWITCHING CHARACTERISTICS</b>						
Total Gate Charge	$Q_g$	—	4.0 7.8	—	nC	$V_{DS} = -15\text{V}, V_{GS} = -4.5\text{V}, I_D = -5.0\text{A}$ $V_{DS} = -15\text{V}, V_{GS} = -10\text{V}, I_D = -5.0\text{A}$
Gate-Source Charge	$Q_{gs}$	—	1.0	—		$V_{DS} = -15\text{V}, V_{GS} = -4.5\text{V}, I_D = -5.0\text{A}$
Gate-Drain Charge	$Q_{gd}$	—	2.5	—		$V_{DS} = -15\text{V}, V_{GS} = -4.5\text{V}, I_D = -5.0\text{A}$
Turn-On Delay Time	$t_{d(on)}$	—	6.0	—	ns	$V_{DS} = -15\text{V}, V_{GS} = -10\text{V},$ $I_D = -1.0\text{A}, R_G = 6.0\Omega$
Rise Time	$t_r$	—	5.0	—		
Turn-Off Delay Time	$t_{d(off)}$	—	17.6	—		
Fall Time	$t_f$	—	9.5	—		

Notes: 5. Test pulse width  $t = 300\mu\text{s}$ .  
6. Guaranteed by design. Not subject to production testing.



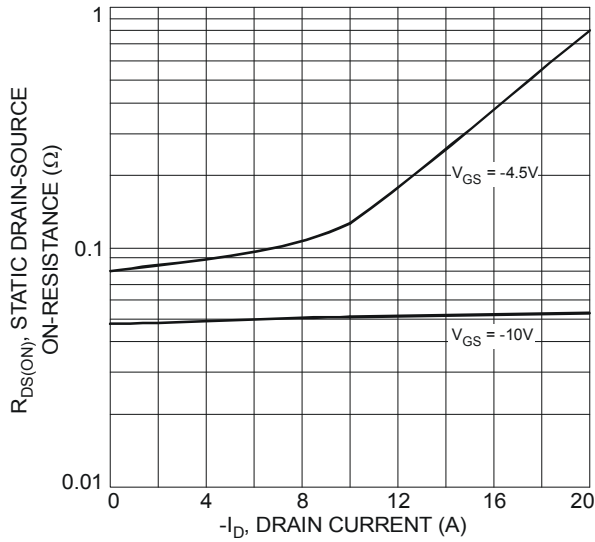


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

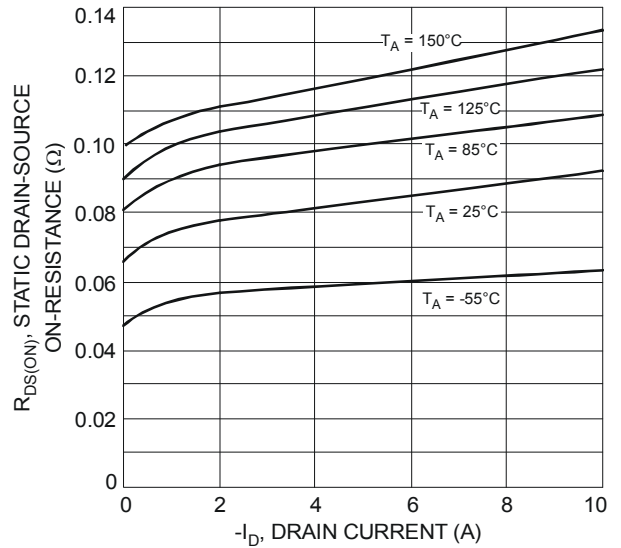


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

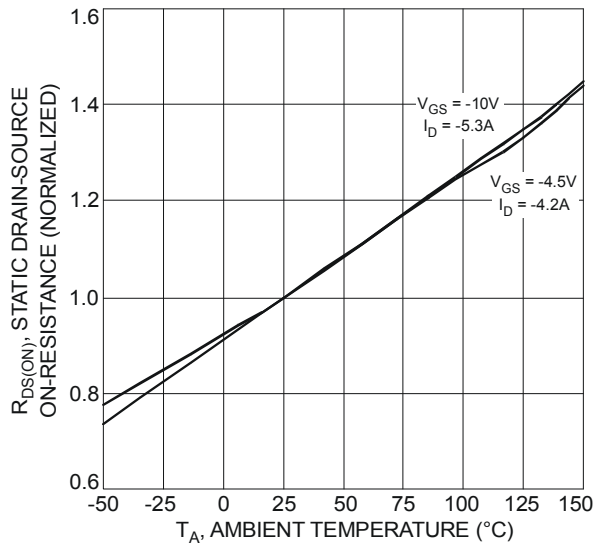


Fig. 5 On-Resistance Variation with Temperature

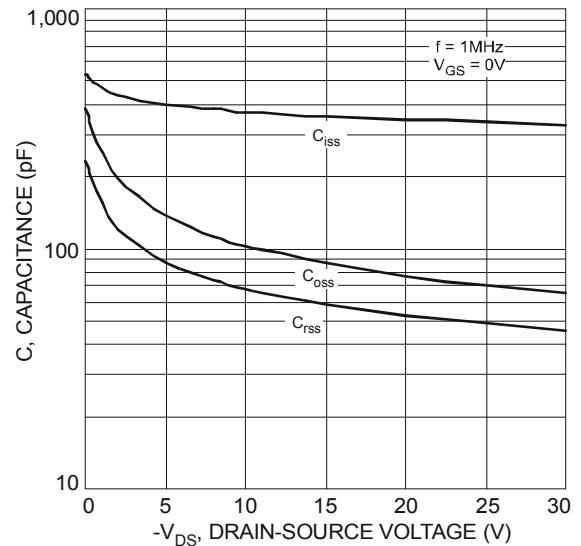


Fig. 6 Typical Capacitance

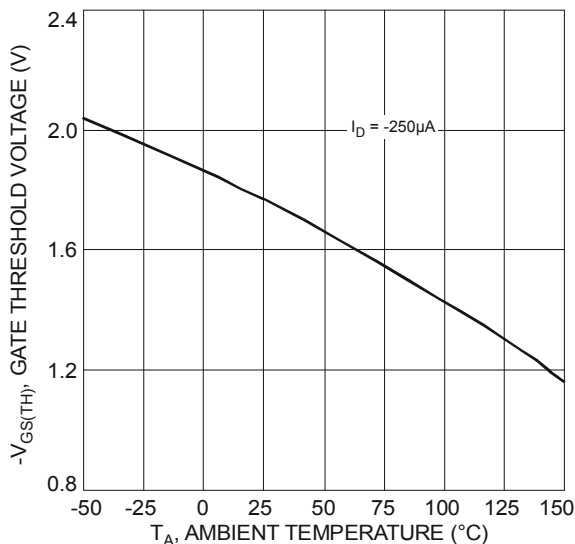


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

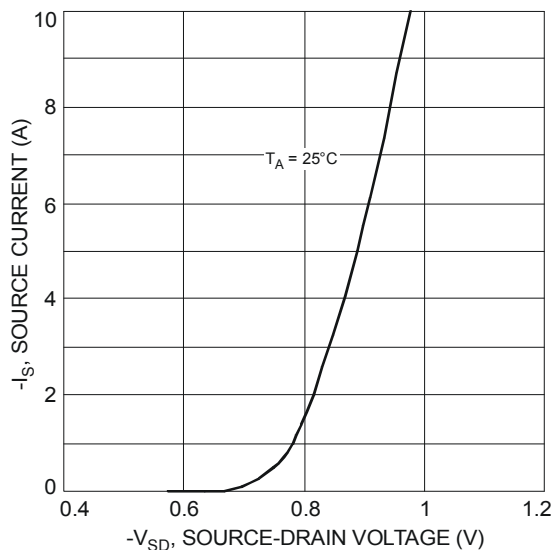


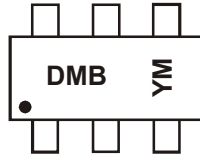
Fig. 8 Diode Forward Voltage vs. Current

**Ordering Information** (Note 7)

Part Number	Case	Packaging
DMP3098LDM-7	SOT-26	3000/Tape & Reel

Notes: 7. For packaging details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

**Marking Information**

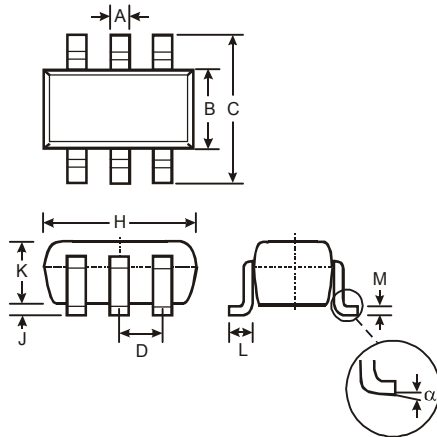


DMB = Product Type Marking Code  
 YM = Date Code Marking  
 Y = Year (ex: V = 2008)  
 M = Month (ex: 9 = September)

Date Code Key

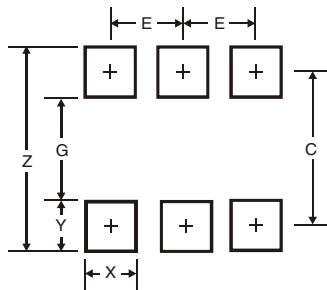
Year	2008	2009	2010	2011	2012	2013	2014	2015				
Code	V	W	X	Y	Z	A	B	C				
Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Package Outline Dimensions**



SOT-26			
Dim	Min	Max	Typ
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	—	—	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
$\alpha$	0°	8°	—
All Dimensions in mm			

**Suggested Pad Layout**



Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C	2.40
E	0.95

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