

High-performance Regulator IC Series for PCs

# Termination Regulators for DDR-SDRAMs

**BD3537F**

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**●Description**

BD3537F is a termination regulator compatible with JEDEC DDR-SDRAM, which functions as a linear power supply incorporating an N-channel MOSFET and provides a sink/source current capability up to 1.8A respectively. A built-in high-speed OP-AMP specially designed offers an excellent transient response. Requires 5.0 volts as a bias power supply to drive the N-channel MOSFET. For BD3537F, ceramic capacitor can be used as output capacitor. Thus, the BD3537F is designed to enable significant package profile downsizing as the total regulator part.

**●Features**

- 1) Incorporates a push-pull power supply for termination (VTT)
- 2) Incorporates an enabler
- 3) Incorporates an undervoltage lockout (UVLO)
- 4) Employs SOP8 package
- 5) Incorporates a thermal shutdown protector (TSD)
- 6) Compatible with Dual Channel (DDR-II)
- 7) Operates with input voltage from 4.75 to 5.25 volts
- 8) Incorporates soft start function

**●Use**

Power supply for DDR I/II - SDRAM

●ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits	Unit
Input Voltage	VCC	7 <sup>*1</sup>	V
REF Input Voltage	REF	7 <sup>*1</sup>	V
Termination Input Voltage	VTT_IN	7 <sup>*1</sup>	V
Output Current	ITT	3	A
Power Dissipation1	Pd1	560 <sup>*2</sup>	mW
Power Dissipation2	Pd2	690 <sup>*3</sup>	mW
Operating Temperature Range	Topr	-30~+100	°C
Storage Temperature Range	Tstg	-55~+150	°C
Maximum Junction Temperature	Tjmax	+150	°C

\*1 Should not exceed Pd.

\*2 Reduced by 4.48mW for each increase in Ta of 1°C over 25°C (no heat sink).

\*3 Reduced by 5.52mW for each increase in Ta of 1°C over 25°C (when mounted on 70mm x 70mm x 1.6mm Glass-epoxy PCB).

●OPERATING CONDITIONS (Ta=25°C)

Parameter	Symbol	MIN	MAX	Unit
Input Voltage	VCC	4.75	5.25	V
Termination Input Voltage	VTT_IN	1.746	1.854	V
Reference Voltage	VEN	0.6	1.6	V

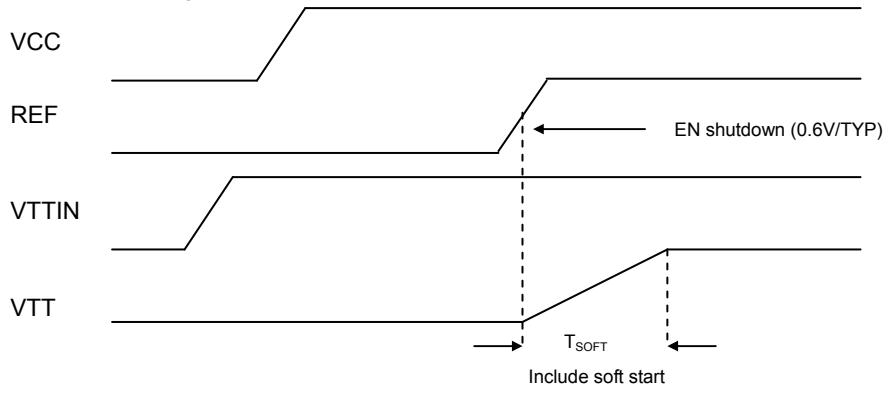
★ No radiation-resistant design is adopted for the present product.

●ELECTRICAL CHARACTERISTICS (unless otherwise noted, Ta=25°C, VCC=5V, REF=0.9V, VTT\_IN=1.8V)

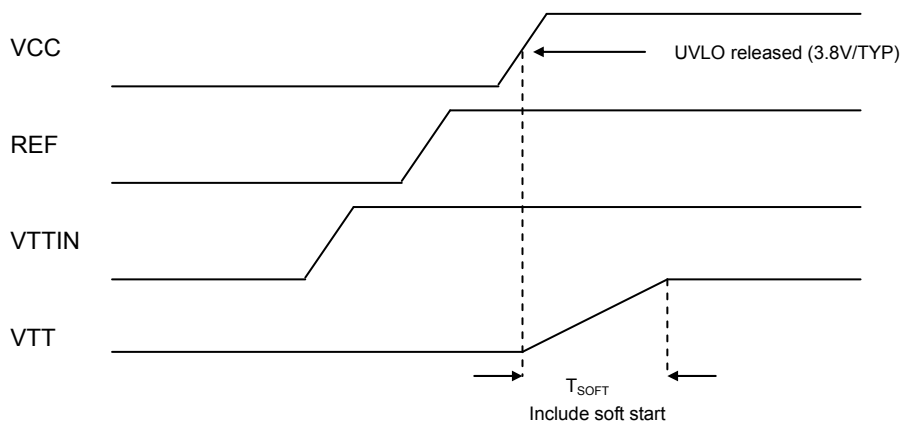
Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Standby Current	IST	-	50	90	uA	REF<0.15V(Shutdown)
Bias Current	ICC	-	1	2.5	mA	REF=0.9V
[Termination]						
Termination Output Voltage 1	VTT1	REF-20m	REF	REF+20m	V	ITT=0A
Termination Output Voltage 2	VTT2	REF-20m	REF	REF+20m	V	ITT=-1.8A to 1.8A
Source Current	ITT+	1.8	-	-	A	
Sink Current	ITT-	-	-	-1.8	A	
Upper Side ON Resistance 1	HRON1	-	0.3	0.5	Ω	
Lower Side ON Resistance 1	LRON1	-	0.3	0.5	Ω	
[UVLO block]						
UVLO Threshold Voltage	VUVLO	3.5	3.8	4.1	V	VCC : sweep up
UVLO Hysteresis Voltage	ΔVUVLO	100	160	220	mV	VCC : sweep down
[Enable block]						
EN-ON Voltage	V <sub>ENH</sub>	0.6	-	-	V	
EN-OFF Voltage	V <sub>ENL</sub>	-	-	0.15	V	

● Soft start function

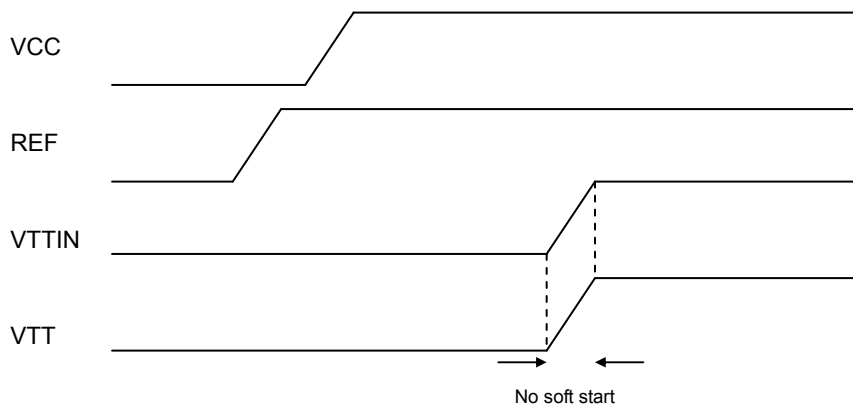
(a) when input REF voltage



(b) when input VCC voltage



(c) when input VTTIN voltage



※ $T_{SOFT} \leq 1\text{msec}$

●Reference Data

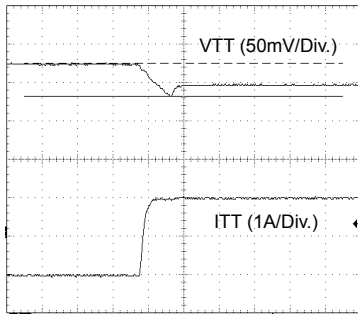


Fig.1 DDRI (-1A→1A)

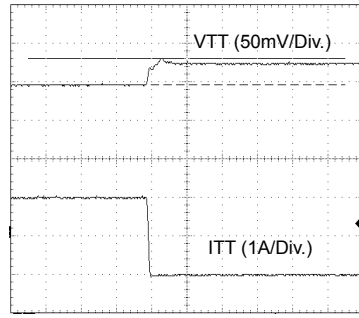


Fig.2 DDRI (1A→-1A)

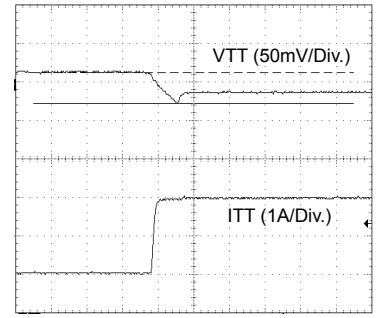


Fig.3 DDR II (-1A→1A)

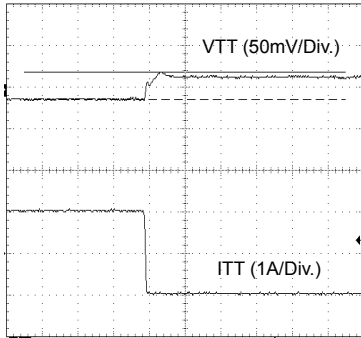


Fig.4 DDR II (-1A→1A)

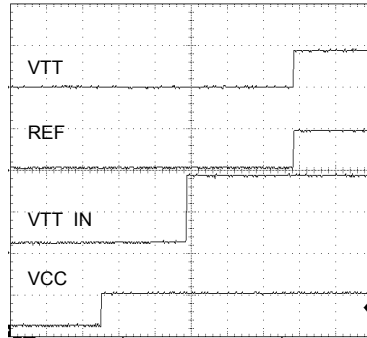


Fig.5 Input Sequence 1

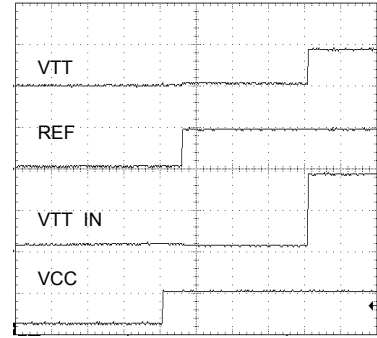


Fig.6 Input Sequence 2

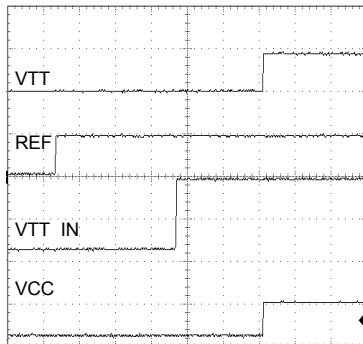


Fig.7 Input Sequence 3

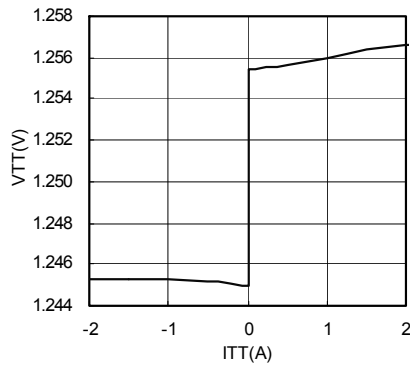


Fig.8 ITT-VTT (DDR-I)

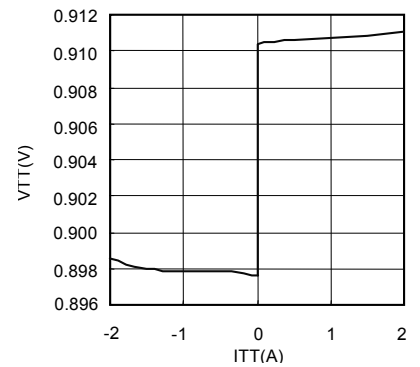


Fig.9 ITT-VTT (DDR-II)

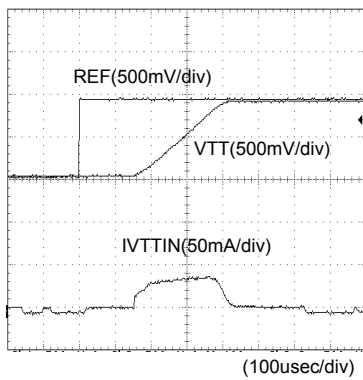
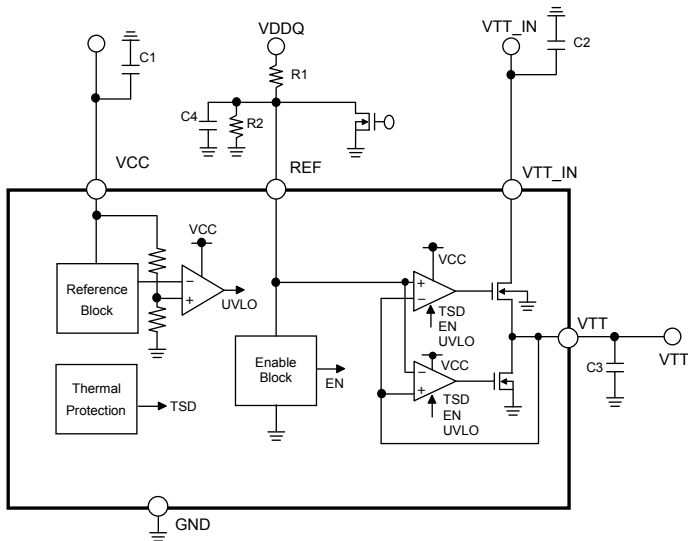
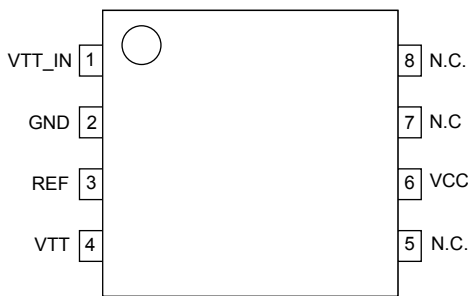


Fig.10 Soft start

●BLOCK DIAGRAM



●PIN CONFIGURATION



●PIN FUNCTION

PIN No.	PIN name	PIN Function
1	VTT_IN	Termination power supply pin
2	GND	Ground pin
3	REF	Reference voltage output pin
4	VTT	Termination output pin
5	N.C.	Non connection
6	VCC	VCC Pin
7	N.C.	Non connection
8	N.C.	Non connection

●Description of operations

• VCC

In BD3537F, an independent power input pin is provided for an internal circuit operation of the IC. This is used to drive the amplifier circuit of the IC, and its maximum current rating is 2.5mA. The power supply voltage is 5.0 volts. It is recommended to connect a bypass capacitor of 1μF or so to VCC.

• VTT\_IN

VTT\_IN is a power supply input pin for VTT output. Voltage in the range up to 1.8 volts may be supplied to this VTT\_IN terminal, but care must be taken to the current limitation due to on-resistance of the IC and the change in allowable loss due to input/output voltage difference.

Higher impedance of the voltage input at VTT\_IN may result in oscillation or degradation in ripple rejection, which must be noted. To VTT\_IN terminal, it is recommended to use a 10μF capacitor characterized with less change in capacitance. But it may depend on the characteristics of the power supply input and the impedance of the pc board wiring, which must be carefully checked before use.

• VTT

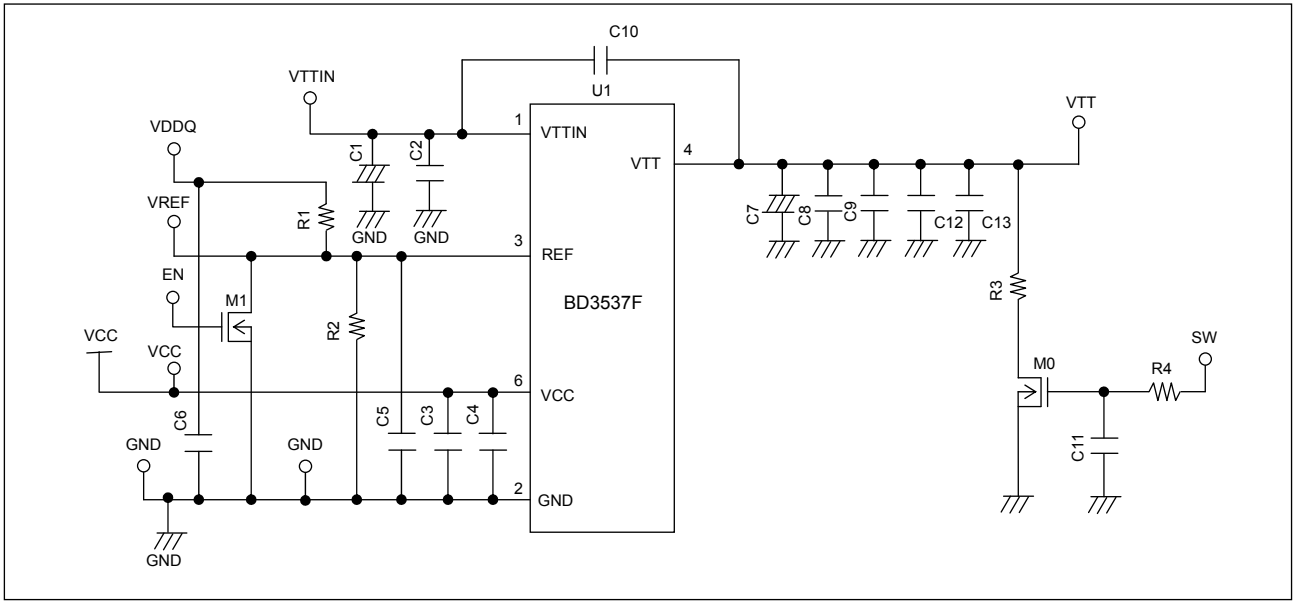
A DDR memory termination output pin. BD3537F has a sink/source current capability of ±1.8A respectively. The output voltage is same as REF voltage. VTT output is turned to OFF when VCC UVLO or thermal shutdown protector is activated with EN pin level becomes EN-OFF voltage or below. Do not fail to connect a capacitor to VTT output pin for a loop gain phase compensation and a reduction in output voltage variation in the event of sudden change in load. Insufficient capacitance may cause an oscillation. High ESR (Equivalent Series Resistance) of the capacitor may result in increase in output voltage variation in the event of sudden change in load. It is recommended to use a 10 μF ceramic capacitor (X5R or X7R), though it depends on ambient temperature and other conditions. A low ESR ceramic capacitor may reduce a loop gain phase margin and may cause an oscillation, which may be improved by connecting a resistor in series with the OS-capacitor (several-hundred μF).

• REF

With an input of 0.6 volts or higher, the level at REF pin turns to “High” to provide VTT output. If the input is lowered to 0.15 volts or less, the level at REF pin turns to “Low” and VTT status turns to Hi-Z.

● Evaluation Board

■ Evaluation Board circuit



■ Evaluation Board Application Components

Part No	Value	Company	Parts Name
U1		ROHM	BD3537F
M0			
M1			
C1			
C2	0.1uF	KYOCERA	CM05B104K10A
C3	0.1uF	KYOCERA	CM05B104K10A
C4			
C5	1uF	KYOCERA	CM05B105K10A
C6			
C7			

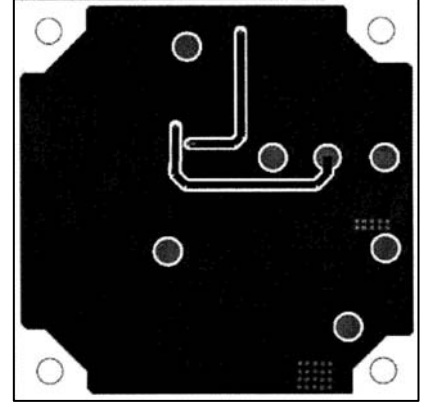
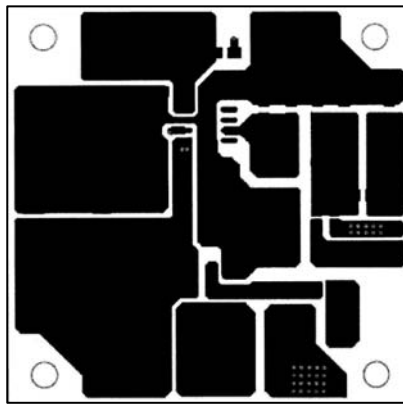
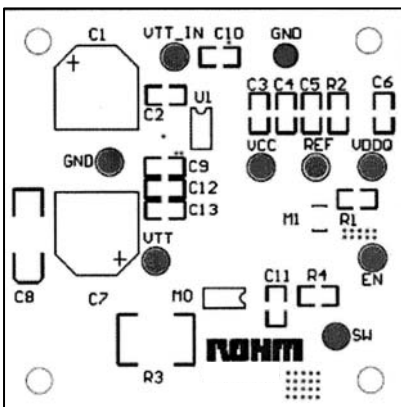
Part No	Value	Company	Parts Name
C8			
C9	10uF	KYOCERA	CM316B106M10A
C10			
R1	100kΩ	ROHM	MCR03
R2	100kΩ	ROHM	MCR03
R3			
R4			
R5			
R6			

■ BD3537F (SOP8) Evaluation Board Layout

Silk Screen

TOP Layer

Bottom Layer



## ● Heat loss

Thermal design must be conducted with the operation under the conditions listed below (which are the guaranteed temperature range requiring consideration on appropriate margins etc.):

1. Ambient temperature  $T_a$ : 100°C or lower
2. Chip junction temperature  $T_j$ : 150°C or lower

The chip junction temperature  $T_j$  can be considered as follows. See Page 9/9 for  $\theta_{ja}$ .

Most of heat loss in BD3537F occurs at the output N-channel FET. The power lost is determined by multiplying the voltage between  $V_{IN}$  and  $V_o$  by the output current. As this IC employs the power PKG, the thermal derating characteristics significantly depends on the pc board conditions. When designing, care must be taken to the size of a pc board to be used.

Power dissipation (W) = {Input voltage ( $V_{TT\_IN}$ ) – Output voltage ( $V_{TT \rightleftharpoons REF}$ )} $\times I_o$  (Ave)

If  $V_{TT\_IN} = 1.8$ volts,  $REF=0.9$ volts, and  $I_o$  (Ave)=0.5 A, for instance, the power dissipation is determined as follows:

Power dissipation (W) = {1.8 (V) – 0.9 (V)}  $\times$  0.5 (A) = 0.4 (W)

## ● NOTE FOR USE

### 1. Absolute maximum ratings

For the present product, thoroughgoing quality control is carried out, but in the event that applied voltage, working temperature range, and other absolute maximum rating are exceeded, the present product may be destroyed. Because it is unable to identify the short mode, open mode, etc., if any special mode is assumed, which exceeds the absolute maximum rating, physical safety measures are requested to be taken, such as fuses, etc.

### 2. GND potential

Bring the GND terminal potential to the minimum potential in any operating condition.

### 3. Thermal design

Consider allowable loss (Pd) under actual working condition and carry out thermal design with sufficient margin provided.

### 4. Terminal-to-terminal short-circuit and erroneous mounting

When the present IC is mounted to a printed circuit board, take utmost care to direction of IC and displacement. In the event that the IC is mounted erroneously, IC may be destroyed. In the event of short-circuit caused by foreign matter that enters in a clearance between outputs or output and power-GND, the IC may be destroyed.

### 5. Operation in strong electromagnetic field

The use of the present IC in the strong electromagnetic field may result in maloperation, to which care must be taken.

### 6. Built-in thermal shutdown protection circuit

The present IC incorporates a thermal shutdown protection circuit (TSD circuit). The working temperature is 175°C (standard value) and has a -15°C (standard value) hysteresis width. When the IC chip temperature rises and the TSD circuit operates, the output terminal is brought to the OFF state. The built-in thermal shutdown protection circuit (TSD circuit) is first and foremost intended for interrupt IC from thermal runaway, and is not intended to protect and warrant the IC. Consequently, never attempt to continuously use the IC after this circuit is activated or to use the circuit with the activation of the circuit premised.

### 7. Capacitor across output and GND

In the event a large capacitor is connected across output and GND, when  $V_{cc}$  and  $V_{IN}$  are short-circuited with 0V or GND for some kind of reasons, current charged in the capacitor flows into the output and may destroy the IC. Use a capacitor smaller than 1000  $\mu F$  between output and GND.

### 8. Inspection by set substrate

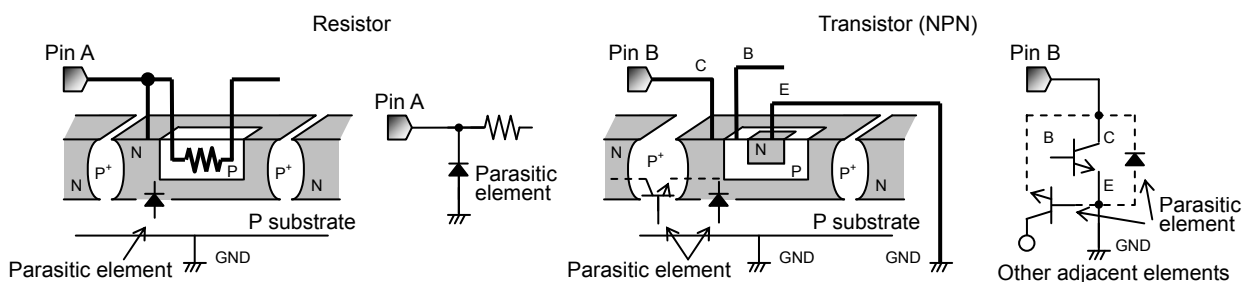
In the event a capacitor is connected to a pin with low impedance at the time of inspection with a set substrate, there is a fear of applying stress to the IC. Therefore, be sure to discharge electricity for every process. As electrostatic measures, provide grounding in the assembly process, and take utmost care in transportation and storage. Furthermore, when the set substrate is connected to a jig in the inspection process, be sure to turn OFF power supply to connect the jig and be sure to turn OFF power supply to remove the jig.

### 9. Inputs to IC terminals

This device is a monolithic IC with  $P^+$  isolation between P-substrate and each element as illustrated below. This P-layer and the N-layer of each element form a PN junction which works as:

- a diode if the electric potentials at the terminals satisfy the following relationship;  $GND > Terminal A > Terminal B$ , or
- a parasitic transistor if the electric potentials at the terminals satisfy the following relationship;  $Terminal B > GND > Terminal A$ .

The structure of the IC inevitably forms parasitic elements, the activation of which may cause interference among circuits, and/or malfunctions contributing to breakdown. It is therefore requested to take care not to use the device in such manner that the voltage lower than GND (at P-substrate) may be applied to the input terminal, which may result in activation of parasitic elements.



10. GND wiring pattern

When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

11. Output capacitor (C3)

Do not fail to connect a output capacitor to VTT output terminal for stabilization of output voltage. The capacitor connected to VTT output terminal works as a loop gain phase compensator. Insufficient capacitance may cause an oscillation. It is recommended to connect a 10 μF ceramic capacitor (X5R or X7R) near to VTT and GND, though it depends on ambient temperature and other conditions. A low ESR ceramic capacitor may reduce a loop gain phase margin and may cause an oscillation, which may be improved by connecting a resistor in series with the OS-capacitor (several-hundred μF). It is therefore requested to carefully check under the actual temperature and load conditions to be applied.

12. Input capacitors (C1 and C2)

These input capacitors are used to reduce the output impedance of power supply to be connected to the input terminals (VCC and VTT\_IN). Increase in the power supply output impedance may result in oscillation or degradation in ripple rejecting characteristics. It is recommended to use a low temperature coefficient 1μF (for VCC) and 10μF (for VTT\_IN) capacitor, but it depends on the characteristics of the power supply input, and the capacitance and impedance of the pc board wiring pattern. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.

13. Input terminals (VCC, VTT\_IN and REF)

VCC, VTT\_IN and REF terminals of this IC are made up independent one another. To VCC terminal, the UVLO function is provided for malfunction protection. REF pin includes the Enable circuit. Irrespective of the input order of the inputs terminals, VTT output is activated to provide the output voltage when UVLO voltages reach the threshold voltage while REF voltage reaches the threshold of EN pin.

14. REF pin (R1 , R2 , C4)

REF pin controls this IC's status ON or OFF. When REF voltage reaches EN-ON voltage, the output voltage operates. Then BD3537F does not include "soft start function" so set the start up time by the value of extra components R1, R2 and C4.

15. Operating range

Within the operating range, the operation and function of the circuits are generally guaranteed at an ambient temperature within the range specified. The values specified for electrical characteristics may not be guaranteed, but drastic change may not occur to such characteristics within the operating range.

16. Allowable loss Pd

For the allowable loss, the thermal derating characteristics are shown in the Exhibit, which should be used as a guide. Any uses that exceed the allowable loss may result in degradation in the functions inherent to IC including a decrease in current capability due to chip temperature increase. Use within the allowable loss.

17. Built-in thermal shutdown protection circuit

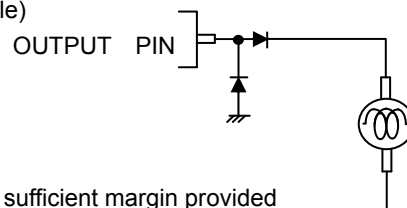
Thermal shutdown protection circuit is built-in to prevent thermal breakdown. Turns VTT output to OFF when the thermal shutdown protection circuit activates. This thermal shutdown protection circuit is originally intended to protect the IC itself. It is therefore requested to conduct a thermal design not to exceed the temperature under which the thermal shutdown protection circuit can work.

18. The use in the strong electromagnetic field may sometimes cause malfunction, to which care must be taken.

In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

19. In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

(Example)

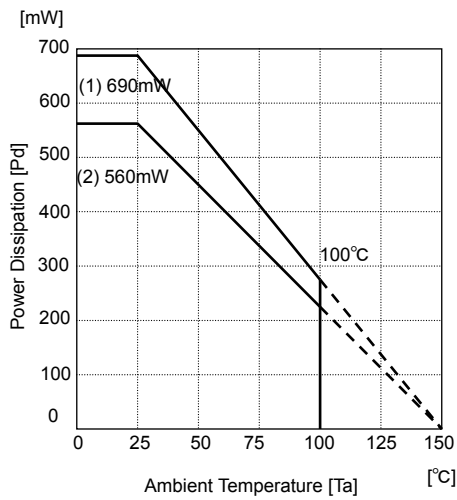


20. We are certain that examples of applied circuit diagrams are recommendable, but you are requested to thoroughly confirm the characteristics before using the IC.

In addition, when the IC is used with the external circuit changed, decide the IC with sufficient margin provided while consideration is being given not only to static characteristics but also variations of external parts and our IC including transient characteristics.

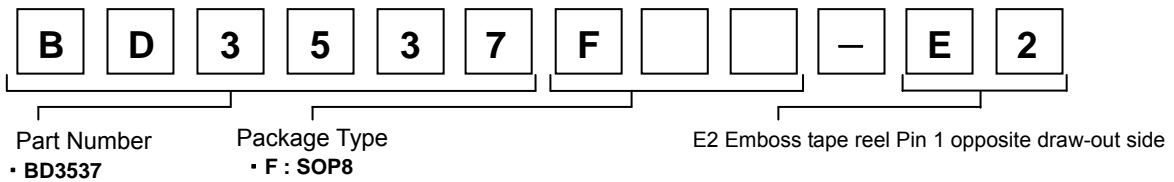


●POWER DISSIPATION  
 ◎SOP8(BD3537F)



(1) 70mm × 70mm × 1.6mm Glass-epoxy PCB  
 $\theta_{j-c}=181^{\circ}\text{C/W}$   
 (2) With no heat sink  
 $\theta_{j-a}=222^{\circ}\text{C/W}$

●Ordering part number



SOP8

<Dimension>		<Tape and Reel information>							
		<table border="1"> <tr> <td>Tape</td> <td>Embossed carrier tape</td> </tr> <tr> <td>Quantity</td> <td>2500pcs</td> </tr> <tr> <td>Direction of feed</td> <td>E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)</td> </tr> </table>		Tape	Embossed carrier tape	Quantity	2500pcs	Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)
Tape	Embossed carrier tape								
Quantity	2500pcs								
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)								
(Unit:mm)		※When you order , please order in times the amount of package quantity.							

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<b>Chicago</b>	TEL: +1-847-368-1006	FAX: +1-847-368-1008	<b>Nanjing</b>	TEL: +86-25-8689-0015	FAX: +86-25-8689-0393
<b>Dallas</b>	TEL: +1-469-287-5366	FAX: +1-469-362-7973	<b>Ningbo</b>	TEL: +86-574-87654201	FAX: +86-574-87654208
<b>Denver</b>	TEL: +1-303-708-0908	FAX: +1-303-708-0858	<b>Qingdao</b>	TEL: +86-532-5779-312	FAX: +86-532-5779-653
<b>Detroit</b>	TEL: +1-248-348-9920	FAX: +1-248-348-9942	<b>Suzhou</b>	TEL: +86-510-82702693	FAX: +86-510-82702992
<b>Nashville</b>	TEL: +1-615-620-6700	FAX: +1-615-620-6702	<b>Wuxi</b>	TEL: +86-510-82702693	FAX: +86-510-82702992
<b>Mexico</b>	TEL: +52-33-3123-2001	FAX: +52-33-3123-2002	<b>Shenzhen</b>	TEL: +86-755-8307-3008	FAX: +86-755-8307-3003
<b>Düsseldorf</b>	TEL: +49-2154-9210	FAX: +49-2154-921400	<b>Dongguan</b>	TEL: +86-769-8393-3320	FAX: +86-769-8398-4140
<b>Munich</b>	TEL: +49-8999-216168	FAX: +49-8999-216176	<b>Fuzhou</b>	TEL: +86-591-8801-8698	FAX: +86-591-8801-8690
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<b>France</b>	TEL: +33-1-5697-3060	FAX: +33-1-5697-3080	<b>Huizhou</b>	TEL: +86-752-205-1054	FAX: +86-752-205-1059
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