Tel: 886-2-66296288
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DESCRIPTION

PT6332 is a VFD driver IC driven on 1/2 to 1/3 duty factor. It can drive up to 168 segments. 56 segment output lines, 3 grid output lines, 4 general purpose output lines, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro controller. Pin configuration and application circuit are optimized for easy PCB layout and cost saving advantages.

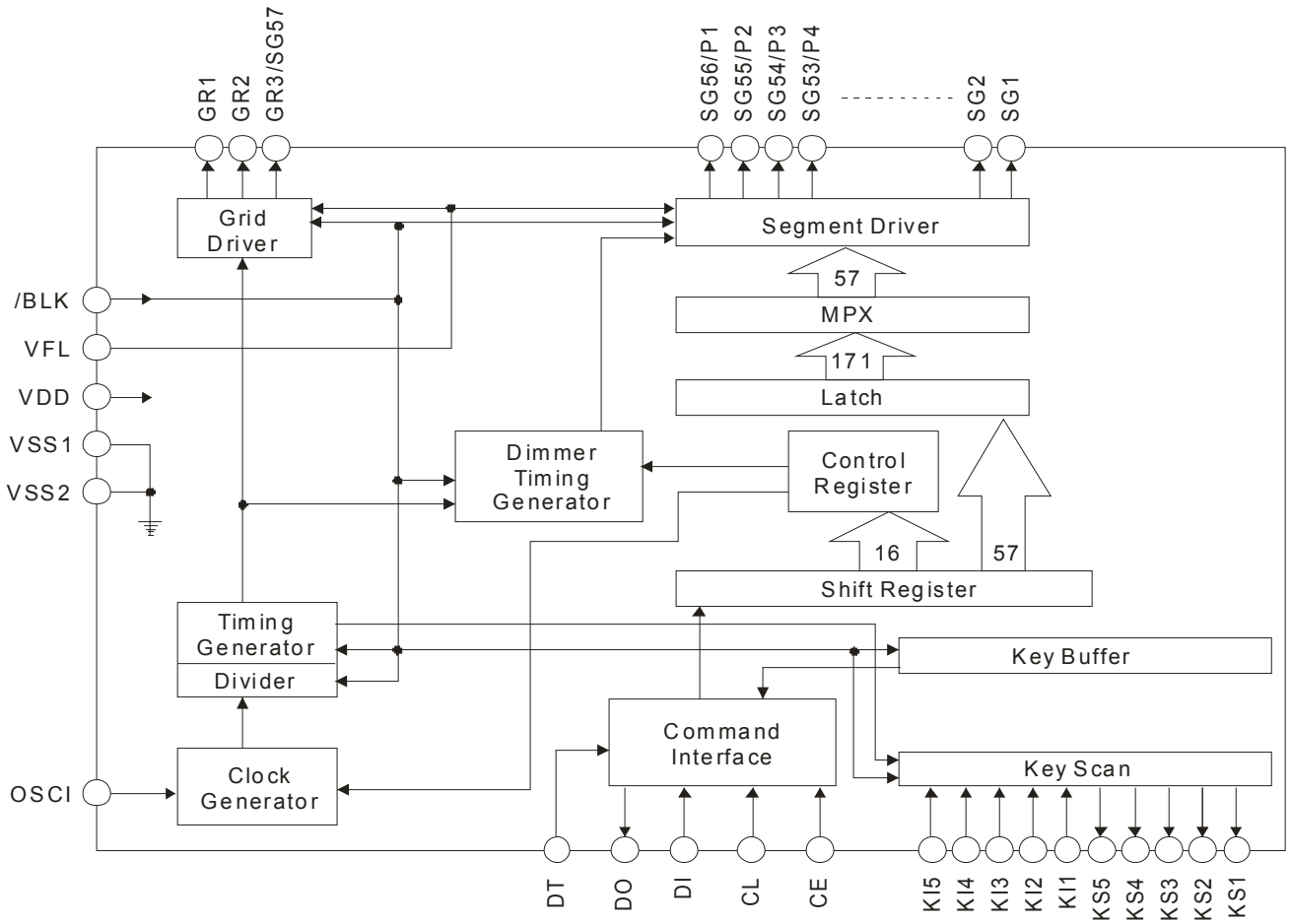
FEATURES

- CMOS technology
- Up to 168 segment outputs (3 Grid & 56 Segment drivers) or
  Up to 114 segment outputs (2 Grid & 57 Segment drivers)
- Up to 25 key inputs
- Up to 4 general purpose outputs
- Sleep and dimmer mode
- One-Pin oscillation circuit
- Hard ware duty cycle selection 1/2 or 1/3
- Available in 80 pins, LQFP

APPLICATION

- Electronic equipment with VFD display

BLOCK DIAGRAM



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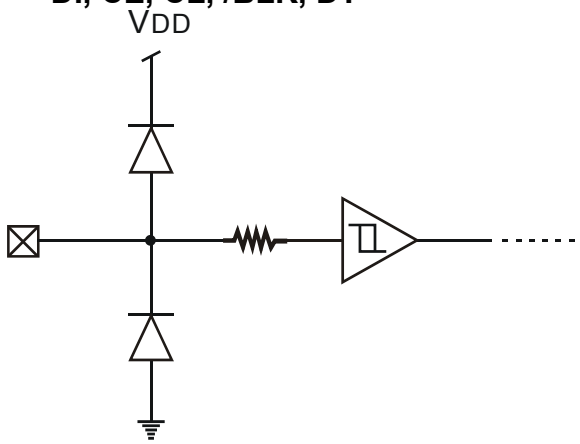
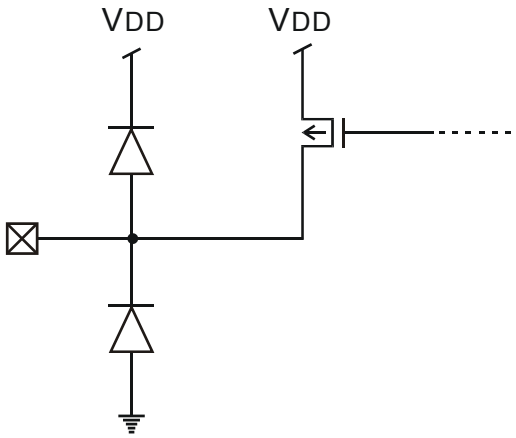
INPUT/OUTPUT PINS EQUIVALENT CIRCUIT

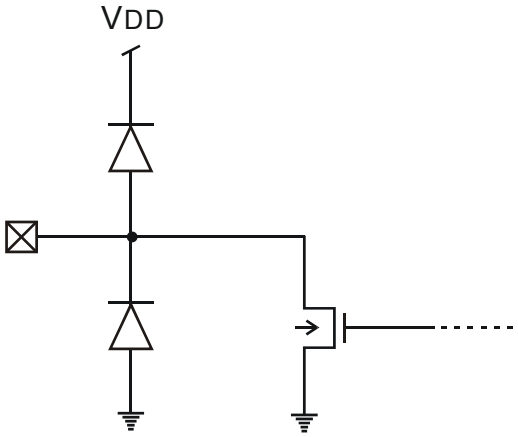
- **DI, CE, CL, /BLK, DT**



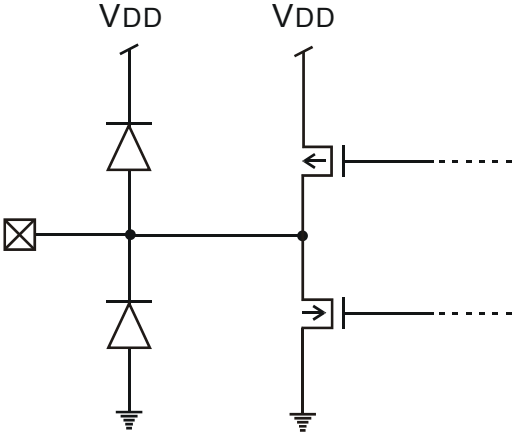
- **OSCI**



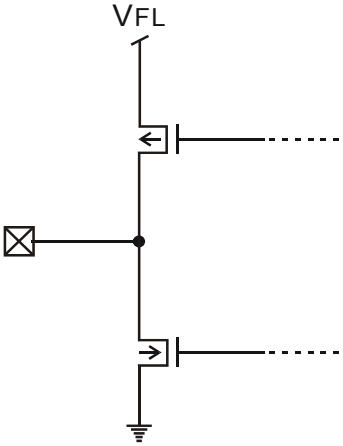
- **DO**



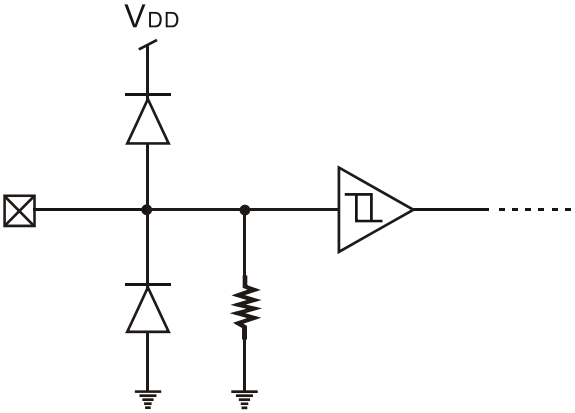
- **KSn**



- **GRn, SGn**



- **KIn**



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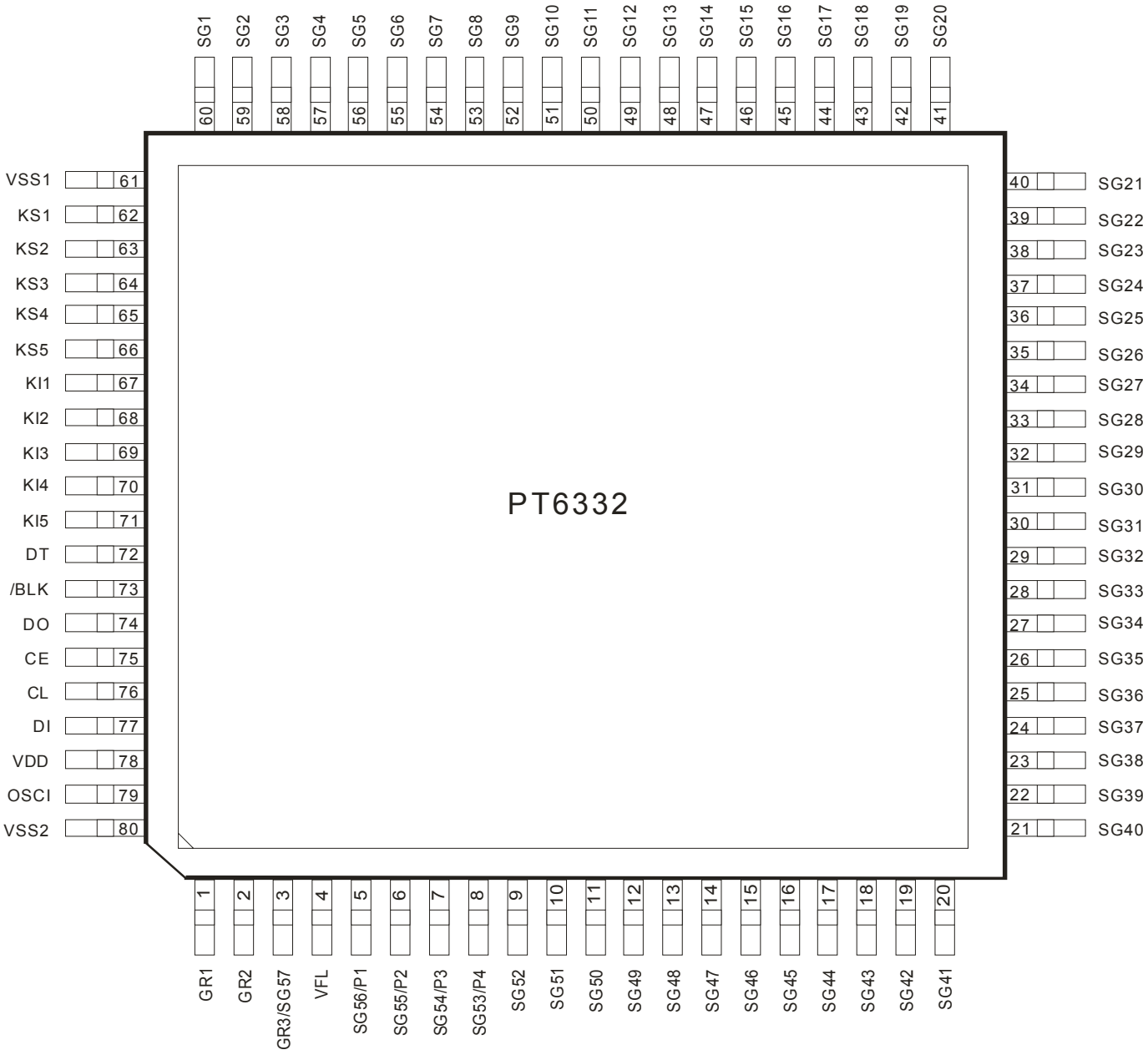
PIN CONFIGURATION



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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
GR1 ~ GR2	O	Grid driver output pin	1 ~ 2
GR3/SG57	O	Grid/Segment driver output pin	3
VFL	-	Driver power supply	4
SG56/P1 ~ SG53/P4	O	Segment driver/General purpose output pin	5 ~ 8
SG52 ~ SG1	O	Segment output pin	9~ 60
VSS1	-	Ground pin	61
KS1 ~ KS5	O	Key scan output pin	62 ~ 66
KI1 ~ KI5	I	Key scan input pin	67 ~ 71
DT	I	Duty cycle selection pin (DT=0, 1/3 duty) (DT=1, 1/2 duty)	72
/BLK	I	Blank input pin (Reset pin) When this pin is set to “Low” level, the display is turned off and key scan is disabled. All key data are reset to low. When this pin is set to “High”, the display is turned on and the key scan is enabled. (see note)	73
DO	O	Data output pin (open ~ drain)	74
CE	I	Chip enable input pin	75
CL	I	Clock input pin	76
DI	I	Data input pin	77
VDD	-	Power supply	78
OSCI	I	Oscillation input pin	79
VSS2	-	Ground pin	80

FUNCTION DESCRIPTION

SERIAL DATA INPUT

1/3 DUTY

When stopped with CL at the low level.

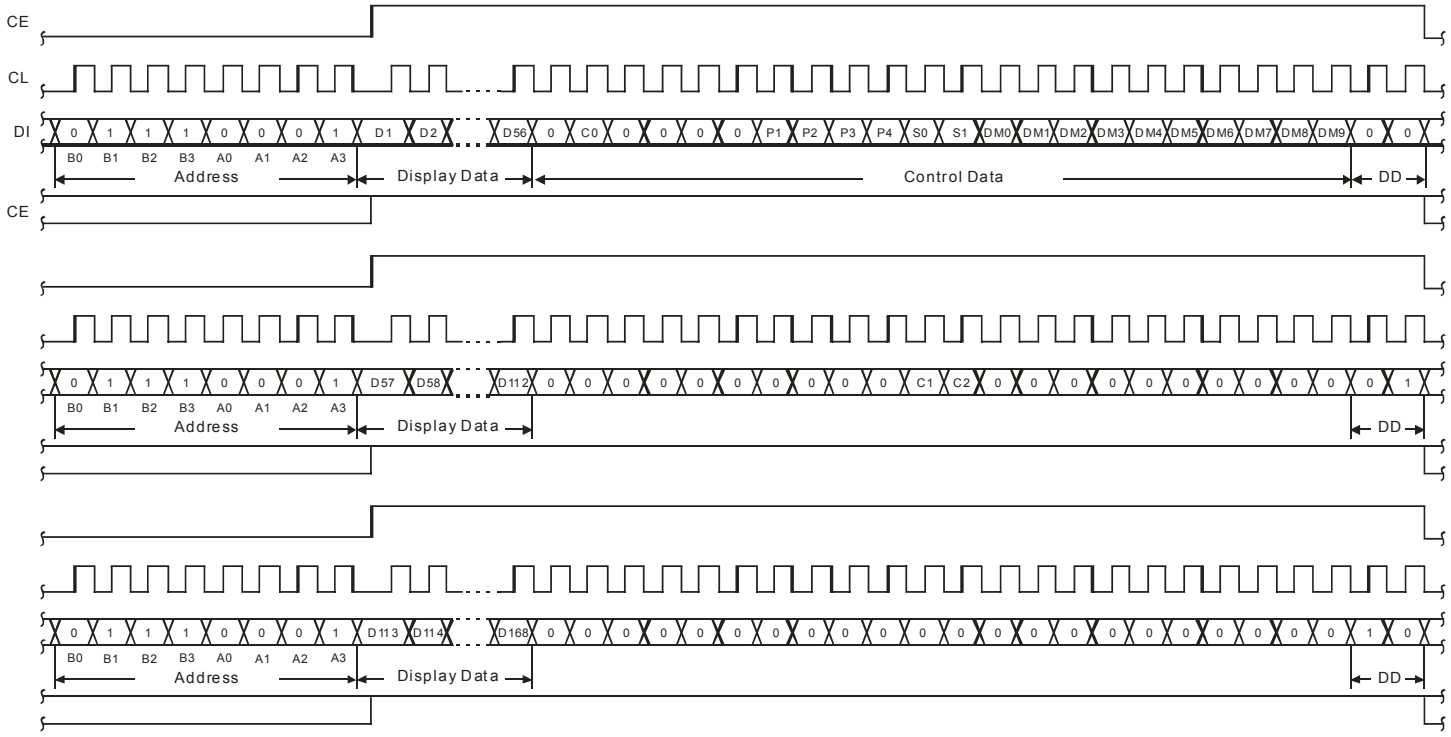


Figure 1

Note: DD=Direction Data

When stopped with CL at the high level.

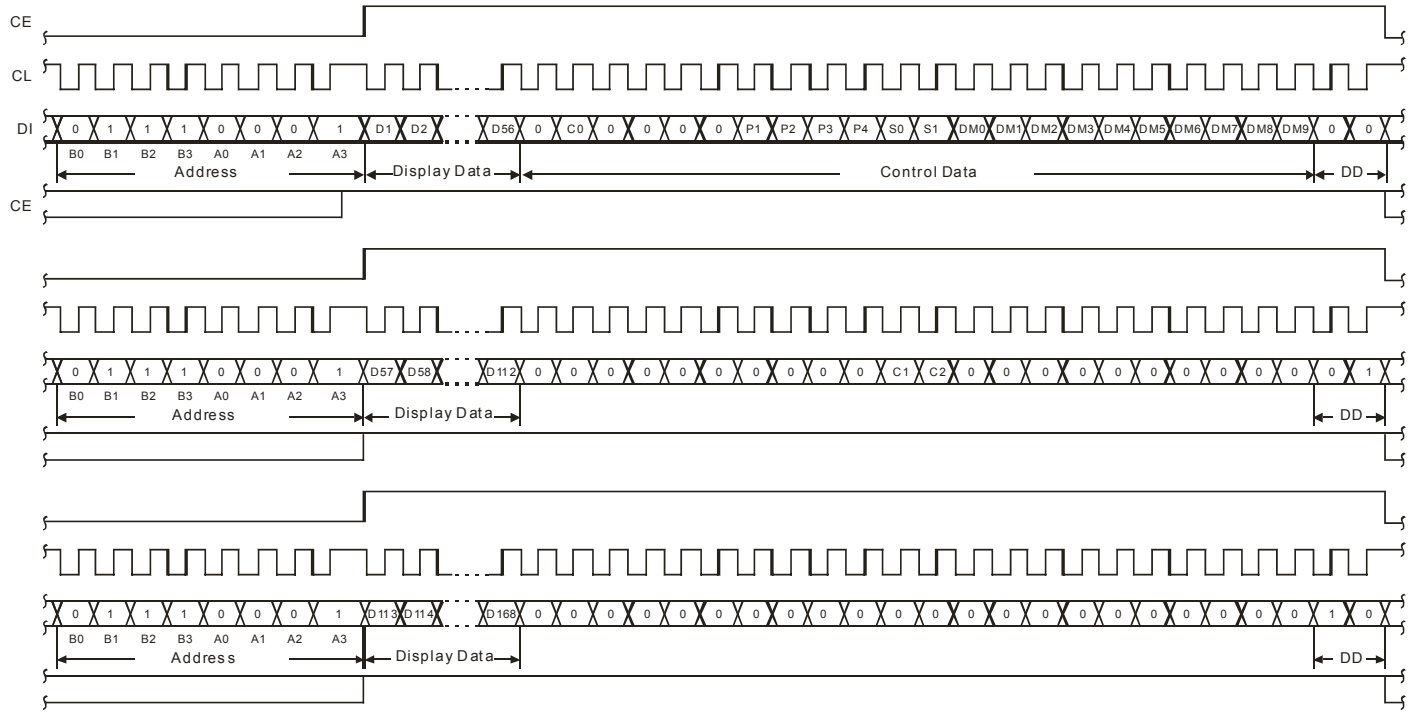


Figure 2

Notes:

1. DD : Direction Data
2. Address : Applications must send the value ($8E_H$) as shown in figure 1 & 2
3. D1 to D56 : Segment display data for the GR1 digit output pin (when P1 ~ P4=0)
   Dn (n=1 to 56)=1: Segment on
   Dn (n=1 to 56)=0: Segment off
4. D57 to D112 : Segment display data for the GR2 digit output pin
   Dn (n=57 to 112)=1: Segment on
   Dn (n=57 to 112)=0: Segment off
5. D113 to D168 : Segment display data for the GR3 digit output pin
   Dn (n=113 to 168)=1: Segment on
   Dn (n=113 to 168)=0: Segment off
6. D53 to D56 : General purpose output pin (when P1~P4=1)
   Dn (n=53 to 56)=1: General purpose on (High level)
   Dn (n=53 to 56)=0: General purpose off (Low level)
7. C0 to C2 : Sleep Mode Current Setup
   Cn (n=0 to 2)=0: $I_{DD1} \leq 100\mu A$ (Normal mode)
   Cn (n=0 to 2)=1: $I_{DD1} \leq 5\mu A$ (Test mode)

1/2 DUTY

When stopped with CL at the low level.

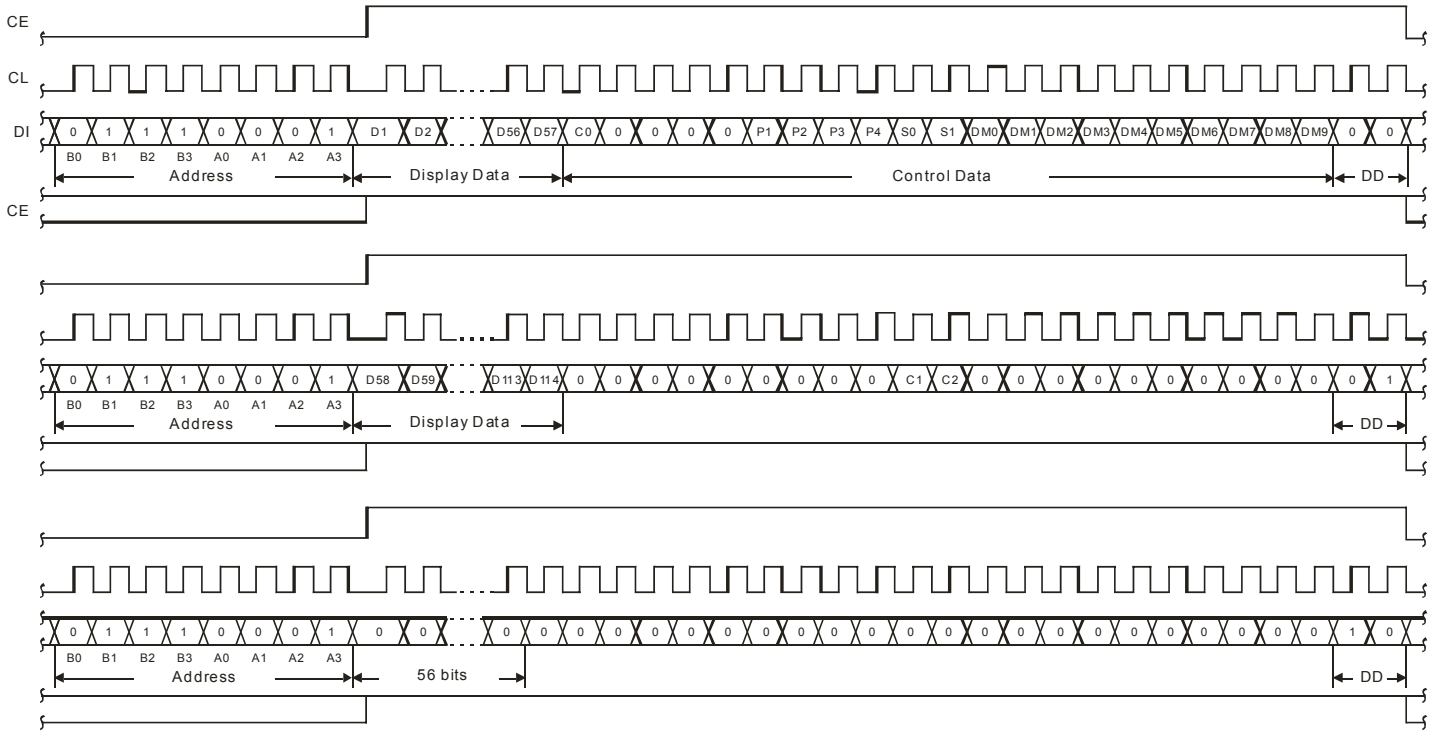


Figure 3

Note: DD=Direction Data

When stopped with CL at the high level.

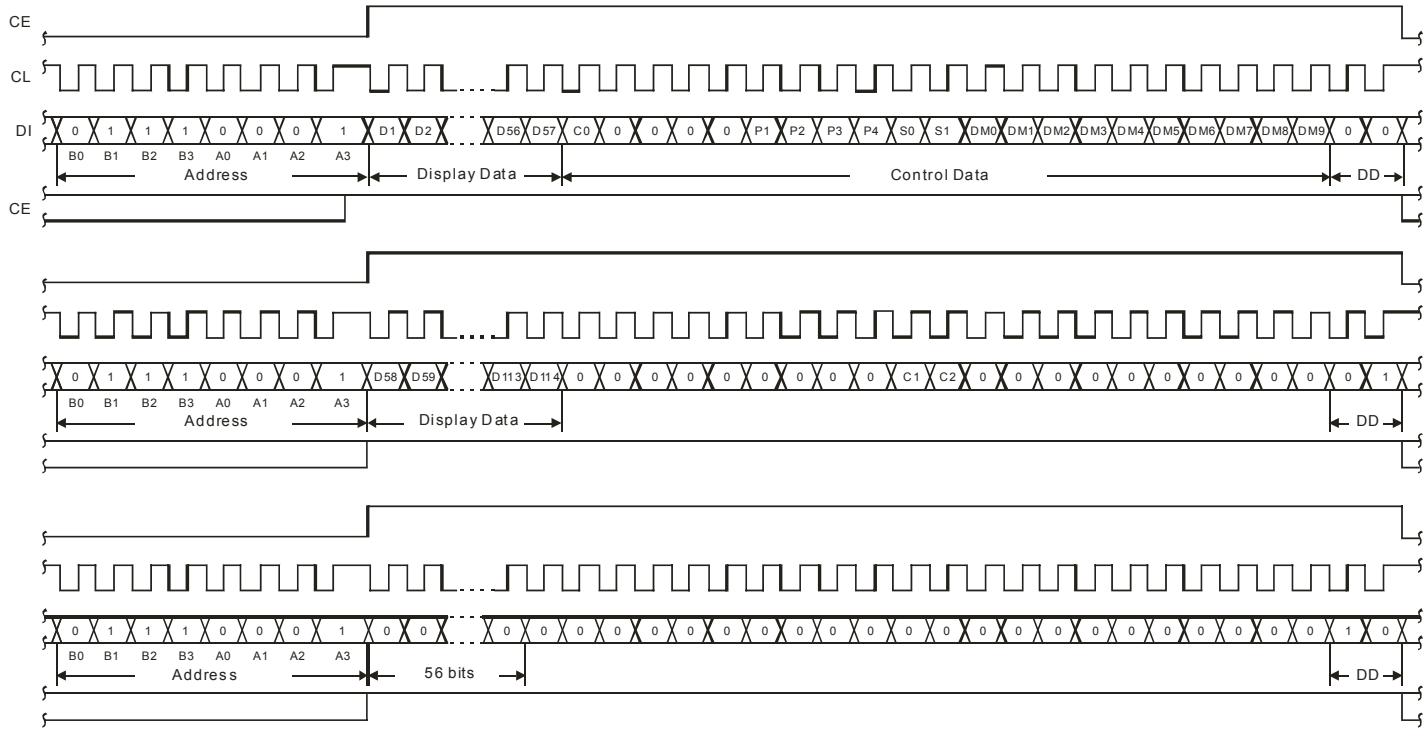


Figure 4

Notes:

1. DD : Direction Data
2. Address : Applications must send the value ($8E_H$) as shown in figure 3 & 4
3. D1 to D57 : Segment display data for the GR1 digit output pin (when P1 ~ P4 = 0)
   Dn (n=1 to 57) = 1: Segment on
   Dn (n=1 to 57) = 0: Segment off
4. D58 to D114 : Segment display data for the GR2 digit output pin
   Dn (n=58 to 114) = 1: Segment on
   Dn (n=58 to 114) = 0: Segment off
5. D53 to D56 : General purpose output pin (when P1 ~ P4=1)
   Dn (n=53 to 56) = 1: General purpose on (High level)
   Dn (n=53 to 56) = 0: General purpose off (Low level)
6. C0 to C2 : Sleep Mode Current Setup
   Cn (n=0 to 2)=0: $I_{DD1} \leq 100\mu A$ (Normal mode)
   Cn (n=0 to 2)=1: $I_{DD1} \leq 5\mu A$ (Test mode)

CONTROL DATA

P1 TO P4: SEGMENT DRIVER/GENERAL PURPOSE OUTPUT CONTROL DATA

This control data controls switching SG56/P1~SG53/P4 between segment driver and general purpose output. When SG56/P1~SG53/P4 is used as general purpose output which will be not affected by dimming and segment control.

Control Bit	Data	Output Pin Mode
P1	H/L	P1/SG56
P2	H/L	P2/SG55
P3	H/L	P3/SG54
P4	H/L	P4/SG53

When SG56/P1~SG53/P4 is used as general purpose output. The table lists the relationship between the output pin and control bit as below.

Output Pin Mode	Control Bit
SG56/P1	D56
SG55/P2	D55
SG54/P3	D54
SG53/P4	D53

S0, S1: SLEEP CONTROL DATA

This control data controls switching between sleep mode and normal mode, and also sets the states of the KS1 to KS5 key scan output pins in key scan standby mode.

Control Data		Mode	Clock Generator (oscillator circuit)	Segment Outputs Digit Output	Output Pin states during key scan standby				
S0	S1				KS1	KS2	KS3	KS4	KS5
0	0	Normal	Oscillator operating	Operating	H	H	H	H	H
0	1	Sleep	Stopped	L	L	L	L	L	H
1	0	Sleep	Stopped	L	L	L	L	H	H
1	1	Sleep	Stopped	L	H	H	H	H	H

CT0 TO CT3: SLEEP CURRENT CONTROL DATA

Control Bit			Current	Mode
CT0	CT1	CT2		
0	0	0	$I_{DD1} \leq 100\mu A$	Normal mode
1	1	1	$I_{DD1} \leq 5\mu A$	Test mode

DM0 TO DM9: DIMMER DATA

This data controls the duty of the SG1 to SG56 segment output pins. This data forms a 10-bit binary value in which D0 is the LSB. The brightness of the display can be controlled by adjusting the duty of the SG1 to SG56 segment output pins. The table lists the relationship between the dimmer data and the dimmer value.

DM9	DM8	DM7	DM6	DM5	DM4	DM3	DM2	DM1	DM0	Dimmer Value (t4/t3)
0	0	0	0	0	0	0	0	0	0	0/1024
0	0	0	0	0	0	0	0	0	1	1/1024
0	0	0	0	0	0	0	0	1	0	2/1024
to										to
1	1	1	1	1	1	1	1	0	0	1020/1024
1	1	1	1	1	1	1	1	0	1	1021/1024
1	1	1	1	1	1	1	1	1	0	1022/1024
1	1	1	1	1	1	1	1	1	1	1022/1024

t3 and t4: see figure 7

RELATIONSHIP BETWEEN THE DISPLAY DAT (D1 TO D168 AND THE SEGMENT OUTPUT PINS)

1/3 DUTY

Segment Output Pin	GR1	GR2	GR3
SG1	D1	D57	D113
SG2	D2	D58	D114
SG3	D3	D59	D115
SG4	D4	D60	D116
SG5	D5	D61	D117
SG6	D6	D62	D118
SG7	D7	D63	D119
SG8	D8	D64	D120
SG9	D9	D65	D121
SG10	D10	D66	D122
SG11	D11	D67	D123
SG12	D12	D68	D124
SG13	D13	D69	D125
SG14	D14	D70	D126
SG15	D15	D71	D127
SG16	D16	D72	D128
SG17	D17	D73	D129
SG18	D18	D74	D130
SG19	D19	D75	D131

Segment Output Pin	GR1	GR2	GR3
SG20	D20	D76	D132
SG21	D21	D77	D133
SG22	D22	D78	D134
SG23	D23	D79	D135
SG24	D24	D80	D136
SG25	D25	D81	D137
SG26	D26	D82	D138
SG27	D27	D83	D139
SG28	D28	D84	D140
SG29	D29	D85	D141
SG30	D30	D86	D142
SG31	D31	D87	D143
SG32	D32	D88	D144
SG33	D33	D89	D145
SG34	D34	D90	D146
SG35	D35	D91	D147
SG36	D36	D92	D148
SG37	D37	D93	D149
SG38	D38	D94	D150

Segment Output Pin	GR1	GR2	GR3
SG39	D39	D95	D151
SG40	D40	D96	D152
SG41	D41	D97	D153
SG42	D42	D98	D154
SG43	D43	D99	D155
SG44	D44	D100	D156
SG45	D45	D101	D157
SG46	D46	D102	D158
SG47	D47	D103	D159
SG48	D48	D104	D160
SG49	D49	D105	D161
SG50	D50	D106	D162
SG51	D51	D107	D163
SG52	D52	D108	D164
SG53	D53	D109	D165
SG54	D54	D110	D166
SG55	D55	D111	D167
SG56	D56	D112	D168

As an example, the table below lists the operation of the SG11 segment output pin.

Display Data			Segment Output Pin (SG11) State
D11	D67	D123	
0	0	0	The segments corresponding to the GR1 to GR3 digit output pins are off
0	0	1	The segment corresponding to the GR3 digit output pin is on
0	1	0	The segment corresponding to the GR2 digit output pin is on
0	1	1	The segments corresponding to the GR2 to GR3 digit output pins are on
1	0	0	The segment corresponding to the GR1 digit output pin is on
1	0	1	The segments corresponding to the GR1 and GR3 digit output pins are on
1	1	0	The segments corresponding to the GR1 and GR2 digit output pins are on
1	1	1	The segments corresponding to the GR1 to GR3 digit output pins are on

RELATIONSHIP BETWEEN THE DISPLAY DAT (D1 TO D114 AND THE SEGMENT OUTPUT PINS)

1/2 DUTY

Segment Output Pin	GR1	GR2
SG1	D1	D58
SG2	D2	D59
SG3	D3	D60
SG4	D4	D61
SG5	D5	D62
SG6	D6	D63
SG7	D7	D64
SG8	D8	D65
SG9	D9	D66
SG10	D10	D67
SG11	D11	D68
SG12	D12	D69
SG13	D13	D70
SG14	D14	D71
SG15	D15	D72
SG16	D16	D73
SG17	D17	D74
SG18	D18	D75
SG19	D19	D76

Segment Output Pin	GR1	GR2
SG20	D20	D77
SG21	D21	D78
SG22	D22	D79
SG23	D23	D80
SG24	D24	D81
SG25	D25	D82
SG26	D26	D83
SG27	D27	D84
SG28	D28	D85
SG29	D29	D86
SG30	D30	D87
SG31	D31	D88
SG32	D32	D89
SG33	D33	D90
SG34	D34	D91
SG35	D35	D92
SG36	D36	D93
SG37	D37	D94
SG38	D38	D95

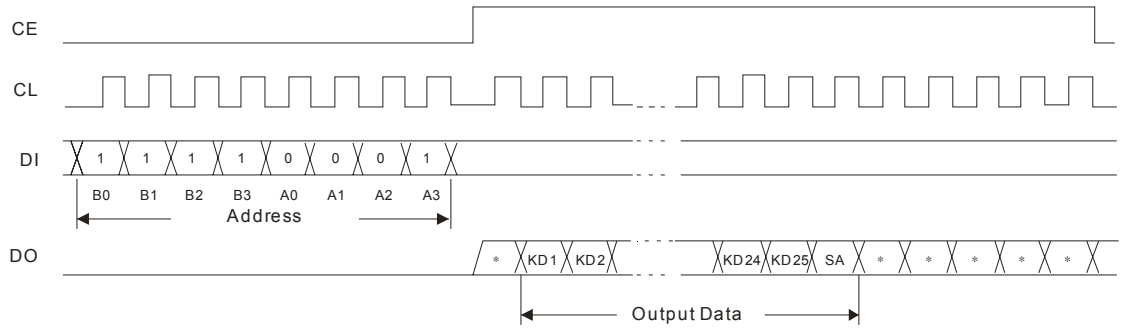
Segment Output Pin	GR1	GR2
SG39	D39	D96
SG40	D40	D97
SG41	D41	D98
SG42	D42	D99
SG43	D43	D100
SG44	D44	D101
SG45	D45	D102
SG46	D46	D103
SG47	D47	D104
SG48	D48	D105
SG49	D49	D106
SG50	D50	D107
SG51	D51	D108
SG52	D52	D109
SG53	D53	D110
SG54	D54	D111
SG55	D55	D112
SG56	D56	D113
SG57	D57	D114

As an example, the table below lists the operation of the SG11 segment output pin.

Display Data		Segment Output Pin (SG11) State
D11	D68	
0	0	The segments corresponding to the GR1 to GR2 digit output pins are off
0	1	The segment corresponding to the GR2 digit output pin is on
1	0	The segment corresponding to the GR1 digit output pin is on
1	1	The segments corresponding to the GR1 to GR2 digit output pins are on

SERIAL DATA OUTPUT

When stopped with CL at the low level



When stopped with CL at the high level

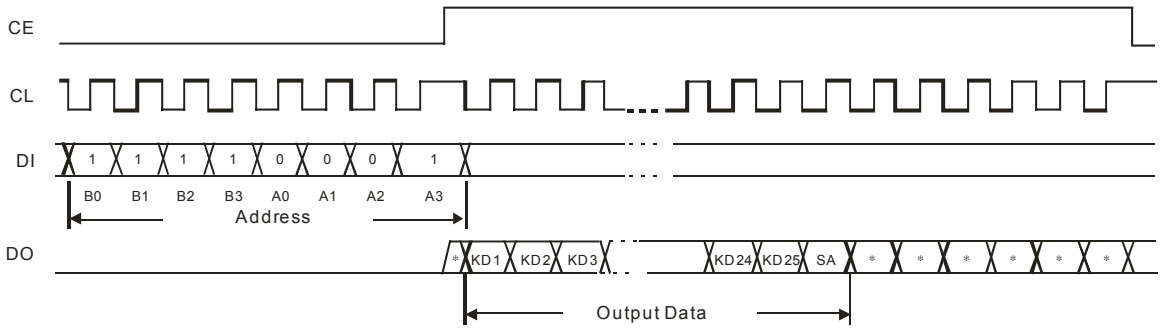


Figure 5

Note:

*	: Don't Care
Address	: Applications must send the value ($8F_H$) as shown in figure 5
KD1 to KD25	: Key Data
SA	: Sleep Acknowledge Data

The key data (KD1 to KD25) and the sleep acknowledge data (SA) will be invalid if the key data is read when DO is high.

OUTPUT DATA

KD1 TO KD25: KEY DATA

These bits represent the key output states when a key matrix with up to 25 keys is formed using the KS1 to KS5 key scan output pins and the KI1 to KI5 key scan input pins. When a key is pressed, the bit corresponding to that key will be set to 1. The correspondence is listed in the following table.

Item	KI1	KI2	KI3	KI4	KI5
KS1	KD1	KD2	KD3	KD4	KD5
KS2	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25

SA: SLEEP ACKNOWLEDGE DATA

This output data is set to the state when the key was pressed. In that case DO will go to the low level. If serial data is input during this period and the mode is set (normal mode or sleep mode), the IC will be set to that mode. SA is set to 1 in the sleep mode and to 0 in the normal mode.

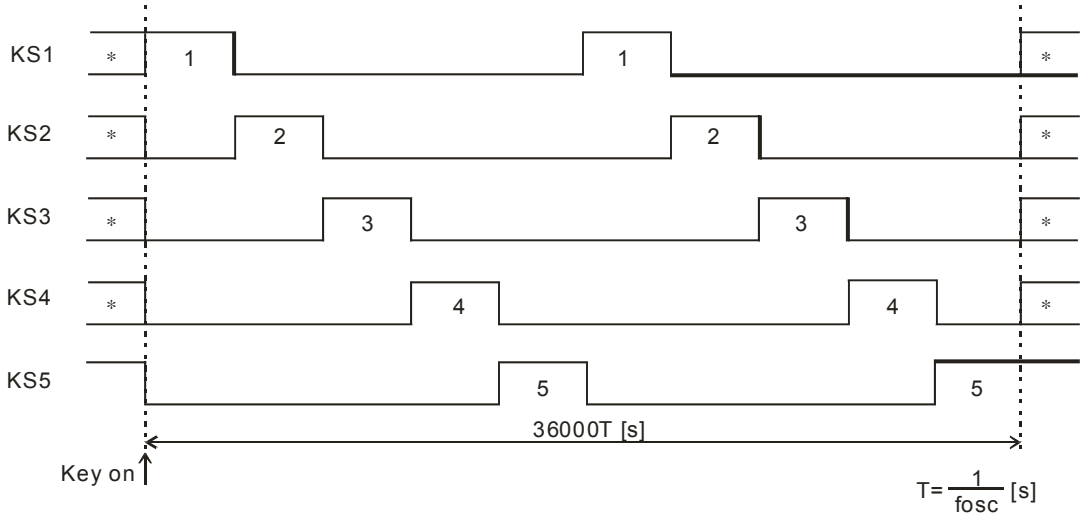
SLEEP MODE

The IC is set to sleep mode by setting either S0 or S1 in the control data to 1. The segment outputs and the digit outputs are all set low, and the clock generator (oscillator circuit) is stopped (although it is restarted when a key is pressed), and thus power dissipation is reduced. This mode is cleared by setting S0 and S1 in the control data to 0.
In sleep mode, the status of segment/general purpose output port will not be changed.

KEY SCAN OPERATION

KEY SCAN TIMING

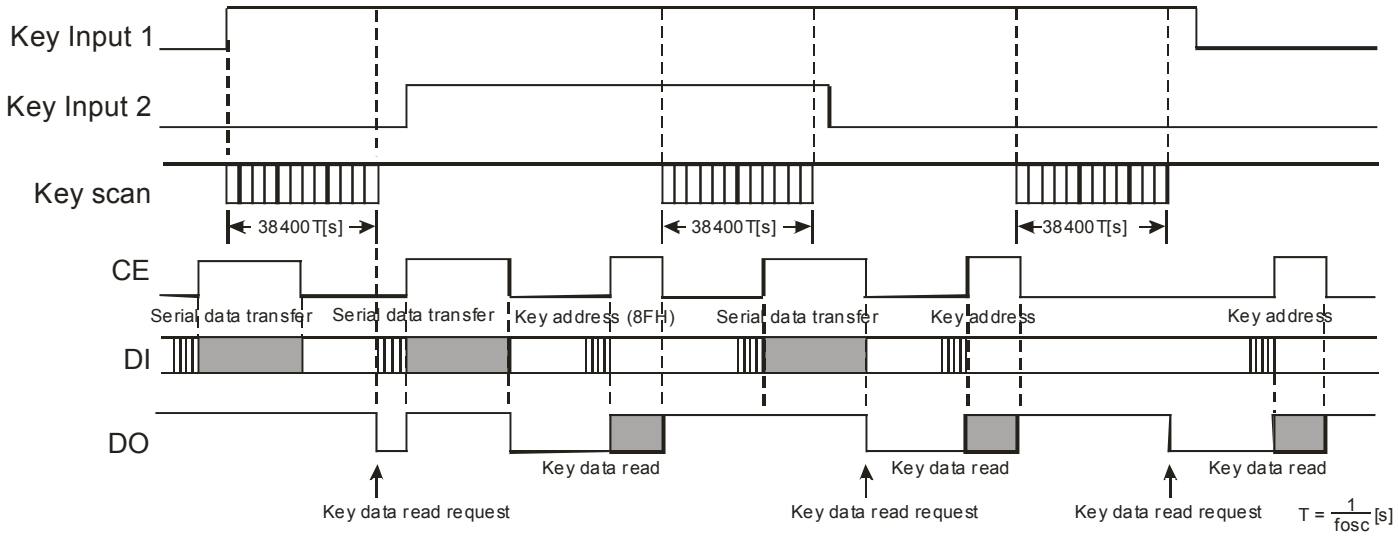
The scan period is 18000T [s]. A key scan is performed twice to reliably recognize the key on/off state by verifying that the key data for the two scans agrees. If the data agrees, the IC recognizes a key press and 38400T [s] after the start of key scan execution issues a key scan data read request by outputting a low level from DO. If the key data does not agree and a key was pressed at the later scan, the IC executes another key scan operation. Note that this means that this IC cannot recognize a key press shorter than 38400T [s].



Note:
*: The high-level and low-level state in sleep mode are set according to the control data S0 and S1. Key scan output signals are not output from pins set to the “L” state.

IN NORMAL MODE

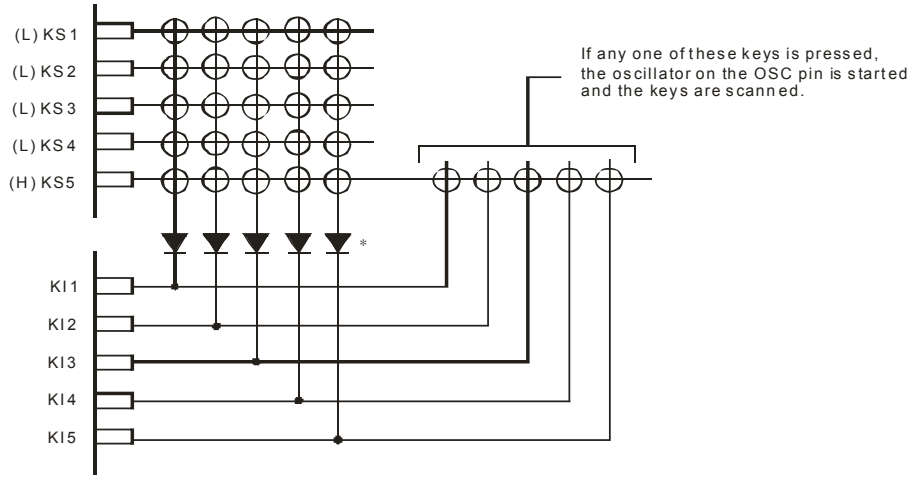
- The pins KS1 to KS5 are set high.
- A key scan is started when any of the keys is pressed, and the keys are kept scanning until all keys are released. The controller can recognize simultaneous multiple key presses by checking the key data for multiple bits being set.
- If a key is pressed for over 38400T [s] (where T=1/fosc), the IC outputs a key data read request to the controller by setting DO low. The controller acknowledges this state and reads the key data. However, note that DO will go high when CE is set high during the serial data transfer.
- After the controller key data readout completes, the key data read request will be cleared (DO will be set high), and the IC performs another key scan. Note that since DO is an open-drain output, a pull-up resistor (between 1 and 10KΩ) is required.



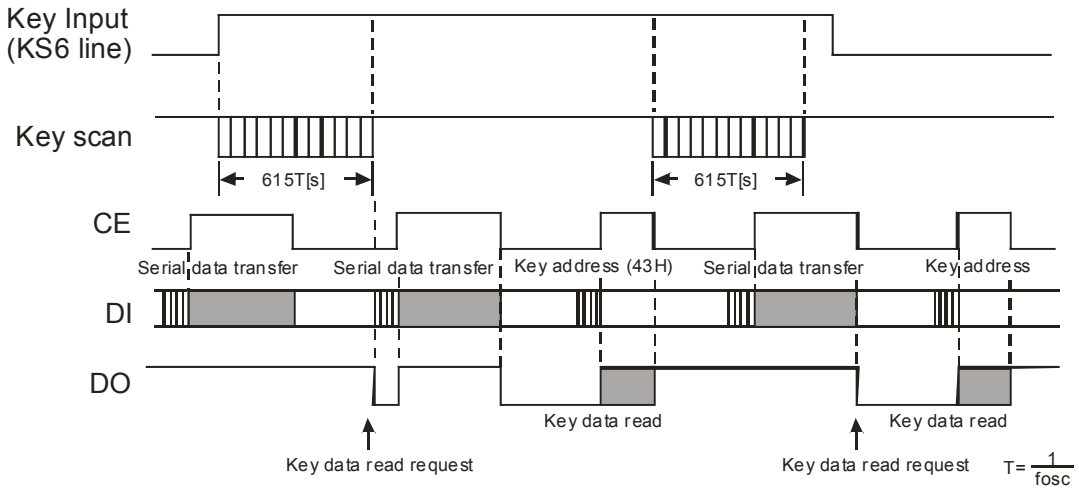
IN SLEEP MODE

- The pins KS1 to KS5 are set to high or low according to the values of S0 and S1 in the control data. (see the description of the control data elsewhere in this document)
- If a key connected to one of the KS1 to KS5 lines that was set high is pressed, the clock generator (oscillator circuit) is started and a key scan is performed, and the keys are kept scanning until all keys are released. The controller can recognize simultaneous multiple key presses by checking the key data for multiple bits being set.
- If a key is pressed for over 38400T [s] (where T=1/fosc), the IC outputs a key data read request to the controller by setting DO low. The controller acknowledges this state and reads the key data. However, note that DO will go high when CE is set high during the serial data transfer.
- After the controller key data readout completes, the key data read request will be cleared (DO will be set high), and the IC performs another key scan. However, sleep mode will not be cleared. Note that since DO is an open-drain output, a pull-up resistor (between 1 and 10KΩ) is required.
- Example of a key scan operation in sleep mode.

Example: Sleep mode with S1=0, S1=1 (only KS5 is set high)



Note:
*: These diodes are required to reliably recognize multiple key presses on the KS5 line when the IC is set to sleep mode with only KS5 set to high as in the example above. That is, they prevent incorrect recognition of key pressed due to sneak currents arising from simultaneous presses of keys on the KS1 through KS4 lines.



MULTIPLE KEY PRESSES

The PT6332, even without diodes in the key scan lines, can scan for any combination of dual key presses, any combination of triple key presses on any of the KI1 to KI5 key scan input pin lines, or any combination of multiple key presses on any of the KS1 to KS5 key scan output lines. However, keys that are not pressed may be seen as having been pressed for any other multiple key press combination. Accordingly, applications must insert diodes at each key. Also, to reject any triple and higher multiple key presses, if three or more data readout are 1 ignore the data by the software or in other ways.

NOTES ON THE /BLK PIN AND DISPLAY CONTROL

Since the states of the IC internal data (D1 to D168, and the control data) are undefined when power is first applied, applications should turn off the display (i.e. set SG1 to SG56 and GR1 to GR3 low) by setting the /BLK pin low at the same time as power is applied. Applications should transfer all 264 bits of the serial data while /BLK is held low, and only then set /BLK high. This will prevent random meaningless display at power on. (see figure 6)

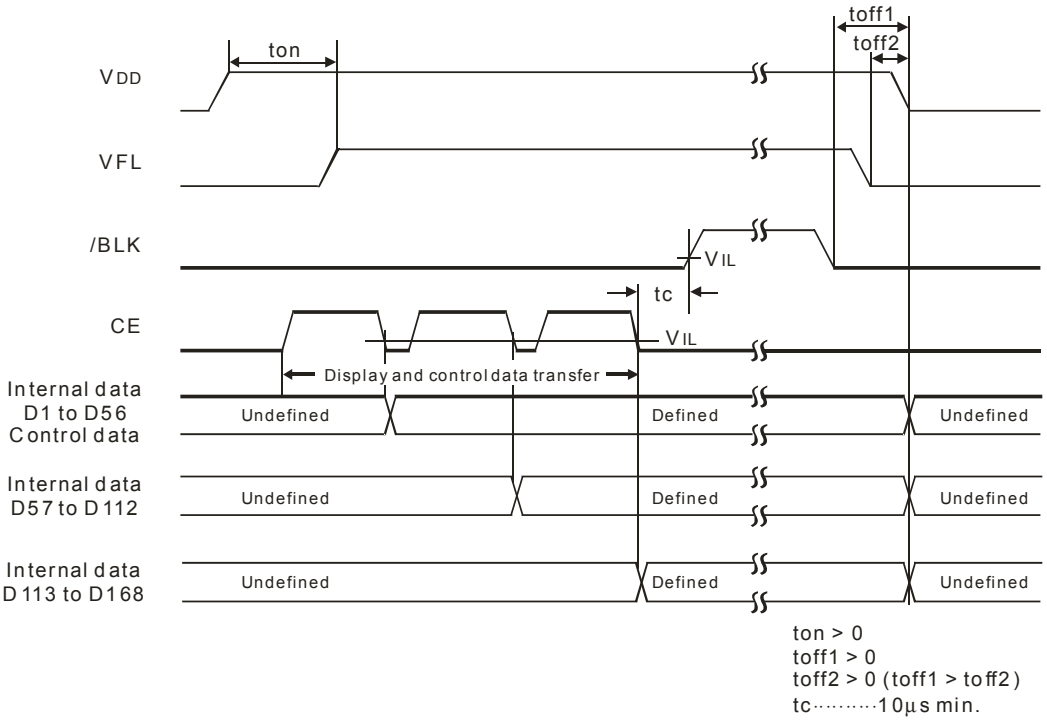
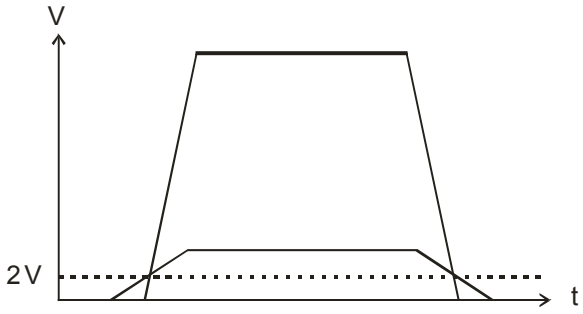


Figure 6

NOTE ON THE POWER ON SEQUENCE

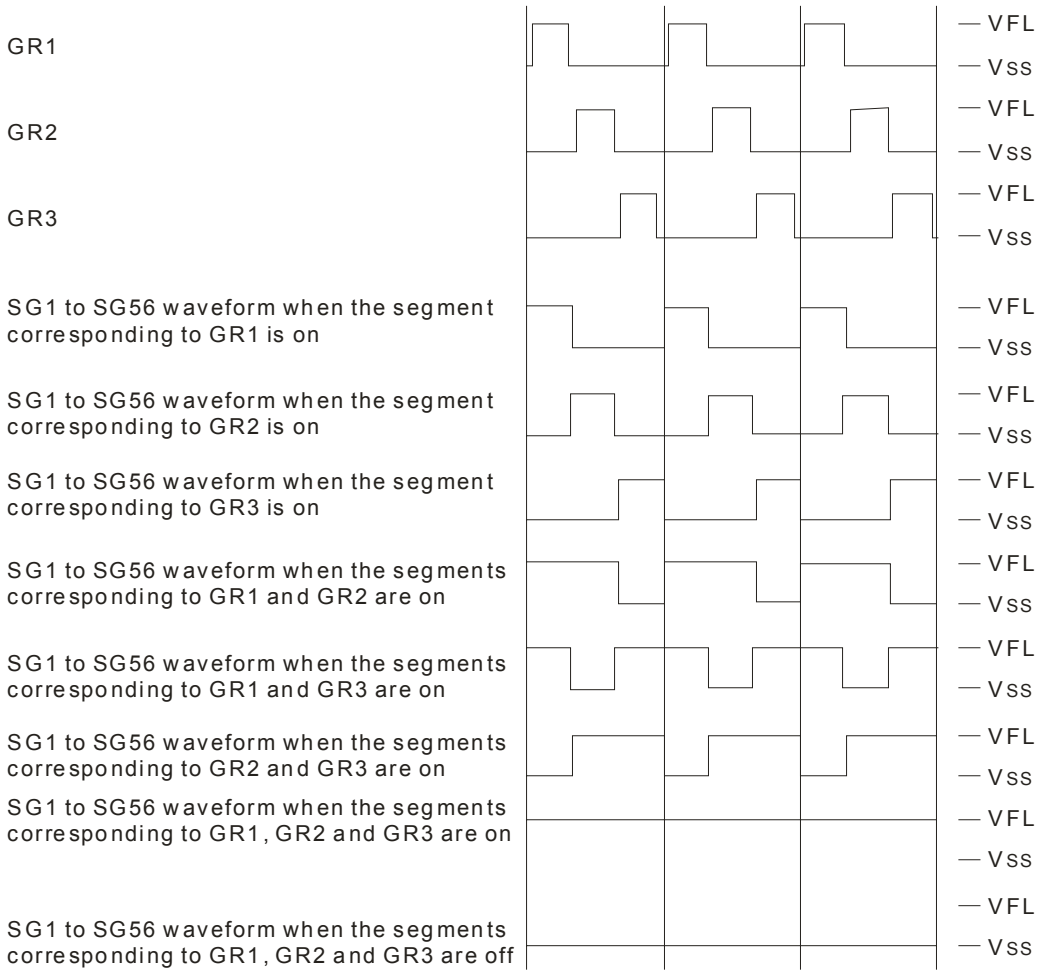
Applications must observe the following sequence when turning the power on or off.

- At power on: First turn on the logic system power (V_{DD}), and then turn on the driver power (V_{FL}).
- At power off: First turn off the driver power (V_{FL}), and then turn off the logic system power (V_{DD}).



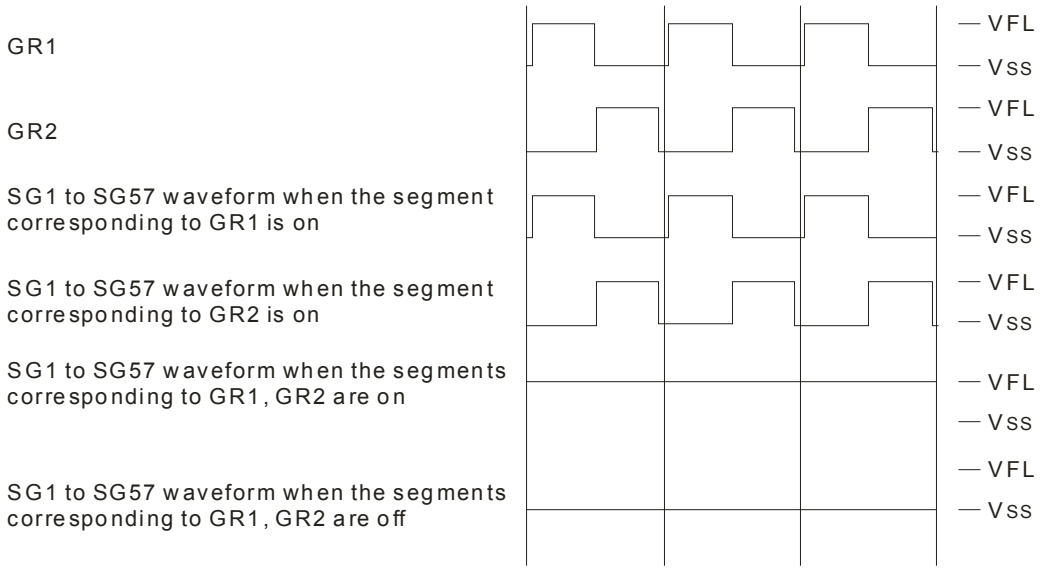
OUTPUT WAVEFOORMS (SG1 TO SG56)

1/3 DUTY



OUTPUT WAVEFOORMS (SG1 TO SG57)

1/2 DUTY



RELATIONSHIP BETWEEN THE SEGMENT AND DIGIT OUTPUTS

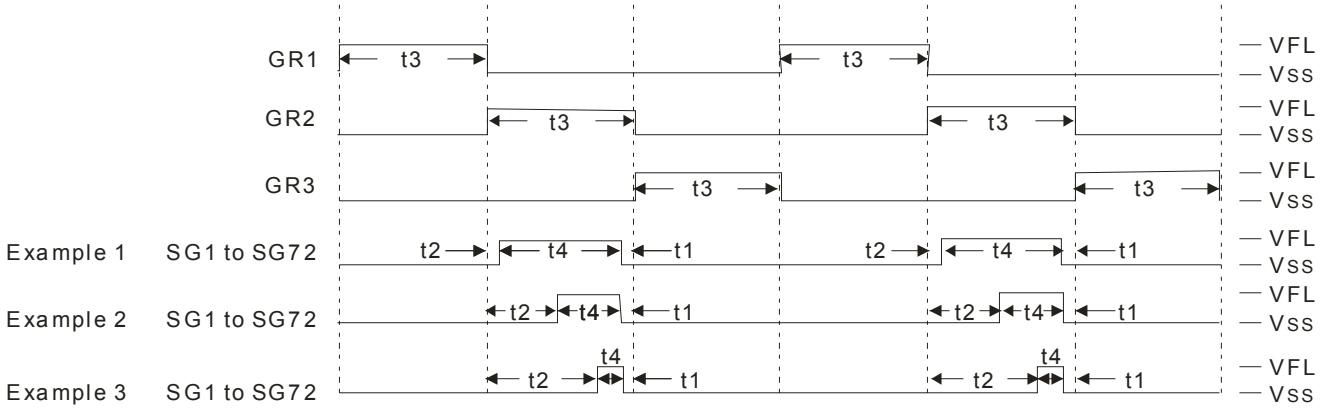


Figure 7

- Figure 7 shows the case where the display data is set up so that the segment outputs SG1 to SG56 output the VSS level with the same timing as the GR1 and GR3 digit outputs, and output the VFL level with the same timing as the GR2 digit output. Here, the segments corresponding to GR2 will be turned on. The relationship between t3 and the oscillator frequency fosc in this case is t3=2048/fosc.
- The SG1 to SG56 segment output waveforms in example 1 correspond to a dimmer data (DM0 to DM9) set to $3FE_H$. The relationship between t1 and the oscillator frequency fosc is t1=2/fosc. Note that t1 and t2 in example 1 are identical times.
- The SG1 to SG56 segment output waveforms in example 2 correspond to a dimmer data (DM0 to DM9) set to a smaller value. Although t1 does not change, t2 becomes longer. Here, if the dimmer data (DM0 to DM9) is set to $1FF_H$ and the oscillator frequency fosc is 2.4MHz, then t2 can be calculated as follows.

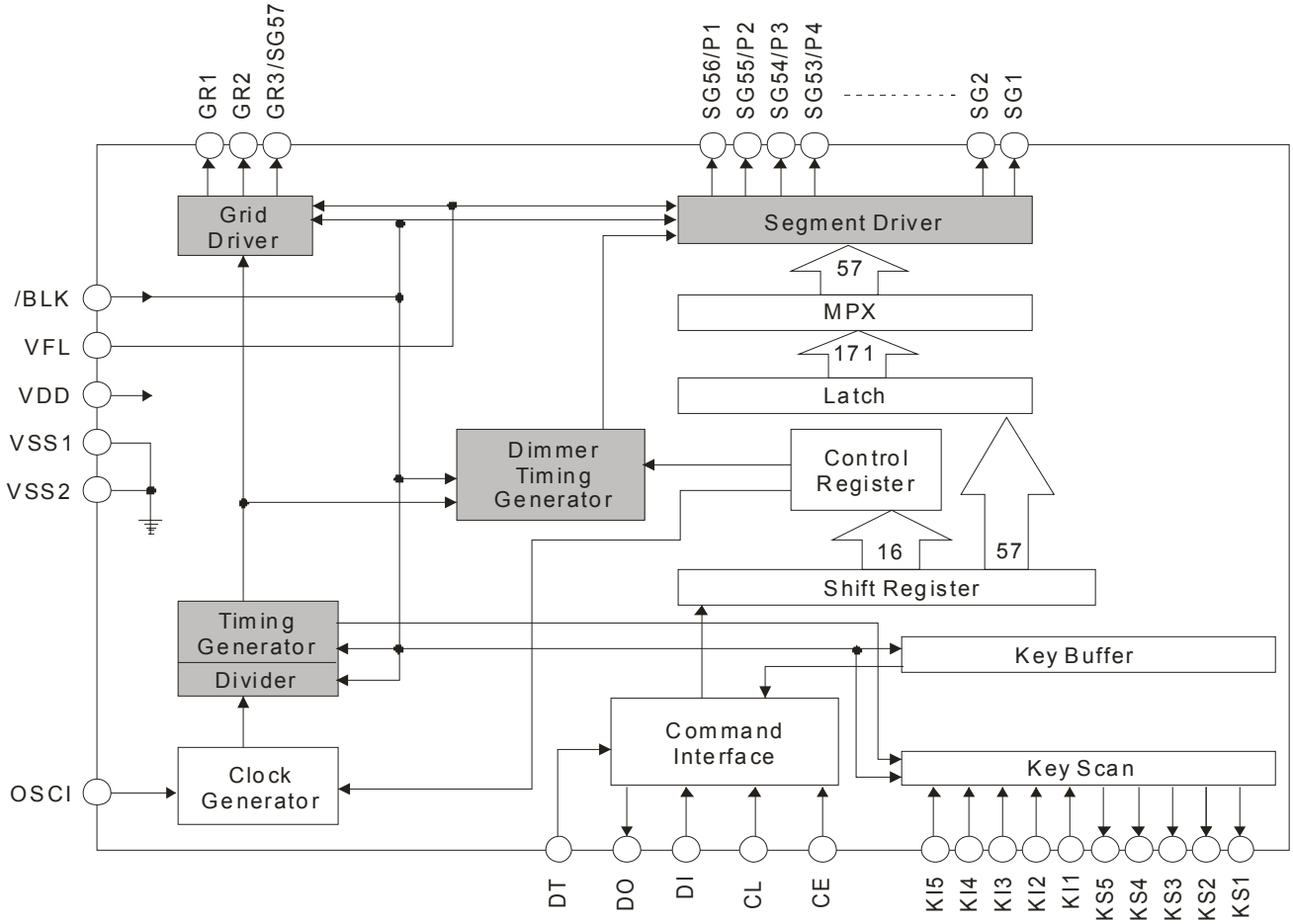
$$t2 = t3 - t1 \times (1FF_H + 1)$$
$$= \frac{1024}{fosc}$$
$$= 0.43[ms]$$

- If the dimmer data (DM0 to DM9) is set to an even smaller value, t2 will become even longer as shown in example 3. Note that t1 does not change in this case as well.

BLOCK STATES DURING THE RESET PERIOD

(when /BLK is low)

- Divider and timing generator
  These circuits are reset and their base clock is stopped.
- Dimmer timing generator
  The circuit is reset and its operation is stopped.
- Digit and segment dividers
  These circuits are reset and the display is turned off (SG1 to SG56 and GR1 to GR3 are set low).
- Key scan
  The circuit is reset, its internal circuits are set to the initial state, and key scanning is disabled.
- Key buffer
  The circuit is reset and all data is set to 0.
- Clock generator
  The state (normal or sleep mode) of this block (the clock oscillator circuit) is determined after the sleep control data (S0 to S1) is transferred.
- CCB interface, shift register, control register, latch, and multiplexer
  The circuits are not reset so that serial data can be input during the reset period.



Block than are reset

OUTPUT PIN STATES DURING THE RESET PERIOD

(when /BLK is low)

Output Pin	State during Reset
SG1 to SG56	L
GR1 to GR3	L
KS1 to KS4	X *1
KS5	H
DO	H *2

Notes:
1. The state of this pin is undefined after power has been applied until the sleep control data (S0 to S1) are transferred.
2. Since this pin is an open-drain output, a pull-up resistor (between 1 and 10KΩ) is required. It remains high during the reset period even if the controller attempts to read the key data.

NOTE ON THE SEGMENT AND DIGIT WAVEFORMS

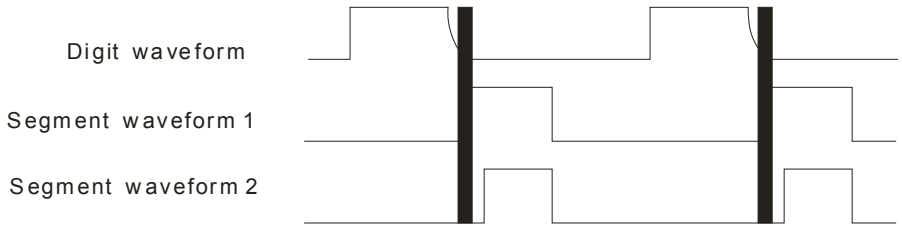


Figure 8

The digit waveform is somewhat deformed due to the VFD panel itself and the circuit wiring. Furthermore, if a segment waveform such as segment waveform 1 in which no dimming is applied is used, the display will glow dimly. Therefore, applications must take this waveform deformation into account and apply adequate dimming such as that shown in segment waveform 2 so that this phenomenon does not occur.

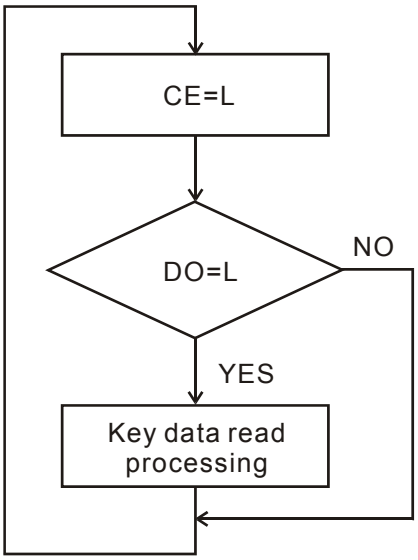
NOTE ON CONTROLLER TRACSFER OF DISPLAY DATA

Since the display data is transferred in three operations as shown in figures 1 & 2, we strongly recommend that applications transfer all the data within a 30ms period to assure display quality.

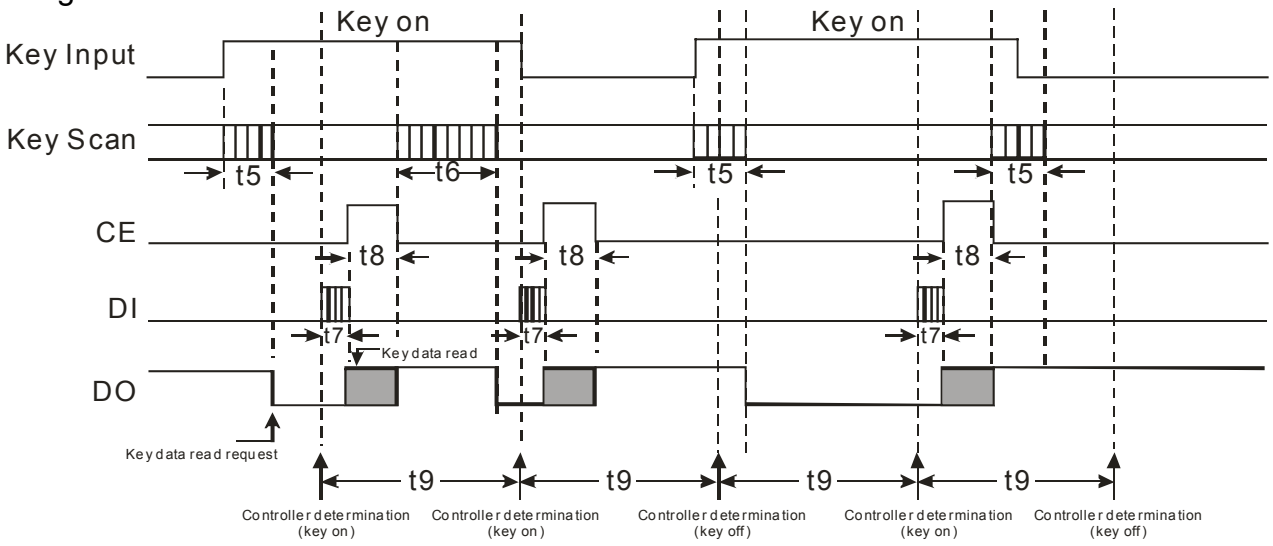
CONTROLLER KEY DATA READOUT PROCEDURE

WHEN THE CONTROLLER USES A TIMER TO READ OUT THE KEY DATA

- Flowchart



- Timing Chart



t5 - Key scan execution time (38400T [s]) when the key data for two key scan operations matches.
t6 - Key scan execution time (76800T [s]) when the key data for the first two key scan operations does not match.
t7 - Key address ($8F_H$) transfer time
t8 - Key data readout time

- Operation

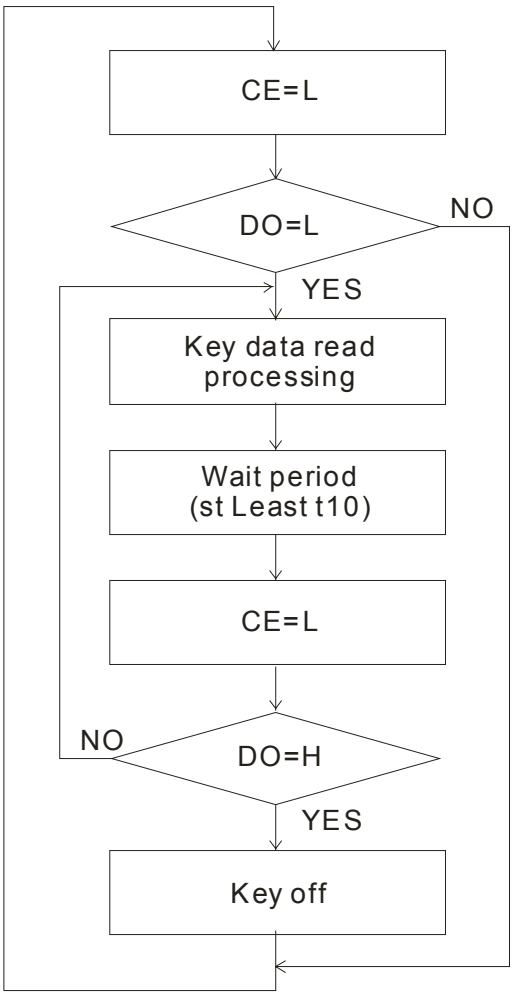
When the controller use timer processing for key on/off determination and key data readout, it must set CE low and check the state of DO at least once every t9 period. If DO is low, the controller must recognize that a key has been pressed and read out the key data.
The period t9 must obey the following inequality:

t9 > t7 + t8 + t6

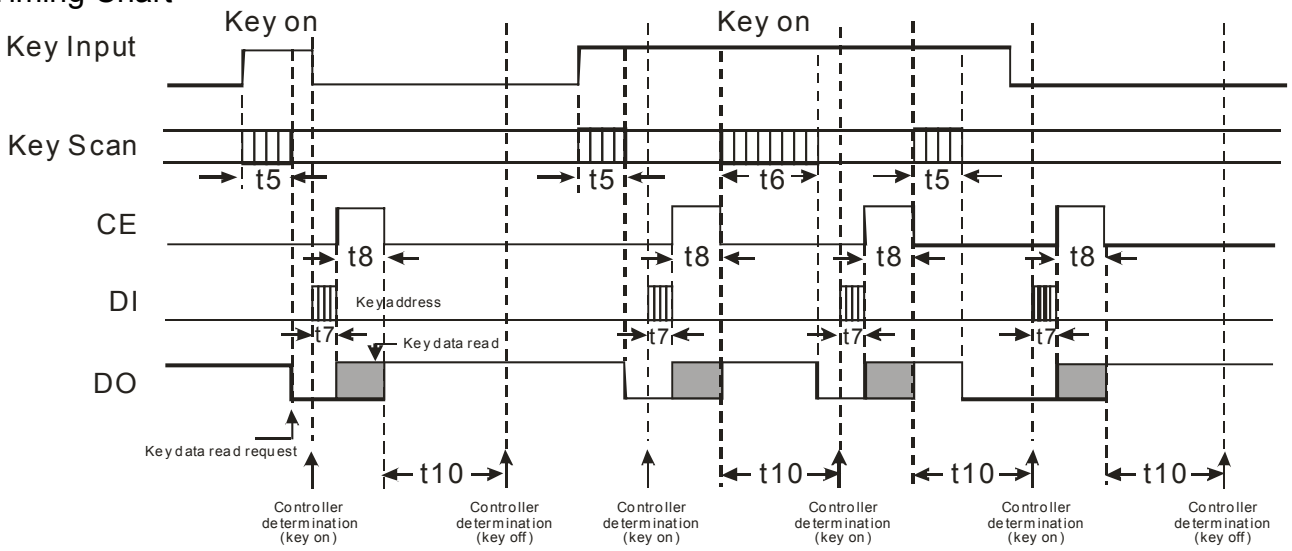
Note: If the controller reads out key data when DO is high, both the key data (KD1 to KD25) and the sleep acknowledge data will be invalid data.

WHEN THE CONTROLLER USES INTERRUPT PROCESSING TO READ OUT THE KEY DATA

- Flowchart



- Timing Chart



t5 - Key scan execution time (38400T [s]) when the key data for two key scan operations matches.
t6 - Key scan execution time (76800T [s]) when the key data for the first two key scan operations does not match.
t7 - Key address ($8F_H$) transfer time

$$T = \frac{1}{fosc}[s]$$

t8 - Key data readout time

- Operation

When the controller use interrupt processing for key on/off determination and key data readout, it must check the state of DO when CE is low, and perform a key data readout if DO is low. The next time the controller checks the on/off states of the keys, it must make that determination at a time t10 after the last readout on the state of DO when CE is low, and then read out the key data.
The time t10 must obey the following inequality:

t10 > t6

Note:
1. If the controller reads out key data when DO is high, both the key data (KD1 to KD25) and the sleep acknowledge data will be invalid data.

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ABSOLUTE MAXIMUM RATINGS

(VSS=0V, Ta=25℃)

Parameter	Symbol	Condition	Rating	Unit
Maximum Supply Voltage	V_{DD} max	V_{DD}	-0.3 ~ +6.5	V
	V_{FL} max	V_{FL}	-0.3 ~ +20	V
Input Voltage	V_{IN1}	DI, CL, CE, /BLK	-0.3 ~ V_{DD}+0.3	V
	V_{IN2}	OSCI, KI1 to KI5	-0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT1}	SG1 to SG52, SG53/P4 to SG56/P1, GR1, GR2, GR3/SG57	-0.3 to V_{FL}+0.3	V
	V_{OUT2}	KS1 to KS5	-0.3 to V_{DD}+0.3	V
	V_{OUT3}	DO	-0.3 ~ V_{DD}+0.3	V
Output Current	I_{OUT1}	SG1 to SG52, SG53/P4 to SG56/P1	6	μA
	I_{OUT2}	GR1, GR2, GR3/SG57	60	mA
	I_{OUT3}	KS1 to KS5	1	mA
Allowable Power Dissipation	Pd max	Ta=85℃	400	mW
Operating Temperature	Topr	-	-40 to +85	℃
Storage Temperature	Tstg	-	-65 to +150	℃

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ALLOWABLE OPERATING RANGES

(Ta=25℃, V_{DD}=3.3 to 5V, V_{FL}=18V, V_{SS}=0V)

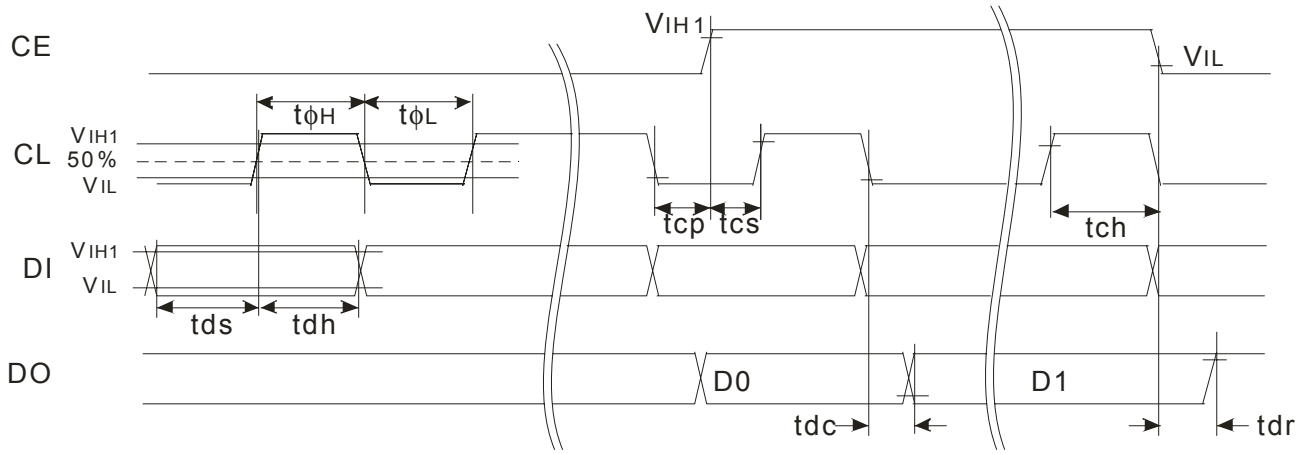
Parameter	Symbol	Condition		Min	Typ	Max	Unit
Supply Voltage	V_{DD}	V_{DD}		3	5.0	5.5	V
	V_{FL}	V_{FL}		8	12	18	V
Input High-Level Voltage	V_{IH1}	DI, CL, CE, /BLK		0.8 V_{DD}	-	5.5	V
	V_{IH2}	KI1 to KI5		0.6 V_{DD}	-	V_{DD}	V
Low-Level Input Voltage	V_{IL}	DI, CL, CE, /BLK, KI1 to KI5		0		0.2 V_{DD}	V
Guaranteed Oscillator Range	fosc	OSCI		0.9	2.4	3.7	MHz
Recommended External Resistance	R_{OSC}	OSCI	V_{DD}=5V	-	12	-	KΩ
			V_{DD}=3.3V	-	7.5	-	
Recommended External Capacitance	C_{OSC}	OSCI		15	33	100	pF
Clock Low-Level Pulse Width	$t_{ØL}$	CL: Figure 9	5V	160	-	-	ns
			3.3V	240	-	-	
Clock High-Level Pulse Width	$t_{ØH}$	CL: Figure 9	5V	160	-	-	ns
			3.3V	240	-	-	
Data Setup Time	t_{ds}	DI, CL: Figure 9	5V	160	-	-	ns
			3.3V	240	-	-	
Data Hold Time	t_{dh}	DI, CL: Figure 9	5V	160	-	-	ns
			3.3V	240	-	-	
CE Wait Time	t_{cp}	CE, CL: Figure 9	5V	160	-	-	ns
			3.3V	240	-	-	
CE Setup Time	t_{cs}	CE, CL: Figure 9	5V	160	-	-	ns
			3.3V	240	-	-	
CE Hold Time	t_{ch}	CE, CL: Figure 9	5V	160	-	-	ns
			3.3V	240	-	-	
DO Output Delay Time	t_{dc}	DO, R_{PU}=4.7KΩ, C_L=10pf*: Figure 9	5V	-	-	1.5	µs
			3.3V	-	-	1.6	
DO Rise Time	t_{dr}	DO, R_{PU}=4.7KΩ, C_L=10pf*: Figure 9	5V	-	-	1.5	µs
			3.3V	-	-	1.6	
/BLK Switching Time	t_C	/BLK, CE: Figure 6	5V	10	-	-	µs
			3.3V	14	-	-	

ELECTRICAL CHARACTERISTICS

(Ta=25℃, V_{DD}=3.3 to 5V, V_{FL}=18V, V_{SS}=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
High Level Input Current	I_{IH}	DI, CL, CE, /BLK: V_{IN}=5.0V		-	-	5	μA
Low Level Input Current	I_{IL}	DI, CL, CE, /BLK, V_{IN}=0V		-5	-	-	μA
Input Floating Voltage	V_{IF}	KI1~KI5		-	-	0.05V_{DD}	V
Pull-down Resistance	R_{PD}	KI1~KI5: V_{DD}=5.0V		50	100	250	KΩ
Output Off Leakage Current	I_{OFFH}	DO: V_O=5.0V		-	-	5	μA
High Level Output Voltage	V_{OH1}	SG1~SG52, SG53/P4~SG56/P1: I_O=-2mA		V_{FL}-0.6	-	-	V
	V_{OH2}	GR1, GR2, GR3/SG57: I_O=-50mA		V_{FL}-1.3	-	-	V
	V_{OH3}	KS1~KS5: I_O=-500μA	5V	V_{DD}-1.2	V_{DD}-0.5	V_{DD}-0.2	V
			3.3V	V_{DD}-1.2	V_{DD}-0.5	V_{DD}-0.2	
Low Level Output Voltage	V_{OL1}	SG1~SG52, SG53/P4~SG56/P1, GR1, GR2, GR3/SG57: I_O=50μA		-	-	0.5	V
	V_{OL2}	KS1~KS5: I_O=25μA	5V	0.2	0.5	1.5	V
			3.3V	0.2	0.5	1.2	
	V_{OL3}	DO: I_O=1mA	5V	-	0.1	0.5	V
			3.3V	-	0.1	0.4	
Oscillator Frequency	f_{OSC}	R_{OSC}=12KΩ, C_{OSC}=33pF	5V	-	2.4	-	MHZ
		R_{OSC}=7.5KΩ, C_{OSC}=33pF	3.3V	-	1.7	-	
Hysteresis Voltage	V_H	DI, CL, CE, /BLK, KI1~KI5		-	0.1V_{DD}	-	V
Current Drain	I_{DD1}	Sleep mode, Figure 1~4	C0~C2=0 Normal mode	-	-	100	μA
			C0~C2=1 Test mode	-	-	5	
	I_{DD2}	Output open: f_{OSC}=2.4MHz		-	-	10	mA

When stopped with CL at the low level



When stopped with CL at the HIGH level

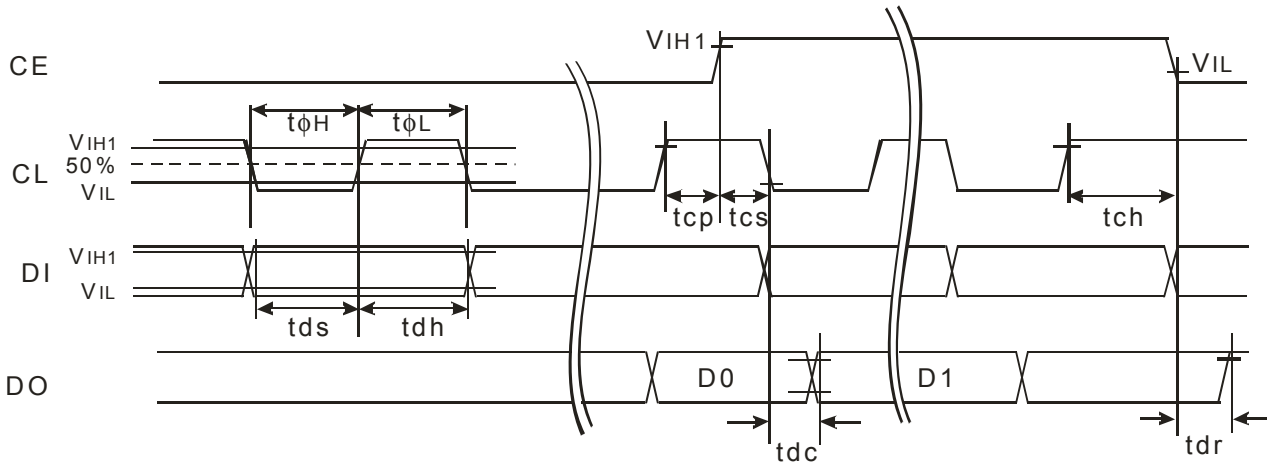
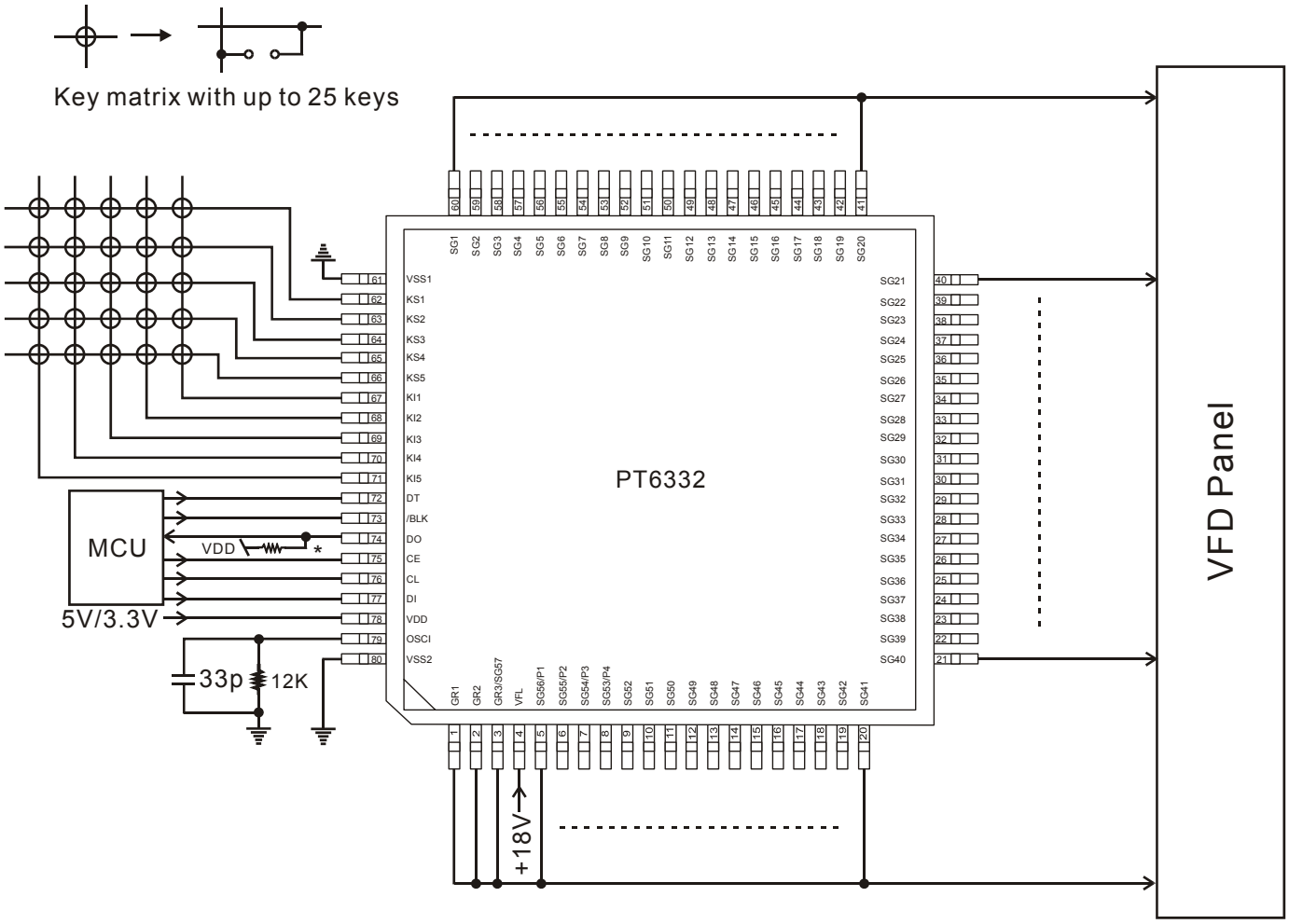


Figure 9

APPLICATION CIRCUIT



Note: *- Since DO is an open-drain output, a pull-up resistor is required. Select a value in the range 1 to 10KΩ that is most appropriate for the capacitance of the external lines so that the waveform is not distorted.

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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6332-LQ	80 Pin, LQFP	PT6332-LQ

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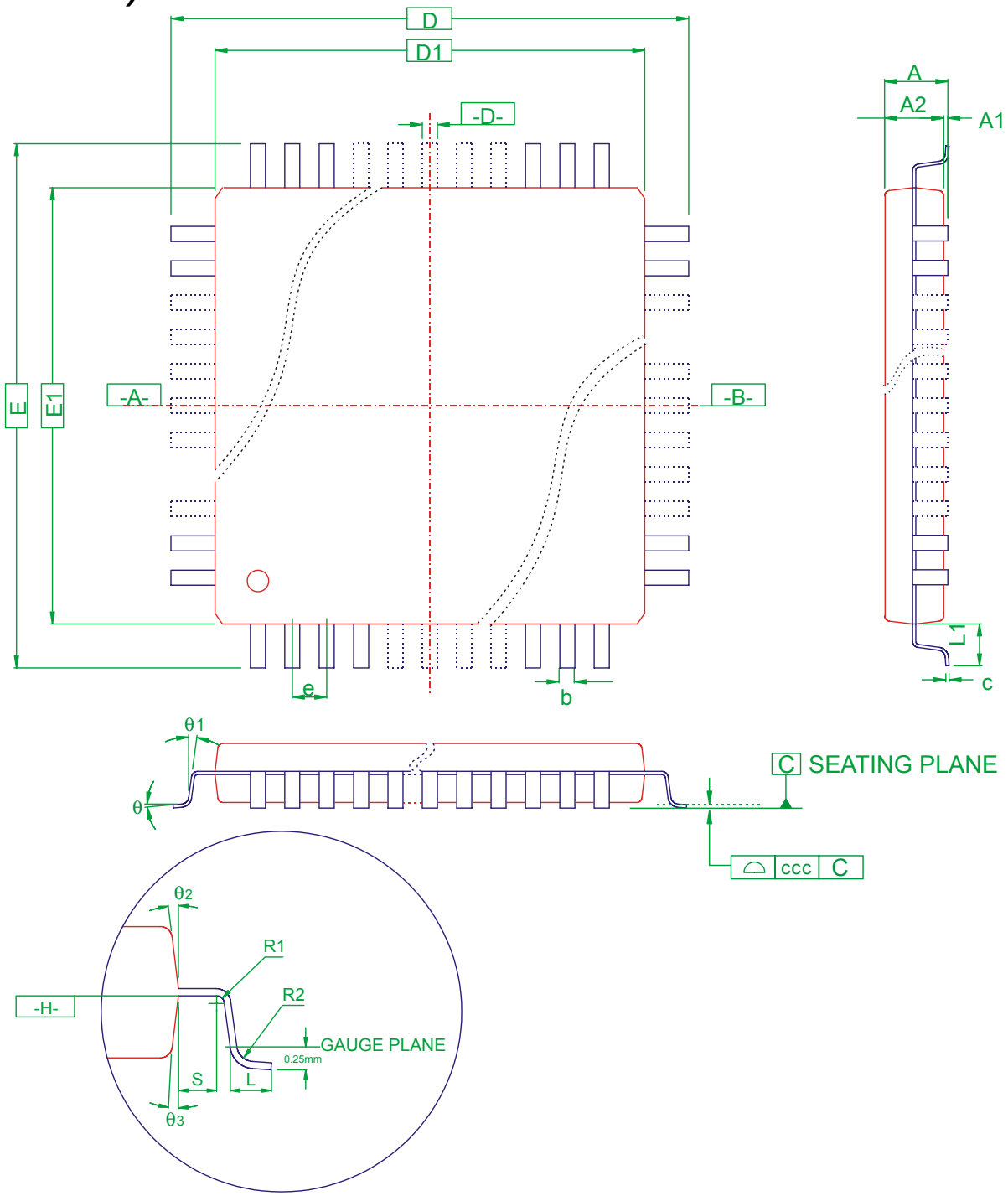
PACKAGE INFORMATION

80 PINS, LQFP (BODY SIZE: 12MMx12MM, PITCH: 0.50MM, THK: 1.40MM)



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
D		14.00 BSC.	
D1		12.00 BSC.	
e		0.50 BSC.	
E		14.00 BSC.	
E1		12.00 BSC.	
S	0.20	-	-
R1	0.08	-	-
R2	0.08	-	0.20
L	0.45	0.60	0.75
L1		1.00 REF.	
C	0.09	-	0.20
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
ccc		0.08	

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. The top package body may be smaller than the bottom package size as much as 0.15mm.
3. Datum A-B and D to be determined at the datum plane H.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25mm per side. d1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Controlling Dimensions: Millimeters
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4mm and 0.5mm pitch package.
7. A1 is defined as the distance from the seating plane to the lowest point on the package body.
8. Refer to JEDEC MS-026 Variation BDD.

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