# CY2XP24

# Crystal to LVPECL Clock Generator

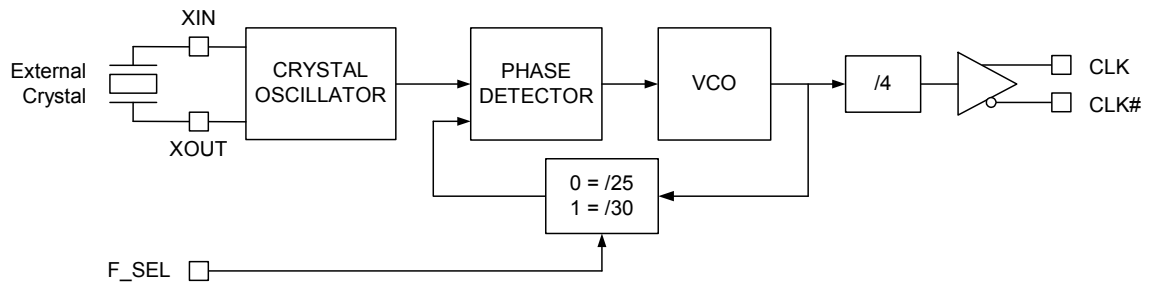
## Features

- One LVPECL Output Pair
- Selectable Output Frequency: 156.25 MHz or 187.5 MHz
- External Crystal Frequency: 25 MHz
- Low RMS Phase Jitter at 156.25 MHz, using 25 MHz crystal (1.875 MHz to 20 MHz): 0.33 ps (typical)
- Pb-Free 8-Pin TSSOP Package
- Supply Voltage: 3.3V or 2.5V
- Commercial and Industrial Temperature Ranges

## Functional Description

The CY2XP24 is a PLL (Phase Locked Loop) based high performance clock generator. It is optimized to generate 10 Gb Ethernet, Fibre Channel, and other high performance clock frequencies. It produces an output frequency that is either 6.25 times or 7.5 times the crystal frequency. It uses Cypress's low noise VCO technology to achieve less than 1 ps typical RMS phase jitter, that meets both 10Gb Ethernet, Fibre Channel, and SATA jitter requirements. The CY2XP24 has a crystal oscillator interface input and one LVPECL output pair.

## Logic Block Diagram




## Pinouts

**Figure 1. Pin Diagram - 8 Pin TSSOP**


**Table 1. Pin Definitions - 8 Pin TSSOP**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1, 8 | VDD | Power | 3.3V or 2.5V power supply. All supply current flows through pin 1 |
| 2 | VSS | Power | Ground |
| 3, 4 | XOUT, XIN | XTAL Output and Input | Parallel resonant crystal interface |
| 5 | F_SEL | CMOS Input | Frequency select. When HIGH, the output frequency is 7.5 times of the crystal frequency. When LOW, the output frequency is 6.25 times of the crystal frequency |
| 6,7 | CLK#, CLK | LVPECL Output | Differential clock output |

## Frequency Table

| Inputs | | PLL Multiplier Value | Output Frequency (MHz) |
|---|---|---|---|
| Crystal Frequency (MHz) | F_SEL | | |
| 25 | 1 | 7.5 | 187.5 |
| 25 | 0 | 6.25 | 156.25 |

## Absolute Maximum Conditions

| Parameter | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | –0.5 | 4.4 | V |
| $V_{IN}$[1] | Input Voltage, DC | Relative to $V_{SS}$ | –0.5 | $V_{DD}$ + 0.5 | V |
| $T_S$ | Temperature, Storage | Non operating | –65 | 150 | °C |
| $T_J$ | Temperature, Junction | | | 135 | °C |
| $ESD_{HBM}$ | ESD Protection (Human Body Model) | JEDEC STD 22-A114-B | 2000 | | V |
| UL–94 | Flammability Rating | At 1/8 in. | V–0 | | |
| $\Theta_{JA}$[2] | Thermal Resistance, Junction to Ambient | 0 m/s airflow | 100 | | °C/W |
| | | 1 m/s airflow | 91 | | |
| | | 2.5 m/s airflow | 87 | | |

## Operating Conditions

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 3.3V Supply Voltage | 3.135 | 3.465 | V |
| | 2.5V Supply Voltage | 2.375 | 2.625 | V |
| $T_A$ | Ambient Temperature, Commercial | 0 | 70 | °C |
| | Ambient Temperature, Industrial | -40 | 85 | °C |
| $T_{PU}$ | Power up time for all $V_{DD}$ to reach minimum specified voltage (ensure power ramps are monotonic) | 0.05 | 500 | ms |

## DC Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$[3] | Power Supply Current with output terminated | $V_{DD}$ = 3.465V, $F_{OUT}$ = 187.5 MHz, output terminated | – | – | 150 | V |
| | | $V_{DD}$ = 2.625V, $F_{OUT}$ = 187.5 MHz, output terminated | – | – | 145 | V |
| $V_{OH}$ | LVPECL Output High Voltage | $V_{DD}$ = 3.3V or 2.5V, $R_{TERM}$ = 50Ω to $V_{DD}$ – 2.0V | $V_{DD}$ –1.15 | – | $V_{DD}$ –0.75 | V |
| $V_{OL}$ | LVPECL Output Low Voltage | $V_{DD}$ = 3.3V or 2.5V, $R_{TERM}$ = 50Ω to $V_{DD}$ – 2.0V | $V_{DD}$ –2.0 | – | $V_{DD}$ –1.625 | V |
| $V_{OD1}$ | LVPECL Peak-to-Peak Output Voltage Swing | $V_{DD}$ = 3.3V or 2.5V, $R_{TERM}$ = 50Ω to $V_{DD}$ – 2.0V | 600 | – | 1000 | mV |
| $V_{OD2}$ | LVPECL Output Voltage Swing ($V_{OH}$ - $V_{OL}$) | $V_{DD}$ = 2.5V, $R_{TERM}$ = 50Ω to $V_{DD}$ – 1.5V | 500 | – | 1000 | mV |

**Note**
1. The voltage on any input or I/O pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
3. $I_{DD}$ includes approximately 24 mA of current that is dissipated externally in the output termination resistors.

## DC Electrical Characteristics (continued)

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OCM}$ | LVPECL Output Common Mode Voltage ($V_{OH}$ + $V_{OL}$)/2 | $V_{DD}$ = 2.5V, $R_{TERM}$ = 50Ω to $V_{DD}$ – 1.5V | 1.2 | – | – | V |
| $V_{IH}$ | Input High Voltage | | 0.7*$V_{DD}$ | – | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | –0.3 | – | 0.3*$V_{DD}$ | V |
| $I_{IH}$ | Input High Current | F_SEL = $V_{DD}$ | – | – | 115 | µA |
| $I_{IL}$ | Input Low Current | F_SEL = $V_{SS}$ | –50 | – | – | µA |
| $C_{IN}$ | Input Capacitance | | | 15 | | pF |
| $C_{INX}$ | Pin Capacitance, XIN & XOUT | | | 4.5 | | pF |

## AC Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{OUT}$ | Output Frequency | | 156.25 | – | 187.5 | MHz |
| $T_R$, $T_F$[5] | Output Rise/Fall time | 20% to 80% of full swing | – | 500 | – | ps |
| $T_{Jitter(\phi)}$[8] | RMS Phase Jitter (Random) | 156.25 MHz, (1.875–20 MHz), 3.3V | – | 0.33 | – | ps |
| $T_{DC}$[9] | Duty Cycle | Measured at zero crossing point | 45 | – | 55 | % |
| $T_{LOCK}$ | Startup Time | Time for CLK to reach valid frequency measured from the time $V_{DD}$ = $V_{DD}$(min.) or from F_SEL changing | – | – | 10 | ms |

## Recommended Crystal Specifications[6]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| Mode | Mode of Oscillation | Fundamental | | |
| F | Frequency | 25 | 25 | MHz |
| ESR | Equivalent Series Resistance | – | 50 | Ω |
| $C_0$ | Shunt Capacitance | – | 7 | pF |

**Notes**
4. Outputs are terminated with 50Ω to $V_{DD}$ – 2V. Refer to Figure 2 on page 4 and Figure 3 on page 4.
5. Refer to Figure 7 on page 5.
6. Characterized using an 18 pF parallel resonant crystal.
7. Not 100% tested, guaranteed by design and characterization.
8. Refer to Figure 4 on page 4.
9. Refer to Figure 7 on page 5.

## Parameter Measurements

**Figure 2. 3.3V Output Load AC Test Circuit**

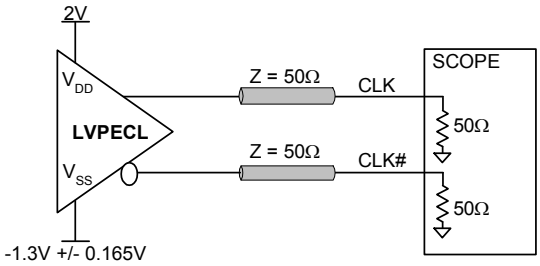



**Figure 3. 2.5V Output Load AC Test Circuit**

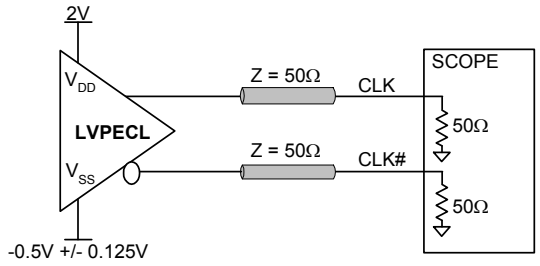



**Figure 4. Output DC Parameters**

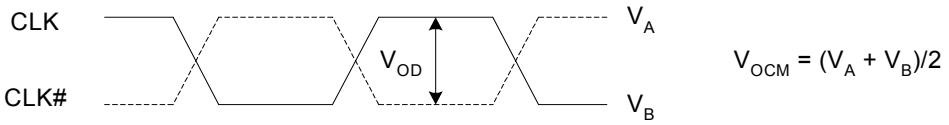



**Figure 5. Output Rise and Fall Time**

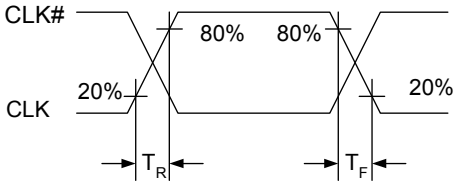



**Figure 6. RMS Phase Jitter**

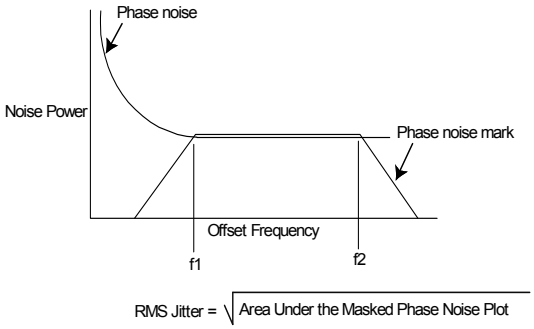
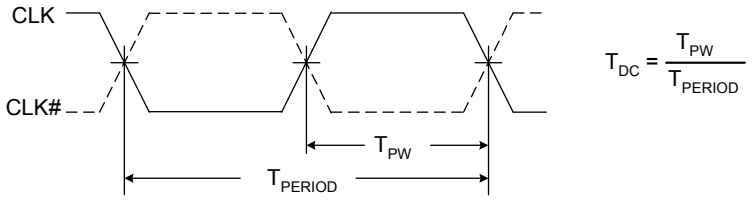


**Figure 7. Output Duty Cycle**

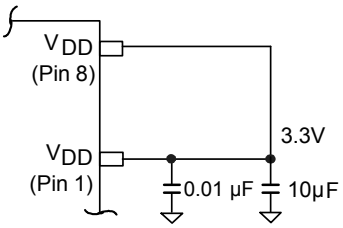



## Application Information

### Power Supply Filtering Techniques

As in any high speed analog circuitry, noise at the power supply pins can degrade performance. To achieve optimum jitter performance, use good power supply isolation practices. Figure 8 illustrates a typical filtering scheme. Because all current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 µF ceramic chip capacitor is also located close to this pin to provide a short and low impedance AC path to ground. A 1 to 10 µF ceramic or tantalum capacitor is located in the general vicinity of this device and may be shared with other devices.

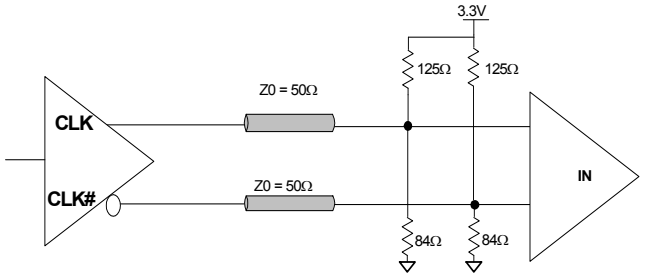
**Figure 8. Power Supply Filtering**




### Termination for LVPECL Output

The CY2XP24 implements its LVPECL driver with a current steering design. For proper operation, it requires a 50 ohm dc termination on each of the two output signals. For 3.3V operation, this data sheet specifies output levels for termination to $V_{DD}$–2.0V. This termination voltage can also be used for $V_{DD}$ = 2.5V operation, or it can be terminated to $V_{DD}$-1.5V. Note that it is also possible to terminate with 50 ohms to ground ($V_{SS}$), but the high and low signal levels differ from the data sheet values. Termination resistors are best located close to the destination device. To avoid reflections, trace characteristic impedance ($Z_0$) should match the termination impedance. Figure 9 shows a standard termination scheme.

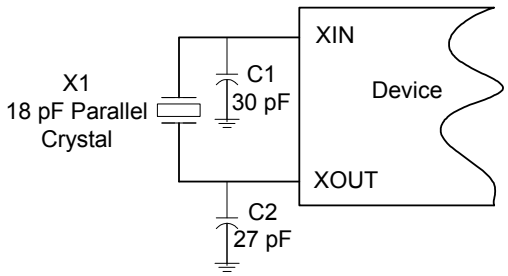
**Figure 9. LVPECL Output Termination**




### Crystal Input Interface

The CY2XP24 is characterized with 18 pF parallel resonant crystals. The capacitor values shown in Figure 10 are determined using a 25 MHz 18 pF parallel resonant crystal and are chosen to minimize the ppm error. Note that the optimal values for C1 and C2 depend on the parasitic trace capacitance and are therefore layout dependent.

**Figure 10. Crystal Input Interface**

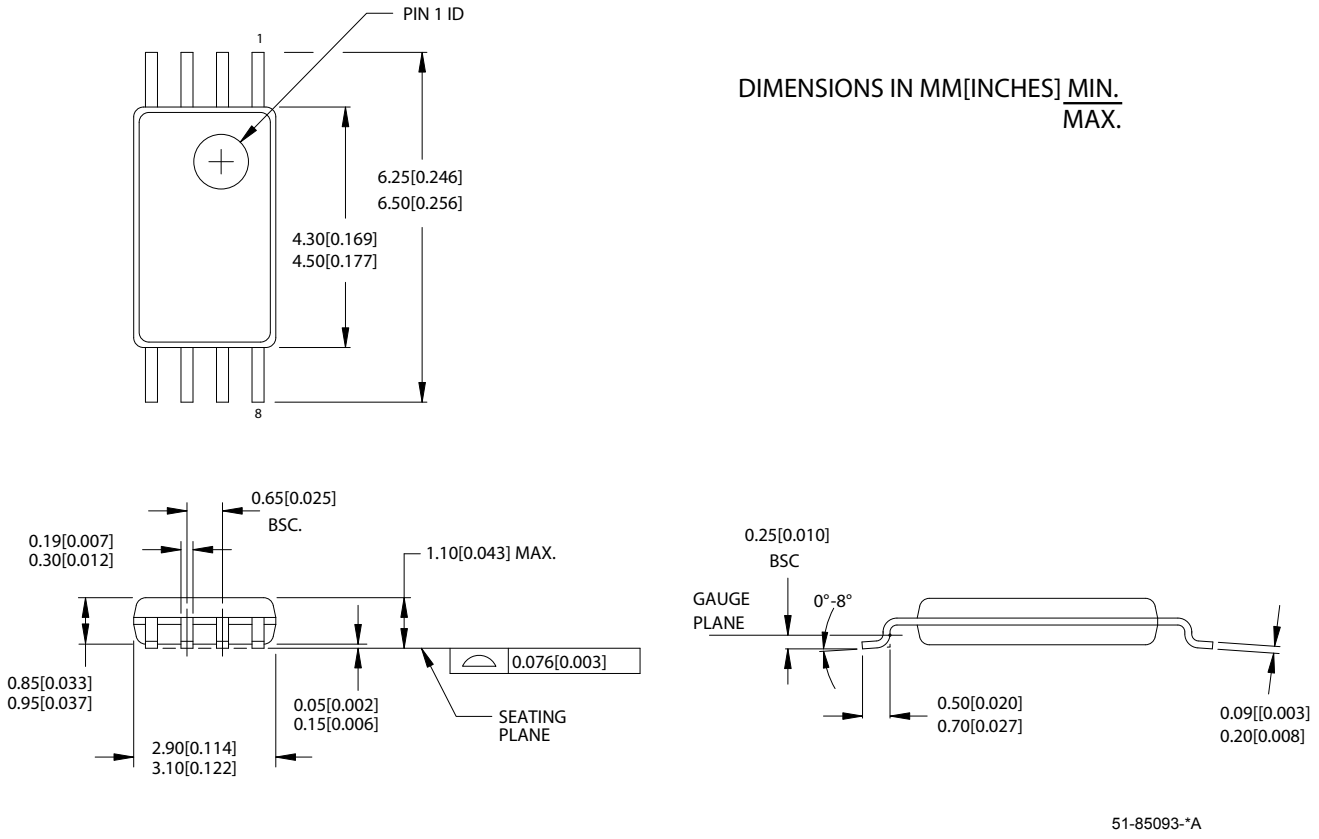


## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| CY2XP24ZXC | 8-Pin TSSOP | Commercial, 0°C to 70°C |
| CY2XP24ZXCT | 8-Pin TSSOP–Tape and Reel | Commercial, 0°C to 70°C |
| CY2XP24ZXI | 8-Pin TSSOP | Industrial, -40°C to 85°C |
| CY2XP24ZXIT | 8-Pin TSSOP–Tape and Reel | Industrial, -40°C to 85°C |

## Package Drawing and Dimensions

**Figure 11. 8-Pin Thin Shrunk Small Outline Package (4.40 MM Body) Z8**



## Document History Page

| Document Title: CY2XP24 Crystal to LVPECL Clock Generator<br>Document Number: 001-15705 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 1285703 | See ECN | WWZ/KVM/ ARI | New data sheet |
| *A | 1451704 | See ECN | WWZ/AESA | Added I-temp devices |
| *B | 2669117 | 03/05/2009 | KVM/AESA | Changed crystal frequency and output frequencies<br>Updated phase jitter value<br>Rise & fall times changed from 350 ps to 500 ps (typ.)<br>Junction temperature changed from 125°C to 135°C<br>Changed IIL and IIH values<br>Entered value for IDD<br>Removed MSL spec<br>Changed Data Sheet Status to Final |
| *C | 2700242 | 04/30/2009 | KVM/PYRS | Typos: changed VCC to VDD, changed ps to MHz<br>Changed footnote about external power dissipation<br>Reformatted AC and DC tables<br>Changed LVPECL parameters from VPP to VOD and VOCM<br>Added CINX spec<br>Added IDD for 2.5V<br>Added TLOCK timing<br>Revised text in Application Information section<br>Changed recommended crystal load capacitor values |
| *D | 2718433 | 06/12/2009 | WWZ/HMT | No change. Submit to ECN for product launch. |

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