

103 dB, 192 kHz 6-Channel D/A Converter

Features

- ◆ Advanced Multi-bit Delta Sigma Architecture
- ◆ 24-bit Conversion
- ◆ Automatic Detection of Sample Rates up to 192 kHz
- ◆ 103 dB Dynamic Range
- ◆ -88 dB THD+N
- ◆ Single-Ended Output Architecture
- ◆ Direct Stream Digital® (DSD™) Mode
 - Non-Decimating Volume Control
 - On-Chip 50 kHz Filter
 - Matched PCM and DSD Analog Output Levels
- ◆ Selectable Digital Filters
- ◆ Volume Control with 1/2-dB Step Size and Soft Ramp
- ◆ Low Clock-Jitter Sensitivity
- ◆ +5 V Analog Supply, +2.5 V Digital Supply
- ◆ Separate 1.8 to 5 V Logic Supplies for the Control and Serial Ports

Description

The CS4364 is a complete 6-channel digital-to-analog system. This D/A system includes digital de-emphasis, half-dB step size volume control, ATAPI channel mixing, selectable fast and slow digital interpolation filters followed by an oversampled, multi-bit delta sigma modulator which includes mismatch shaping technology that eliminates distortion due to capacitor mismatch. Following this stage is a multi-element switched capacitor stage and low-pass filter with single-ended analog outputs.

The CS4364 also has a proprietary DSD processor which allows for volume control and 50 kHz on-chip filtering without an intermediate decimation stage. It also offers an optional path for direct DSD conversion by directly using the multi-element switched capacitor array.

The CS4364 accepts PCM data at sample rates from 4 kHz to 216 kHz, DSD audio data, and delivers excellent sound quality. These features are ideal for multi-channel audio systems including SACD players, A/V receivers, digital TV's, mixing consoles, effects processors, and sound cards.

This product is available in 48-pin LQFP package in Commercial (-40°C to +85°C) temperature grade. See "Ordering Information" on page 49 for complete details.

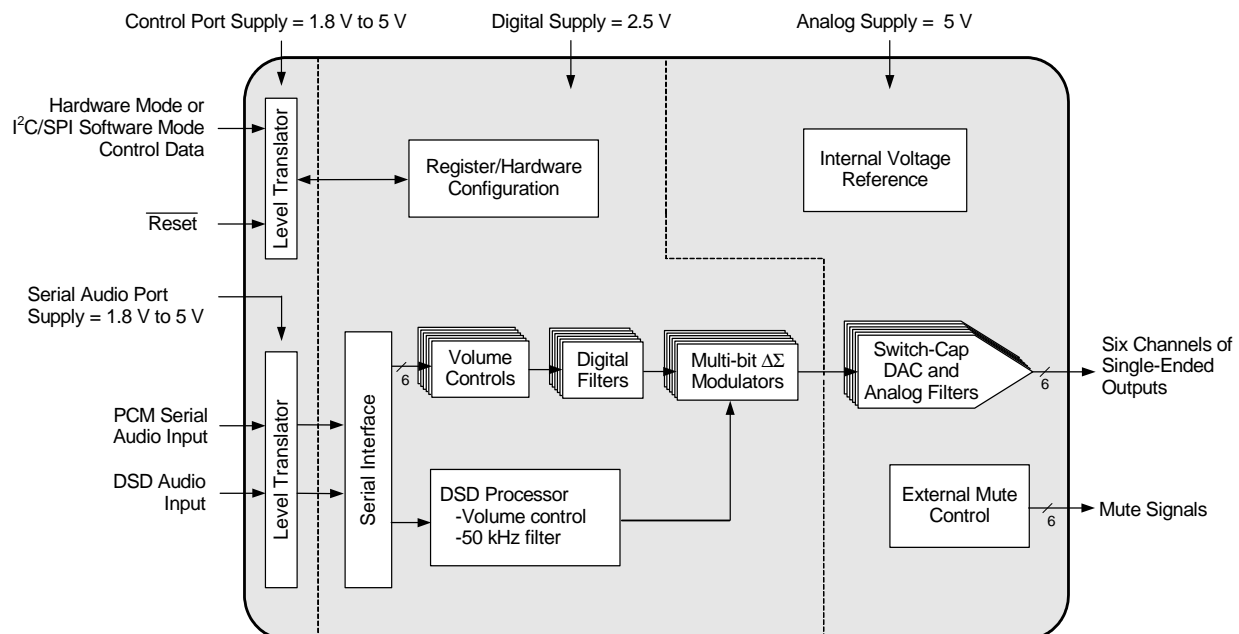


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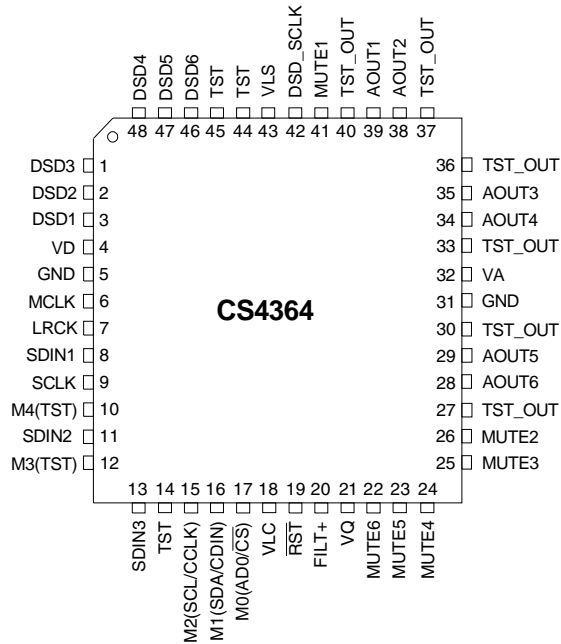
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1. PIN DESCRIPTION



Pin Name	#	Pin Description
VD	4	Digital Power (Input) - Positive power supply for the digital section. Refer to the Recommended Operating Conditions for appropriate voltages.
GND	5 31	Ground (Input) - Ground reference. Should be connected to analog ground.
MCLK	6	Master Clock (Input) - Clock source for the delta-sigma modulator and digital filters. Table 1 illustrates several standard audio sample rates and the required master clock frequencies.
LRCK	7	Left Right Clock (Input) - Determines which channel, Left or Right, is currently active on the serial audio data line. The frequency of the left/right clock must be at the audio sample rate, Fs.
SDIN1 SDIN2 SDIN3	8 11 13	Serial Data Input (Input) - Input for two's complement serial audio data.
SCLK	9	Serial Clock (Input) - Serial clocks for the serial audio interface.
TST	14 44 45	Test - These pins need to be tied to analog ground.
$\overline{\text{RST}}$	19	Reset (Input) - The device enters a low power mode and all internal registers are reset to their default settings when low.
VA	32	Analog Power (Input) - Positive power supply for the analog section. Refer to the Recommended Operating Conditions for appropriate voltages.
VLS	43	Serial Audio Interface Power (Input) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
VLC	18	Control Port Power (Input) - Determines the required signal level for the control port and hardware mode configuration pins. Refer to the Recommended Operating Conditions for appropriate voltages.
VQ	21	Quiescent Voltage (Output) - Filter connection for internal quiescent voltage.

Pin Name	#	Pin Description
FILT+	20	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits. Requires the capacitive decoupling to analog ground as shown in the Typical Connection Diagram.
AOUT1 AOUT2 AOUT3 AOUT4 AOUT5 AOUT6	39 38 35 34 29 28	Analog Output (Output) - The full scale analog output level is specified in the Analog Characteristics specification table.
MUTE1 MUTE2 MUTE3 MUTE4 MUTE5 MUTE6	41 26 25 24 23 22	Mute Control (Output) - These pins are intended to be used as a control for external mute circuits on the line outputs to prevent the clicks and pops that can occur in any single supply system.
TST_OUT	40, 37 36, 33 30, 27	Test Output - These pins need to be floating and not connected to any trace or plane.
Hardware Mode Definitions		
M0 M1 M2 M3 M4	17 16 15 12 10	Mode Selection (Input) - Determines the operational mode of the device as detailed in Tables 4 and 5 .
Software Mode Definitions		
SCL/CCLK	15	Serial Control Port Clock (Input) - Serial clock for the serial control port. Requires an external pull-up resistor to the logic interface voltage in I ² C [®] mode as shown in the Typical Connection Diagram.
SDA/CDIN	16	Serial Control Port Data (Input/Output) - SDA is a data I/O line in I ² C mode and is open drain, requiring an external pull-up resistor to the logic interface voltage, as shown in the Typical Connection Diagram; CDIN is the input data line for the control port interface in SPI [™] mode.
AD0/ $\overline{\text{CS}}$	17	Address Bit 0 (I²C) / Control Port Chip Select (SPI) (Input) - AD0 is a chip address pin in I ² C mode; $\overline{\text{CS}}$ is the chip select signal for SPI mode.
TST	10 12	Test - These pins need to be tied to analog ground.
DSD Definitions		
DSD1, DSD2 DSD3, DSD4 DSD5, DSD6	3, 2 1, 48 47, 46	Direct Stream Digital Input (Input) - Input for Direct Stream Digital serial audio data.
DSD_SCLK	42	DSD Serial Clock (Input) - Serial clock for the Direct Stream Digital serial audio interface.

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Typ	Max	Units	
DC Power Supply	Analog power	VA	4.75	5.0	5.25	V
	Digital internal power	VD	2.37	2.5	2.63	V
	Serial data port interface power	VLS	1.71	5.0	5.25	V
	Control port interface power	VLC	1.71	5.0	5.25	V
Ambient Operating Temperature (Power Applied)	-CQZ	T _A	-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units	
DC Power Supply	Analog power	VA	-0.3	6.0	V
	Digital internal power	VD	-0.3	3.2	V
	Serial data port interface power	VLS	-0.3	6.0	V
	Control port interface power	VLC	-0.3	6.0	V
Input Current	Any Pin Except Supplies	I _{in}	-	±10	mA
Digital Input Voltage	Serial data port interface	V _{IND-S}	-0.3	VLS+ 0.4	V
	Control port interface	V _{IND-C}	-0.3	VLC+ 0.4	V
Ambient Operating Temperature (power applied)		T _{op}	-55	125	°C
Storage Temperature		T _{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS

Test Conditions (unless otherwise indicated): $V_A = V_{LS} = V_{LC} = 5\text{ V}$; $V_D = 2.5\text{ V}$; $T_A = 25\text{ °C}$; Full-Scale 997 Hz input sine wave (Note 1); Tested under max ac-load resistance; Valid with FILT+ and VQ capacitors as shown in “Typical Connection Diagram” on page 18; Measurement Bandwidth 10 Hz to 20 kHz.

Parameters			Symbol	Min	Typ	Max	Unit
FS = 48 kHz, 96 kHz, 192 kHz and DSD							
Dynamic Range	24-bit	A-weighted		97	103	-	dB
		unweighted		94	100	-	dB
	16-bit (Note 2)	A-weighted		-	97	-	dB
		unweighted		-	94	-	dB
Total Harmonic Distortion + Noise (Note 2)	24-bit	-0 dB	THD+N	-	-88	-82	dB
		-20 dB		-	-80	-74	dB
		-60 dB		-	-40	-34	dB
	16-bit	0 dB		-	-88	-	dB
		-20 dB		-	-74	-	dB
		-60 dB		-	-34	-	dB
Idle Channel Noise / Signal-to-noise ratio				-	100	-	dB
Interchannel Isolation			(1 kHz)	-	110	-	dB
DC Accuracy							
Interchannel Gain Mismatch				-	0.1	-	dB
Gain Drift				-	100	-	ppm/°C
Analog Output							
Full Scale Differential- Output Voltage (Note 3)	PCM, DSD processor Direct DSD Mode		V_{FS}	$64\% \cdot V_A$ $47\% \cdot V_A$	$66\% \cdot V_A$ $48\% \cdot V_A$	$68\% \cdot V_A$ $49\% \cdot V_A$	Vpp Vpp
		Output Impedance	Z_{OUT}	-	130	-	Ω
Max DC Current draw from an AOUT pin			I_{OUTmax}	-	1.0	-	mA
Min AC-Load Resistance			R_L	-	3	-	k Ω
Max Load Capacitance			C_L	-	100	-	pF
Quiescent Voltage			V_Q	-	50% V_A	-	VDC
Max Current draw from V_Q			I_{QMAX}	-	10	-	μA

Notes:

1. One-half LSB of triangular PDF dither is added to data.
2. Performance limited by 16-bit quantization noise.
3. V_{FS} is tested under load R_L and includes attenuation due to Z_{OUT}

POWER AND THERMAL CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units	
Power Supplies						
Power Supply Current (Note 4)	normal operation, VA= 5 V	I_A	-	63	69	mA
	VD= 2.5 V	I_D	-	18	22	mA
	(Note 5) Interface current, VLC=5 V	I_{LC}	-	2	-	μ A
	VLS=5 V	I_{LS}	-	84	-	μ A
(Note 6) power-down state (all supplies)	I_{pd}	-	200	-	μ A	
Power Dissipation (Note 4)	VA = 5 V, VD = 2.5 V		-	360	400	mW
	normal operation (Note 6) power-down		-	1	-	mW
Package Thermal Resistance	multi-layer	θ_{JA}	-	48	-	$^{\circ}$ C/Watt
	dual-layer	θ_{JA}	-	65	-	$^{\circ}$ C/Watt
		θ_{JC}	-	15	-	$^{\circ}$ C/Watt
Power Supply Rejection Ratio (Note 7)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	40	-	dB

Notes:

4. Current consumption increases with increasing FS within a given speed mode and is signal dependant. Max values are based on highest FS and highest MCLK.
5. I_{LC} measured with no external loading on the SDA pin.
6. Power Down Mode is defined as \overline{RST} pin = Low with all clock and data lines held static.
7. Valid with the recommended capacitor values on FILT+ and VQ as shown in [Figures 6 and 7](#).

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

The filter characteristics have been normalized to the sample rate (F_s) and can be referenced to the desired sample rate by multiplying the given characteristic by F_s .

(See [\(Note 12\)](#))

Parameter	Fast Roll-Off			Unit	
	Min	Typ	Max		
Combined Digital and On-chip Analog Filter Response - Single-Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.454	F_s
	to -3 dB corner	0	-	.499	F_s
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		0.547	-	-	F_s
StopBand Attenuation	(Note 10)	102	-	-	dB
Group Delay		-	10.4/ F_s	-	s
De-emphasis Error (Note 11) (Relative to 1 kHz)	$F_s = 32$ kHz	-	-	± 0.36	dB
	$F_s = 44.1$ kHz	-	-	± 0.21	dB
	$F_s = 48$ kHz	-	-	± 0.14	dB
Combined Digital and On-chip Analog Filter Response - Double-Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.430	F_s
	to -3 dB corner	0	-	.499	F_s
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.583	-	-	F_s
StopBand Attenuation	(Note 10)	80	-	-	dB
Group Delay		-	6.15/ F_s	-	s
Combined Digital and On-chip Analog Filter Response - Quad-Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.105	F_s
	to -3 dB corner	0	-	.490	F_s
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.635	-	-	F_s
StopBand Attenuation	(Note 10)	90	-	-	dB
Group Delay		-	7.1/ F_s	-	s

Notes:

8. Slow Roll-off interpolation filter is only available in Software Mode.
9. Response is clock dependent and will scale with F_s .
10. For Single-Speed Mode, the Measurement Bandwidth is from stopband to 3 F_s .
For Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 F_s .
For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 F_s .
11. De-emphasis is available only in Single-Speed Mode; Only 44.1 kHz De-emphasis is available in Hardware Mode.
12. Amplitude vs. Frequency plots of this data are available in the ["Filter Response Plots"](#) on page 43.

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(CONTINUED)

Parameter	Slow Roll-Off (Note 8)			Unit	
	Min	Typ	Max		
Single-Speed Mode - 48 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	0.417	Fs
	to -3 dB corner	0	-	0.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.583	-	-	Fs
StopBand Attenuation	(Note 10)	64	-	-	dB
Group Delay		-	7.8/Fs	-	s
De-emphasis Error (Note 11) (Relative to 1 kHz)	Fs = 32 kHz	-	-	±0.36	dB
	Fs = 44.1 kHz	-	-	±0.21	dB
	Fs = 48 kHz	-	-	±0.14	dB
Double-Speed Mode - 96 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.296	Fs
	to -3 dB corner	0	-	.499	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.792	-	-	Fs
StopBand Attenuation	(Note 10)	70	-	-	dB
Group Delay		-	5.4/Fs	-	s
Quad-Speed Mode - 192 kHz					
Passband (Note 9)	to -0.01 dB corner	0	-	.104	Fs
	to -3 dB corner	0	-	.481	Fs
Frequency Response	10 Hz to 20 kHz	-0.01	-	+0.01	dB
StopBand		.868	-	-	Fs
StopBand Attenuation	(Note 10)	75	-	-	dB
Group Delay		-	6.6/Fs	-	s

DSD COMBINED DIGITAL & ON-CHIP ANALOG FILTER RESPONSE

Parameter	Min	Typ	Max	Unit	
DSD Processor Mode					
Passband (Note 9)			50	kHz	
Frequency Response			+0.05	dB	
Roll-off	27	-	-	dB/Oct	
Direct DSD Mode					
Passband (Note 9)	to -0.1 dB corner	0	-	26.9	kHz
	to -3 dB corner	0	-	176.4	kHz
Frequency Response	10 Hz to 20 kHz	-0.1	-	0	dB

DIGITAL CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current (Note 13)	I_{in}	-	-	±10	μA
Input Capacitance		-	8	-	pF
High-Level Input Voltage	Serial I/O	V_{IH}	70%	-	V_{LS}
	Control I/O	V_{IH}	70%	-	V_{LC}
Low-Level Input Voltage	Serial I/O	V_{IL}	-	-	V_{LS}
	Control I/O	V_{IL}	-	-	V_{LC}
Low-Level Output Voltage ($I_{OL} = -1.2$ mA)	Control I/O = 3.3 V, 5 V	V_{OL}	-	-	20% V_{LC}
	Control I/O = 1.8 V, 2.5 V	V_{OL}	-	-	25% V_{LC}
MUTECH auto detect input high voltage	V_{IH}	70%	-	-	VA
MUTECH auto detect input low voltage	V_{IL}	-	-	30%	VA
Maximum MUTECH Drive Current	I_{max}	-	3	-	mA
MUTECH High-Level Output Voltage	V_{OH}	-	VA	-	V
MUTECH Low-Level Output Voltage	V_{OL}	-	0	-	V

13. Any pin except supplies. Transient currents of up to ±100 mA on the input pins will not cause SCR latch-up

SWITCHING CHARACTERISTICS - PCM

(Inputs: Logic 0 = GND, Logic 1 = VLS, $C_L = 30$ pF)

Parameters	Symbol	Min	Max	Units	
$\overline{\text{RST}}$ pin Low Pulse Width (Note 14)		1	-	ms	
MCLK Frequency		1.024	55.2	MHz	
MCLK Duty Cycle (Note 15)		45	55	%	
Input Sample Rate - LRCK (Manual selection)	Single-Speed Mode	F_s	4	54	kHz
	Double-Speed Mode	F_s	50	108	kHz
	Quad-Speed Mode	F_s	100	216	kHz
Input Sample Rate - LRCK (Auto detect)	Single-Speed Mode	F_s	4	54	kHz
	Double-Speed Mode	F_s	84	108	kHz
	Quad-Speed Mode	F_s	170	216	kHz
LRCK Duty Cycle		45	55	%	
SCLK Duty Cycle		45	55	%	
SCLK High Time	t_{sckh}	8	-	ns	
SCLK Low Time	t_{sckl}	8	-	ns	
LRCK Edge to SCLK Rising Edge	t_{lcks}	5	-	ns	
SCLK Rising Edge to LRCK Falling Edge	t_{lckd}	5	-	ns	
SDIN Setup Time Before SCLK Rising Edge	t_{ds}	3	-	ns	
SDIN Hold Time After SCLK Rising Edge	t_{dh}	5	-	ns	

Notes:

14. After powering up, $\overline{\text{RST}}$ should be held low until after the power supplies and clocks are settled.
15. See [Tables 1 - 3](#) for suggested MCLK frequencies.

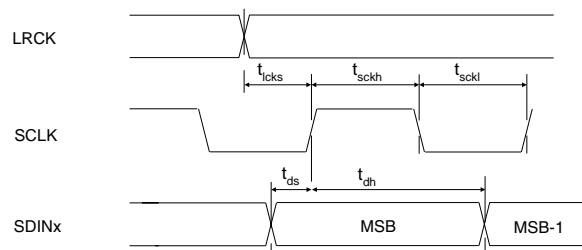


Figure 1. Serial Audio Interface Timing

SWITCHING CHARACTERISTICS - DSD

(Logic 0 = AGND = DGND; Logic 1 = VLS; $C_L = 30$ pF)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Duty Cycle		40	-	60	%
DSD_SCLK Pulse Width Low	t_{sckl}	160	-	-	ns
DSD_SCLK Pulse Width High	t_{sckh}	160	-	-	ns
DSD_SCLK Frequency	(64x Oversampled)	1.024	-	3.2	MHz
	(128x Oversampled)	2.048	-	6.4	MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdhrs}	20	-	-	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	20	-	-	ns
DSD clock to data transition (Phase Modulation Mode)	t_{dpm}	-20	-	20	ns

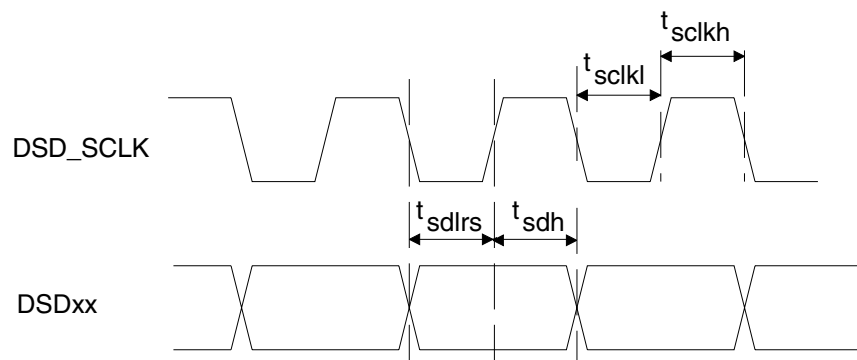


Figure 2. Direct Stream Digital - Serial Audio Input Timing

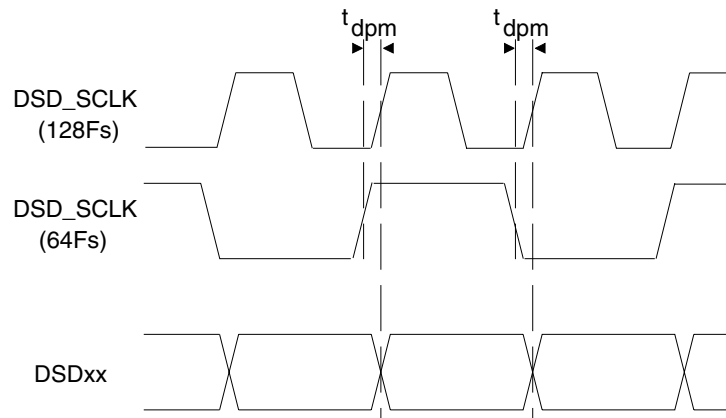


Figure 3. Direct Stream Digital - Serial Audio Input Timing for Phase Modulation Mode

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f _{scl}	-	100	kHz
RST Rising Edge to Start	t _{irs}	500	-	ns
Bus Free Time Between Transmissions	t _{buf}	4.7	-	μs
Start Condition Hold Time (prior to first clock pulse)	t _{hdst}	4.0	-	μs
Clock Low time	t _{low}	4.7	-	μs
Clock High Time	t _{high}	4.0	-	μs
Setup Time for Repeated Start Condition	t _{sust}	4.7	-	μs
SDA Hold Time from SCL Falling (Note 16)	t _{hdd}	0	-	μs
SDA Setup time to SCL Rising	t _{sud}	250	-	ns
Rise Time of SCL and SDA	t _{rc} , t _{rc}	-	1	μs
Fall Time SCL and SDA	t _{fc} , t _{fc}	-	300	ns
Setup Time for Stop Condition	t _{susp}	4.7	-	μs
Acknowledge Delay from SCL Falling	t _{ack}	300	1000	ns

Notes:

16. Data must be held for sufficient time to bridge the transition time, t_{rc}, of SCL.

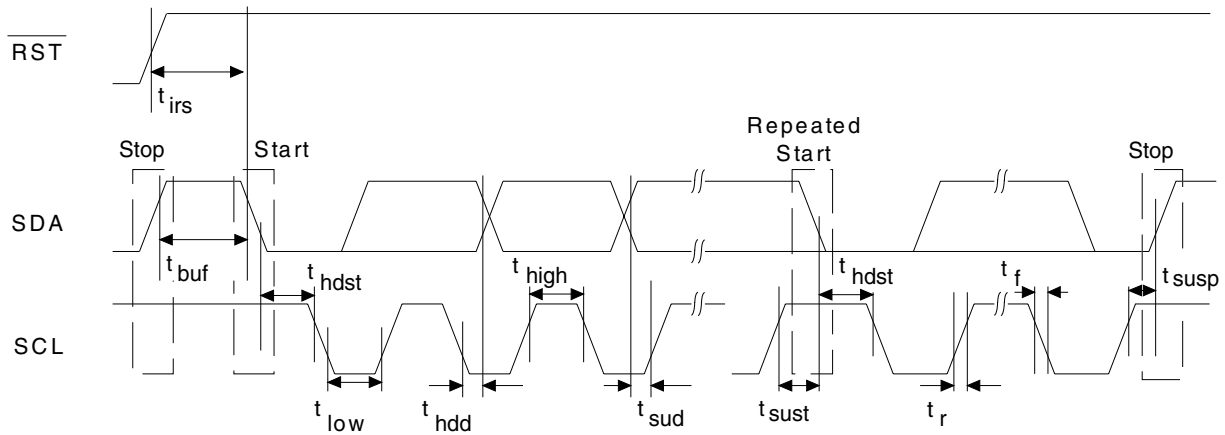


Figure 4. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

(Inputs: Logic 0 = GND, Logic 1 = VLC, $C_L = 30$ pF)

Parameter	Symbol	Min	Max	Unit
CCLK Clock Frequency	f_{sclk}	-	6	MHz
\overline{RST} Rising Edge to \overline{CS} Falling	t_{srs}	500	-	ns
CCLK Edge to \overline{CS} Falling (Note 17)	t_{spi}	500	-	ns
\overline{CS} High Time Between Transmissions	t_{csh}	1.0	-	μ s
\overline{CS} Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	66	-	ns
CCLK High Time	t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 18)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 19)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 19)	t_{f2}	-	100	ns

Notes:

17. t_{spi} only needed before first falling edge of \overline{CS} after \overline{RST} rising edge. $t_{spi} = 0$ at all other times.
18. Data must be held for sufficient time to bridge the transition time of CCLK.
19. For $F_{SCK} < 1$ MHz.

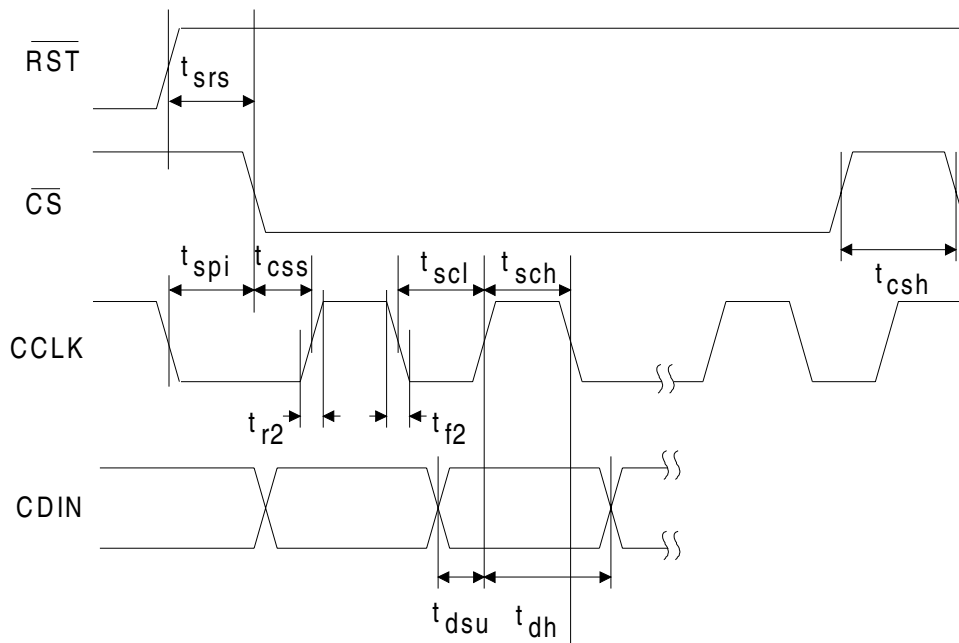


Figure 5. Control Port Timing - SPI Format

3. TYPICAL CONNECTION DIAGRAM

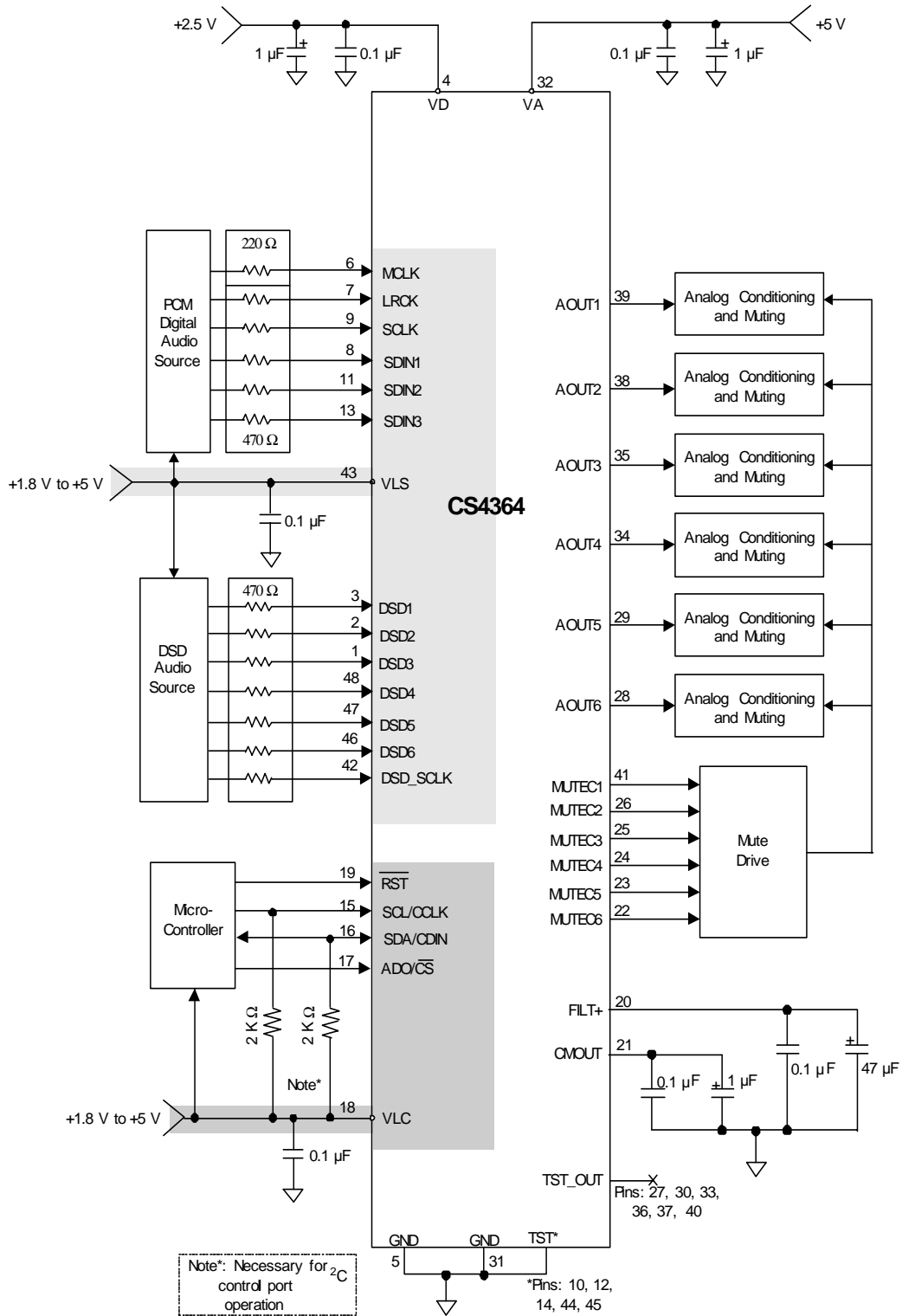


Figure 6. Typical Connection Diagram, Software Mode

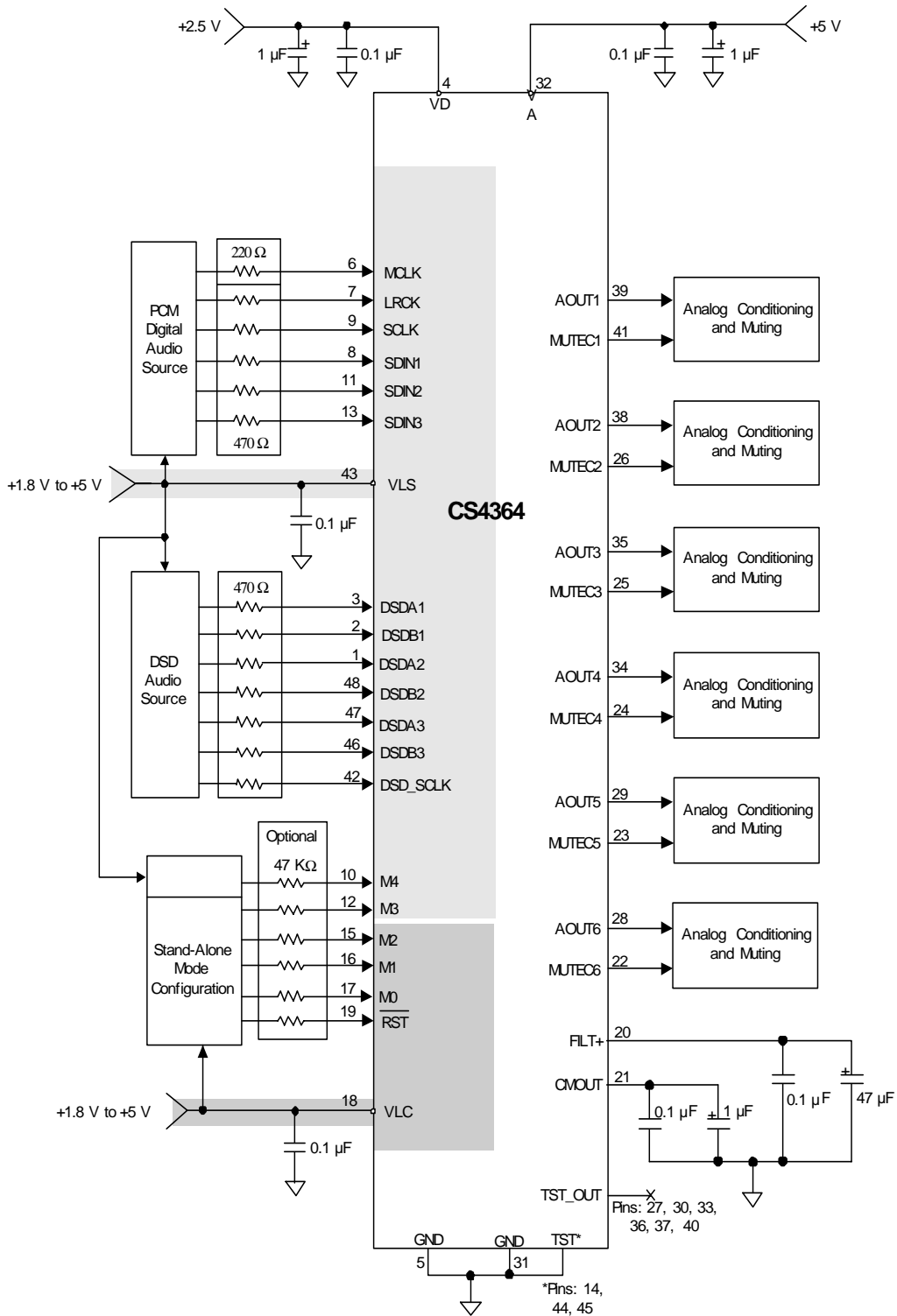


Figure 7. Typical Connection Diagram, Hardware Mode

4. APPLICATIONS

The CS4364 serially accepts two complement formatted PCM data at standard audio sample rates including 48, 44.1 and 32 kHz in SSM, 96, 88.2 and 64 kHz in DSM, and 192, 176.4 and 128 kHz in QSM. Audio data is input via the serial data input pins (SDINx). The Left/Right Clock (LRCK) determines which channel is currently being input on SDINx, and the Serial Clock (SCLK) clocks audio data into the input data buffer. For more information on serial audio interfaces see AN282 “The 2-Channel Serial Audio Interface: A Tutorial”.

The CS4364 can be configured in Hardware Mode by the M0, M1, M2, M3 and M4 pins and in Software Mode through I²C or SPI.

4.1 Master Clock

MCLK/LRCK must be an integer ratio as shown in [Tables 1 - 3](#). The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio and speed mode is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period and by detecting the absolute speed of MCLK. Internal dividers are then set to generate the proper internal clocks. [Tables 1 - 3](#) illustrate several standard audio sample rates and the required MCLK and LRCK frequencies. Please note there is no required phase relationship, but MCLK, LRCK and SCLK must be synchronous.

Sample Rate (kHz)	MCLK (MHz)					
	256x	384x	512x	768x	1024x	1152x
32	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640
44.1	11.2896	16.9344	22.5792	33.8688	45.1584	
48	12.2880	18.4320	24.5760	36.8640	49.1520	

Table 1. Single-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	128x	192x	256x	384x	512x
64	8.1920	12.2880	16.3840	24.5760	32.7680
88.2	11.2896	16.9344	22.5792	33.8688	45.1584
96	12.2880	18.4320	24.5760	36.8640	49.1520

Table 2. Double-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)				
	64x	96x	128x	192x	256x
176.4	11.2896	16.9344	22.5792	33.8688	45.1584
192	12.2880	18.4320	24.5760	36.8640	49.1520

Table 3. Quad-Speed Mode Standard Frequencies

= Denotes clock ratio and sample rate combinations which are NOT supported under auto speed-mode detection. Please see [“Switching Characteristics - PCM”](#) on page 14.

4.2 Mode Select

In Hardware Mode, operation is determined by the Mode Select pins. The states of these pins are continually scanned for any changes; however, the mode should only be changed while the device is in reset (RST pin low) to ensure proper switching from one mode to another. These pins require connection to supply or ground as outlined in [Figure 7](#). For M0, M1, and M2, supply is VLC. For M3 and M4, supply is VLS. [Tables 4 - 6](#) show the decode of these pins.

In Software Mode, the operational mode and data format are set in the FM and DIF registers. See [“PCM Control \(Address 03h\)”](#) on page 34.

M1 (DIF1)	M0 (DIF0)	DESCRIPTION	FORMAT	FIGURE
0	0	Left Justified, up to 24-bit data	0	8
0	1	I ² S, up to 24-bit data	1	9
1	0	Right Justified, 16-bit Data	2	10
1	1	Right Justified, 24-bit Data	3	11

Table 4. PCM Digital Interface Format, Hardware Mode Options

M4	M3	M2 (DEM)	M1	M0	DESCRIPTION
0	0	0	Table 4		Single-Speed without De-Emphasis (4 kHz to 50 kHz sample rates)
0	0	1			Single-Speed with 44.1 kHz De-Emphasis; see Figure 16
0	1	0			Double-Speed (50 kHz to 100 kHz sample rates)
0	1	1			Quad-Speed (100 kHz to 200 kHz sample rates)
1	0	0			Auto Speed-Mode Detect (32 kHz to 200 kHz sample rates)
1	0	1			Auto Speed-Mode Detect with 44.1 kHz De-Emphasis; see Figure 16
1	1		Table 6		DSD Processor Mode

Table 5. Mode Selection, Hardware Mode Options

M2	M1	M0	DESCRIPTION
0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate
0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate
1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate
1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate

Table 6. Direct Stream Digital (DSD), Hardware Mode Options

4.3 Digital Interface Formats

The serial port operates as a slave and supports the I²S, Left-Justified, Right-Justified, and One-Line Mode (OLM) digital interface formats with varying bit depths from 16 to 32 as shown in [Figures 8-15](#). Data is clocked into the DAC on the rising edge. OLM configurations are only supported in Software Mode.

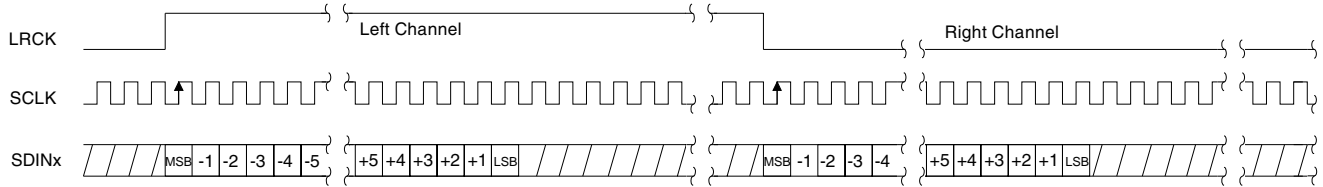


Figure 8. Format 0 - Left-Justified up to 24-bit Data

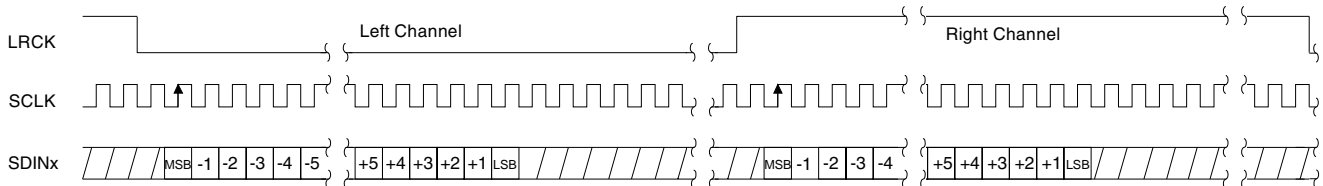


Figure 9. Format 1 - I²S up to 24-bit Data

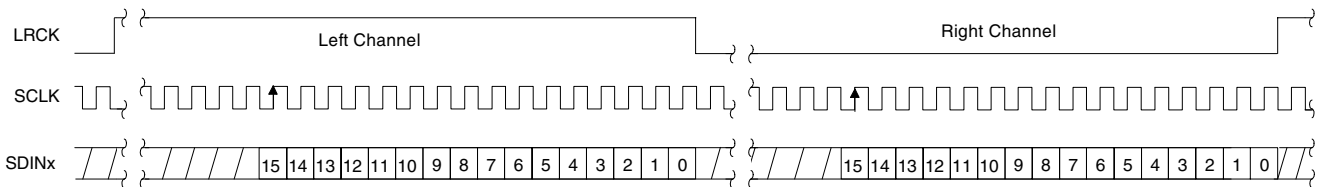


Figure 10. Format 2 - Right-Justified 16-bit Data

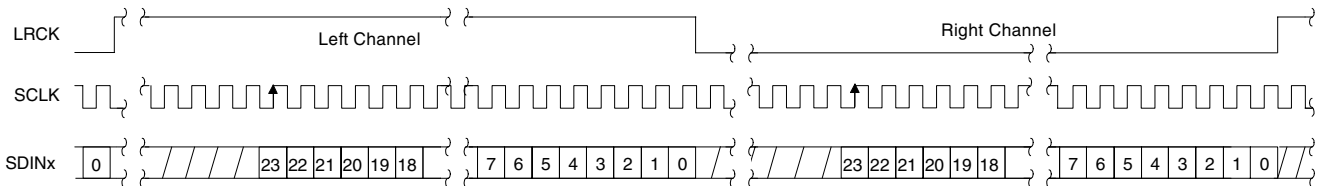


Figure 11. Format 3 - Right-Justified 24-bit Data

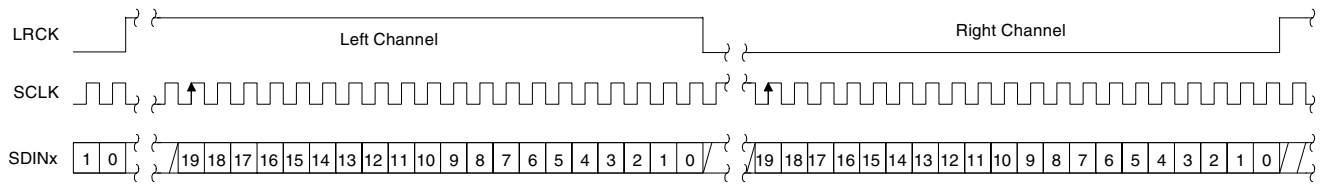


Figure 12. Format 4 - Right-Justified 20-bit Data

4.5 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS4364 incorporates selectable interpolation filters for each mode of operation. A “fast” and a “slow” roll-off filter is available in each of Single-, Double-, or Quad-Speed Modes. These filters have been designed to accommodate a variety of musical tastes and styles. The `FILT_SEL` bit is used to select which filter is used (see the “[Parameter Definitions](#)” on page 47 for more details).

When in Hardware Mode, only the “fast” roll-off filter is available.

Filter specifications can be found in [Section 2](#), and filter response plots can be found in [Figures 24 to 47](#).

4.6 De-Emphasis

The CS4364 includes on-chip digital de-emphasis filters. The de-emphasis feature is included to accommodate older audio recordings that utilize pre-emphasis equalization as a means of noise reduction. [Figure 16](#) shows the de-emphasis curve. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, F_s if the input sample rate does not match the coefficient which has been selected.

In Software Mode the required de-emphasis filter coefficients for 32 kHz, 44.1 kHz, or 48 kHz are selected via the de-emphasis control bits.

In Hardware Mode only the 44.1 kHz coefficient is available (enabled through the M2 pin). If the input sample rate is not 44.1 kHz and de-emphasis has been selected then the corner frequencies of the de-emphasis filter will be scaled by a factor of the actual F_s over 44,100.

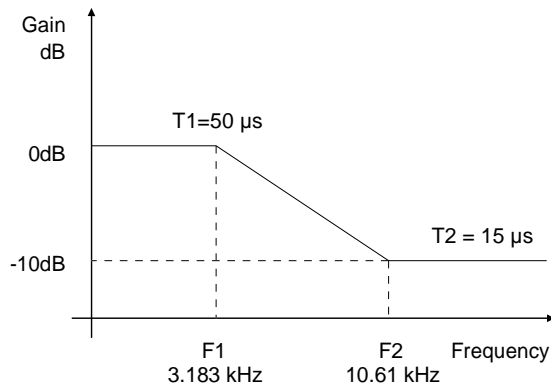


Figure 16. De-Emphasis Curve

4.7 ATAPI Specification

The CS4364 implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to [Table 9 on page 41](#) and [Figure 17](#) for additional information.

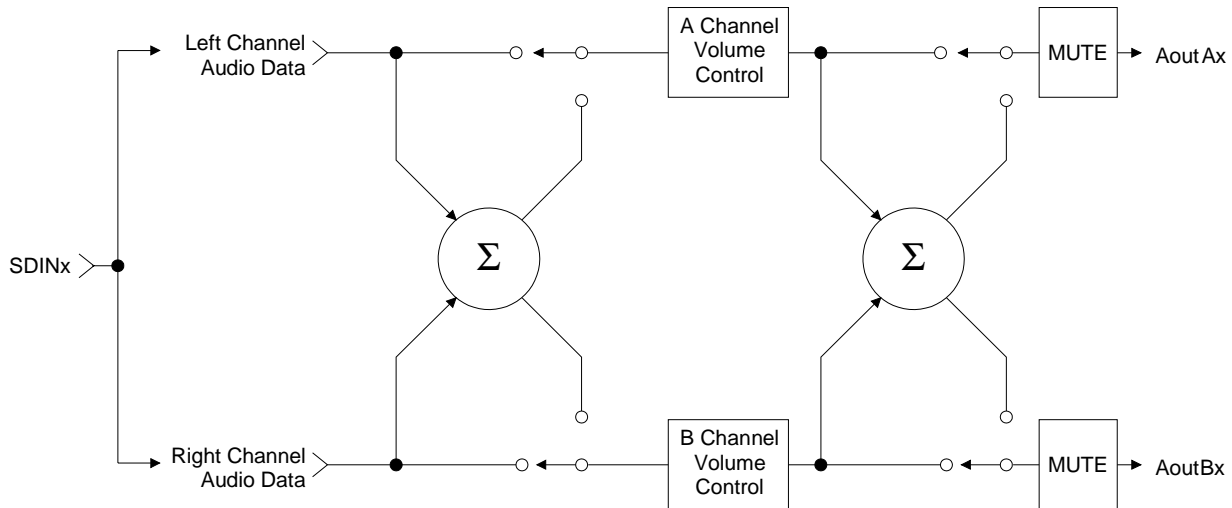


Figure 17. ATAPI Block Diagram (x = channel pair 1, 2, or 3)

4.8 Direct Stream Digital (DSD) Mode

In Software Mode the DSD/PCM bits (Reg. 02h) are used to configure the device for DSD mode. The DSD_DIF bits (Reg 04h) then control the expected DSD rate and MCLK ratio.

The DIR_DSD bit (Reg 04h) selects between two proprietary methods for DSD to analog conversion. The first method uses a decimation free DSD processing technique which allows for features such as matched PCM level output, DSD volume control, and 50kHz on chip filter. The second method sends the DSD data directly to the on-chip switched-capacitor filter for conversion (without the above mentioned features).

The DSD_PM_EN bit (Reg. 04h) selects Phase Modulation (data plus data inverted) as the style of data input. In this mode the DSD_PM_Mode bit selects whether a 128Fs or 64x clock is used for phase modulated 64x data (see [Figure 18](#)). Use of Phase Modulation Mode may not directly effect the performance of the CS4364, but may lower the sensitivity to board level routing of the DSD data signals.

The CS4364 can detect errors in the DSD data which does not comply with the SACD specification. The STATIC_DSD and INVALID_DSD bits (Reg. 04h) allow the CS4364 to alter the incoming invalid DSD data. Depending on the error, the data may either be attenuated or replaced with a muted DSD signal (the MUTE pins would be set according to the DAMUTE bit (Reg. 08h)).

More information for any of these register bits can be found in the [“Parameter Definitions” on page 47](#).

The DSD input structure and analog outputs are designed to handle a nominal 0 dB-SACD (50% modulation index) at full rated performance. Signals of +3 dB-SACD may be applied for brief periods of time however, performance at these levels is not guaranteed. If sustained +3 dB-SACD levels are required, the digital volume control should be set to -3.0 dB. This same volume control register affects PCM output levels. There is no need to change the volume control setting between PCM and DSD in order to have the 0 dB output levels match (both 0 dBFS and 0 dB-SACD will output at -3 dB in this case).

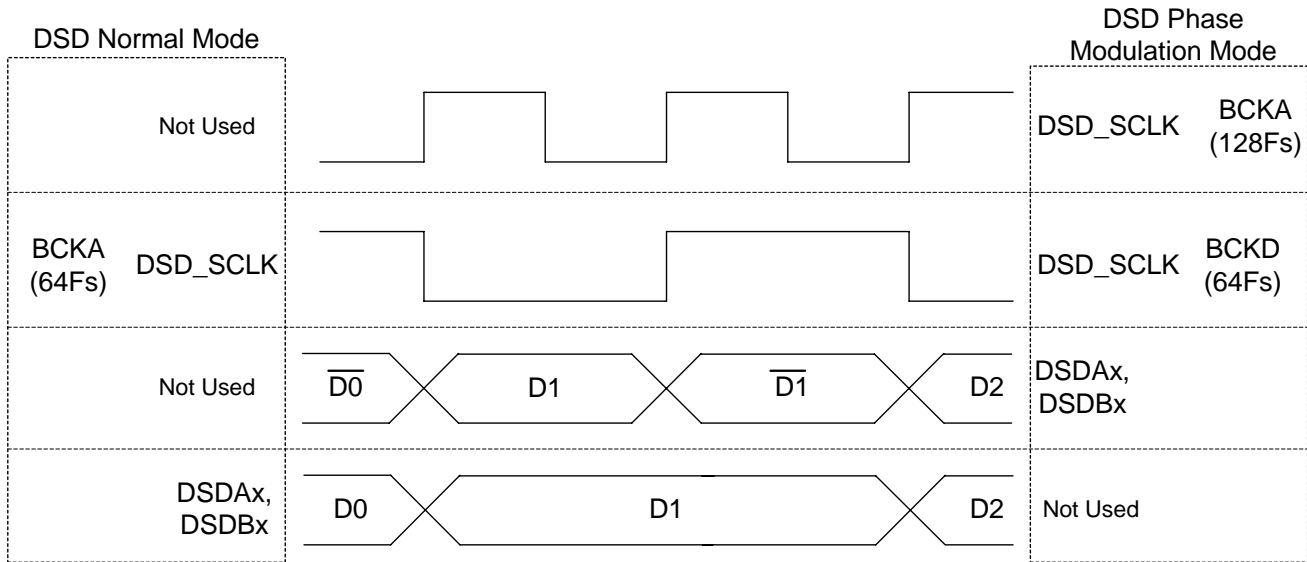


Figure 18. DSD Phase Modulation Mode Diagram

4.9 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS4364 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. The Typical Connection Diagram shows the recommended power arrangements, with VA, VD, VLC, and VLS connected to clean supplies. If the ground planes are split between digital ground and analog ground, the GND pins of the CS4364 should be connected to the analog ground plane.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the DAC.

4.9.1 Capacitor Placement

Decoupling capacitors should be placed as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC. If desired, all supply pins with similar voltage ratings may be connected to the same supply, but a decoupling capacitor should still be placed on each supply pin.

Note: All decoupling capacitors should be referenced to analog ground.

The CDB4364 evaluation board demonstrates the optimum layout and power supply arrangements.

4.10 Analog Output and Filtering

The CS4364 does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

[Figure 19](#) shows how the full-scale analog output level specification is derived.

[Figure 20](#) shows how the recommended output filtering with location for optional mute circuit.

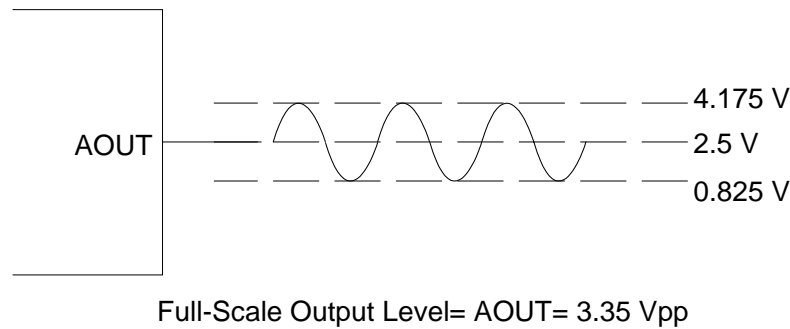


Figure 19. Full-Scale Output

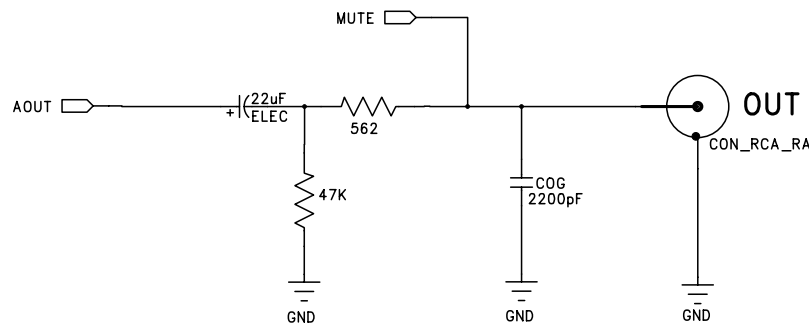


Figure 20. Recommended Output Filter

4.11 The MUTE outputs

The MUTE1 pins have an auto-polarity detect feature. The MUTE output pins are high impedance at the time of reset. The external mute circuitry needs to be self biased into an active state in order to be muted during reset. Upon release of reset, the CS4364 will detect the status of the MUTE pins (high or low) and will then select that state as the polarity to drive when the mutes become active. The external-bias voltage level that the MUTE pins see at the time of release of reset must meet the “MUTE auto detect input high/low voltage” specs as outlined in the Digital Characteristics section.

[Figure 21](#) shows a single example of both an active high and an active low mute drive circuit. In these designs, the pull-up and pull-down resistors have been especially chosen to meet the input high/low threshold when used with the MMUN2111 and MMUN2211 internal bias resistances of 10 kΩ.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit.

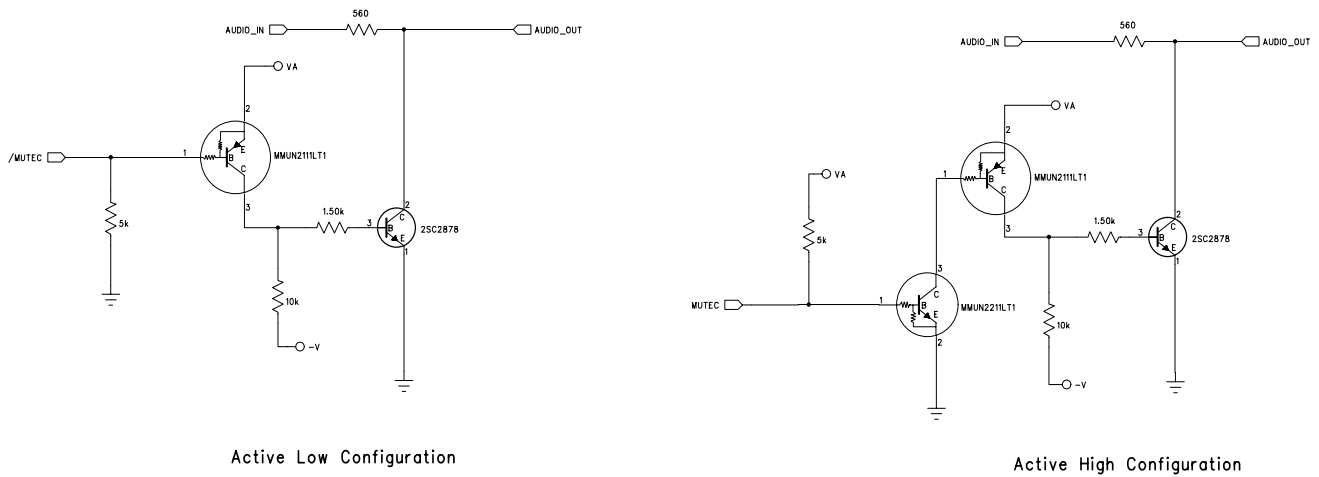


Figure 21. Recommended Mute Circuitry

4.12 Recommended Power-Up Sequence

4.12.1 Hardware Mode

1. Hold $\overline{\text{RST}}$ low until the power supplies and configuration pins are stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in [Section 4.1](#). In this state, the registers are reset to the default settings, FILT^+ will remain low, and VQ will be connected to $\text{VA}/2$. If $\overline{\text{RST}}$ can not be held low long enough the SDIN_x pins should remain static low until all other clocks are stable, and if possible the $\overline{\text{RST}}$ should be toggled low again once the system is stable.
2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with FILT^+ low and will initiate the Hardware power-up sequence after approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode).

4.12.2 Software Mode

1. Hold $\overline{\text{RST}}$ low until the power supply is stable, and the master and left/right clocks are locked to the appropriate frequencies, as discussed in [Section 4.1](#). In this state, the registers are reset to the default settings, FILT^+ will remain low, and VQ will be connected to $\text{VA}/2$.
2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with FILT^+ low for 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode).
3. In order to reduce the chances of clicks and pops, perform a write to the CP_EN bit prior to the completion of approximately 512 LRCK cycles in Single-Speed Mode (1024 LRCK cycles in Double-Speed Mode, and 2048 LRCK cycles in Quad-Speed Mode). The desired register settings can be loaded while keeping the PDN bit set to 1. Set the RMP_UP and RMP_DN bits to 1, then set the format and mode control bits to the desired settings.

If more than the stated number of LRCK cycles passes before CPEN bit is written then the chip will enter Hardware Mode and begin to operate with the M0-M4 as the mode settings. CPEN bit may be written at anytime, even after the Hardware sequence has begun. It is advised that if the CPEN bit can not be set in time then the SDIN_x pins should remain static low (this way no audio data can be

converted incorrectly by the Hardware Mode settings).

4. Set the PDN bit to 0. This will initiate the power-up sequence, which lasts approximately 50 μ s.

4.13 Recommended Procedure for Switching Operational Modes

For systems where the absolute minimum in clicks and pops is required, it is recommended that the MUTE bits are set prior to changing significant DAC functions (such as changing sample rates or clock sources). The mute bits may then be released after clocks have settled and the proper modes have been set.

It is required to have the device held in reset if the minimum high/low time specs of MCLK can not be met during clock source changes.

4.14 Control Port Interface

The control port is used to load all the internal register settings in order to operate in Software Mode (see the “[Parameter Definitions](#)” on page 47). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port operates in one of two modes: I²C or SPI.

4.14.1 MAP Auto Increment

The device has MAP (memory address pointer) auto increment capability enabled by the INCR bit (also the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I²C writes or reads and SPI writes. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

4.14.2 I²C Mode

In the I²C Mode, data is clocked into and out of the bi-directional serial control data line, SDA, by the serial control port clock, SCL (see [Figure 22](#) for the clock to data relationship). There is no CS pin. Pin AD0 enables the user to alter the chip address (001100[AD0][R/W]) and should be tied to VLC or GND as required, before powering up the device. If the device ever detects a high to low transition on the AD0/CS pin after power-up, SPI Mode will be selected.

4.14.2.1 I²C Write

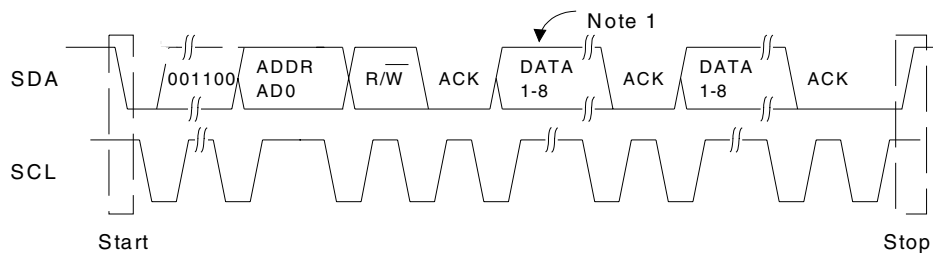
To write to the device, follow the procedure below while adhering to the control port Switching Specifications in [Section 2](#).

1. Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001100. The seventh bit must match the setting of the AD0 pin, and the eighth must be 0. The eighth bit of the address byte is the R/W bit.
2. Wait for an acknowledge (ACK) from the part, then write to the memory address pointer, MAP. This byte points to the register to be written.
3. Wait for an acknowledge (ACK) from the part, then write the desired data to the register pointed to by the MAP.
4. If the INCR bit (see [Section 4.14.1](#)) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.
5. If the INCR bit is set to 0 and further I²C writes to other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

4.14.2.2 I²C Read

To read from the device, follow the procedure below while adhering to the control port Switching Specifications.

1. Initiate a START condition to the I²C bus followed by the address byte. The upper 6 bits must be 001100. The seventh bit must match the setting of the AD0 pin, and the eighth must be 1. The eighth bit of the address byte is the R/W bit.
2. After transmitting an acknowledge (ACK), the device will then transmit the contents of the register pointed to by the MAP. The MAP register will contain the address of the last register written to the MAP, or the default address (see [Section 4.14.1](#)) if an I²C read is the first operation performed on the device.
3. Once the device has transmitted the contents of the register pointed to by the MAP, issue an ACK.
4. If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock and issue an ACK after each byte until all the desired registers are read, then initiate a STOP condition to the bus.
5. If the INCR bit is set to 0 and further I²C reads from other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from steps 1 and 2 from the I²C Write instructions followed by step 1 of the I²C Read section. If no further reads from other registers are desired, initiate a STOP condition to the bus.



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 22. Control Port Timing, I²C Mode

4.14.3 SPI Mode

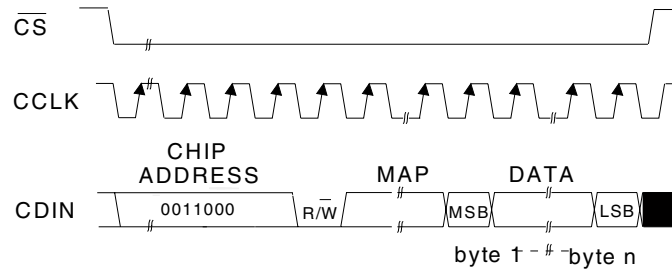
In SPI Mode, data is clocked into the serial control data line, CDIN, by the serial control port clock, CCLK (see [Figure 23](#) for the clock to data relationship). There is no AD0 pin. Pin \overline{CS} is the chip select signal and is used to control SPI writes to the control port. When the device detects a high to low transition on the AD0/ \overline{CS} pin after power-up, SPI Mode will be selected. All signals are inputs and data is clocked in on the rising edge of CCLK.

4.14.3.1 SPI Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in [Section 2](#).

1. Bring \overline{CS} low.
2. The address byte on the CDIN pin must then be 00110000.
3. Write to the memory address pointer, MAP. This byte points to the register to be written.
4. Write the desired data to the register pointed to by the MAP.
5. If the INCR bit (see [Section 4.14.1](#)) is set to 1, repeat the previous step until all the desired registers are written, then bring \overline{CS} high.

6. If the INCR bit is set to 0 and further SPI writes to other registers are desired, it is necessary to bring \overline{CS} high, and follow the procedure detailed from step 1. If no further writes to other registers are desired, bring \overline{CS} high.



MAP = Memory Address Pointer

Figure 23. Control Port Timing, SPI Mode

4.15 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	MAP4	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

4.15.1 INCR (Auto Map Increment Enable)

Default = '0'

0 - Disabled

1 - Enabled

4.15.2 MAP4-0 (Memory Address Pointer)

Default = '00000'

5. REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
01h	Chip Revision default	PART4 0	PART3 1	PART2 1	PART1 0	PART0 0	REV2 x	REV1 x	REV0 x
02h	Mode Control default	CPEN 0	FREEZE 0	DSD/PCM 0	Reserved 0	DAC3_DIS 0	DAC2_DIS 0	DAC1_DIS 0	PDN 1
03h	PCM Control default	DIF3 0	DIF2 0	DIF1 0	DIF0 0	Reserved 0	Reserved 0	FM1 1	FM0 1
04h	DSD Control default	DSD_DIF2 0	DSD_DIF1 0	DSD_DIF0 0	DIR_DSD 0	STATIC_D SD 1	INVALID_D SD 0	DSD_PM_ MD 0	DSD_PM_ EN 0
05h	Filter Control default	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	FILT_SEL 0
06h	Invert Control default	Reserved 0	Reserved 0	INV_B3 0	INV_A3 0	INV_B2 0	INV_A2 0	INV_B1 0	INV_A1 0
07h	Group Control default	MUTEC1 0	MUTEC0 0	Reserved 0	P1_A=B 0	P2_A=B 0	P3_A=B 0	Reserved 0	SINGLVOL 0
08h	Ramp and Mute default	SZC1 1	SZC0 0	RMP_UP 1	RMP_DN 1	PAMUTE 1	DAMUTE 1	MUTE_P1 0	MUTE_P0 0
09h	Mute Control default	Reserved 0	Reserved 0	MUTE_B3 0	MUTE_A3 0	MUTE_B2 0	MUTE_A2 0	MUTE_B1 0	MUTE_A1 0
0Ah	Mixing Control Pair 1 (AOUTx1) default	Reserved 0	P1_DEM1 0	P1_DEM0 0	P1ATAPI4 0	P1ATAPI3 1	P1ATAPI2 0	P1ATAPI1 0	P1ATAPI0 1
0Bh	Vol. Control A1 default	A1_VOL7 0	A1_VOL6 0	A1_VOL5 0	A1_VOL4 0	A1_VOL3 0	A1_VOL2 0	A1_VOL1 0	A1_VOL0 0
0Ch	Vol. Control B1 default	B1_VOL7 0	B1_VOL6 0	B1_VOL5 0	B1_VOL4 0	B1_VOL3 0	B1_VOL2 0	B1_VOL1 0	B1_VOL0 0
0Dh	Mixing Control Pair 2 (AOUTx1) default	Reserved 0	P2_DEM1 0	P2_DEM0 0	P2ATAPI4 0	P2ATAPI3 1	P2ATAPI2 0	P2ATAPI1 0	P2ATAPI0 1
0Eh	Vol. Control A2 default	A2_VOL7 0	A2_VOL6 0	A2_VOL5 0	A2_VOL4 0	A2_VOL3 0	A2_VOL2 0	A2_VOL1 0	A2_VOL0 0
0Fh	Vol. Control B2 default	B2_VOL7 0	B2_VOL6 0	B2_VOL5 0	B2_VOL4 0	B2_VOL3 0	B2_VOL2 0	B2_VOL1 0	B2_VOL0 0
10h	Mixing Control Pair 3 (AOUTx1) default	Reserved 0	P3_DEM1 0	P3_DEM0 0	P3ATAPI4 0	P3ATAPI3 1	P3ATAPI2 0	P3ATAPI1 0	P3ATAPI0 1
11h	Vol. Control A3 default	A3_VOL7 0	A3_VOL6 0	A3_VOL5 0	A3_VOL4 0	A3_VOL3 0	A3_VOL2 0	A3_VOL1 0	A3_VOL0 0
12h	Vol. Control B3 default	B3_VOL7 0	B3_VOL6 0	B3_VOL5 0	B3_VOL4 0	B3_VOL3 0	B3_VOL2 0	B3_VOL1 0	B3_VOL0 0
16h	PCM clock mode default	Reserved 0	Reserved 0	MCLKDIV 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0

6. REGISTER DESCRIPTION

Note: All registers are read/write in I²C Mode and write only in SPI, unless otherwise noted.

6.1 Chip Revision (Address 01h)

7	6	5	4	3	2	1	0
PART4	PART3	PART2	PART1	PART0	REV2	REV1	REV0
0	1	1	0	0	-	-	-

6.1.1 Part Number ID (PART) [Read Only]

01100 - CS4364

6.1.2 Revision ID (REV) [Read Only]

000 - Revision A0

001 - Revision B0

Function:

This read-only register can be used to identify the model and revision number of the device.

6.2 Mode Control 1 (Address 02h)

7	6	5	4	3	2	1	0
CPEN	FREEZE	DSD/PCM	Reserved	DAC3_DIS	DAC2_DIS	DAC1_DIS	PDN
0	0	0	0	0	0	0	1

6.2.1 Control Port Enable (CPEN)

Default = 0

0 - Disabled

1 - Enabled

Function:

This bit defaults to 0, allowing the device to power-up in Stand-Alone Mode. The Control Port Mode can be accessed by setting this bit to 1. This will allow the operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode. To accomplish a clean power-up, the user should write this bit within 10 ms following the release of Reset.

6.2.2 Freeze Controls (FREEZE)

Default = 0

0 - Disabled

1 - Enabled

Function:

This function allows modifications to be made to the registers without the changes taking effect until the FREEZE is disabled. To make multiple changes in the Control port registers take effect simultaneously, enable the FREEZE Bit, make all register changes, then Disable the FREEZE bit.

6.2.3 PCM/DSD Selection (*DSD/PCM*)

Default = 0
 0 - PCM
 1 - DSD

Function:

This function selects DSD or PCM Mode. The appropriate data and clocks should be present before changing modes, or else MUTE should be selected.

6.2.4 DAC Pair Disable (*DACx_DIS*)

Default = 0
 0 - DAC Pair x Enabled
 1 - DAC Pair x Disabled

Function:

When the bit is set, the respective DAC channel pair (AOUTAx and AOUTBx) will remain in a reset state. It is advised that changes to these bits be made while the power-down (PDN) bit is enabled to eliminate the possibility of audible artifacts.

6.2.5 Power Down (*PDN*)

Default = 1
 0 - Disabled
 1 - Enabled

Function:

The entire device will enter a low-power state when this function is enabled, and the contents of the control registers are retained in this mode. The power-down bit defaults to 'enabled' on power-up and must be disabled before normal operation in Control Port Mode can occur.

6.3 PCM Control (Address 03h)

7	6	5	4	3	2	1	0
DIF3	DIF2	DIF1	DIF0	Reserved	Reserved	FM1	FM0
0	0	0	0	0	0	1	1

6.3.1 Digital Interface Format (*DIF*)

Default = 0000 - Format 0 (Left Justified, up to 24-bit data)

Function:

These bits select the interface format for the serial audio input. The *DSD/PCM* bit determines whether PCM or DSD Mode is selected.

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in [Figures 8-15](#).

Note: While in PCM Mode, the DIF bits should only be changed when the power-down (PDN) bit is set to ensure proper switching from one mode to another.

DIF3	DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	0	Left Justified, up to 24-bit data	0	8
0	0	0	1	I ² S, up to 24-bit data	1	9
0	0	1	0	Right Justified, 16-bit data	2	10
0	0	1	1	Right Justified, 24-bit data	3	11
0	1	0	0	Right Justified, 20-bit data	4	12
0	1	0	1	Right Justified, 18-bit data	5	13
1	0	0	0	One-line Mode 1, 24-bit Data	8	14
1	0	0	1	One-line Mode 2, 20-bit Data	9	15
X	X	X	X	All other combinations are Reserved		

Table 7. Digital Interface Formats - PCM Mode

6.3.2 Functional Mode (FM)

Default = 11

00 - Single-Speed Mode (4 to 50 kHz sample rates)

01 - Double-Speed Mode (50 to 100 kHz sample rates)

10 - Quad-Speed Mode (100 to 200 kHz sample rates)

11 - Auto Speed Mode detect (32 kHz to 200 kHz sample rates)

Function:

Selects the required range of input sample rates or Auto Speed Mode.

6.4 DSD Control (Address 04h)

7	6	5	4	3	2	1	0
DSD_DIF2	DSD_DIF1	DSD_DIF0	DIR_DSD	STATIC_DSD	INVALID_DSD	DSD_PM_MD	DSD_PM_EN
0	0	0	0	1	1	0	0

6.4.1 DSD Mode Digital Interface Format (DSD_DIF)

Default = 000 - Format 0 (64x oversampled DSD data with a 4x MCLK to DSD data rate)

Function:

The relationship between the oversampling ratio of the DSD audio data and the required Master clock to DSD data rate is defined by the Digital Interface Format pins.

The DSD/PCM bit determines whether PCM or DSD Mode is selected.

DIF2	DIF1	DIF0	DESCRIPTION
0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate
0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate.
1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate.
1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate.
1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate.

Table 8. Digital Interface Formats - DSD Mode

6.4.2 Direct DSD Conversion (DIR_DSD)

Function:

When set to 0 (default), DSD input data is sent to the DSD processor for filtering and volume control functions.

When set to 1, DSD input data is sent directly to the switched capacitor DACs for a pure DSD conversion. In this mode, the full-scale DSD and PCM levels will not be matched (see [Section 2](#)), the dynamic range performance may be reduced, the volume control is inactive, and the 50 kHz low-pass filter is not available (see [Section 2](#) for filter specifications).

6.4.3 Static DSD Detect (STATIC_DSD)

Function:

When set to 1 (default), the DSD processor checks for 28 consecutive zeroes or ones and, if detected, sends a mute signal to the DACs. The MUTE pins will eventually go active according to the DAMUTE register.

When set to 0, this function is disabled.

6.4.4 Invalid DSD Detect (INVALID_DSD)

Function:

When set to 1, the DSD processor checks for greater than 24 out of 28 bits of the same value and, if detected, will attenuate the data sent to the DACs. The MUTE pins go active according to the DAMUTE register.

When set to 0 (default), this function is disabled.

6.4.5 DSD Phase Modulation Mode Select (DSD_PM_MODE)

Function:

When set to 0 (default), the 128Fs (BCKA) clock should be input to DSD_SCLK for Phase Modulation Mode. (See [Figure 16 on page 24](#).)

When set to 1, the 64Fs (BCKD) clock should be input to DSD_SCLK for Phase Modulation Mode.

6.4.6 DSD Phase Modulation Mode Enable (DSD_PM_EN)

Function:

When set to 1, DSD Phase Modulation Input Mode is enabled and the DSD_PM_MODE bit should be set accordingly.

When set to 0 (default), this function is disabled (DSD normal mode).

6.5 Filter Control (Address 05h)

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	FILT_SEL 0

6.5.1 Interpolation Filter Select (FILT_SEL)

Function:

When set to 0 (default), the Interpolation Filter has a fast roll off.

When set to 1, the Interpolation Filter has a slow roll off.

The specifications for each filter can be found in the Analog characteristics table, and response plots can be found in [Figures 22 to 45](#).

6.6 Invert Control (Address 06h)

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	INV_B3 0	INV_A3 0	INV_B2 0	INV_A2 0	INV_B1 0	INV_A1 0

6.6.1 Invert Signal Polarity (INV_xx)

Function:

When set to 1, this bit inverts the signal polarity of channel xx.

When set to 0 (default), this function is disabled.

6.7 Group Control (Address 07h)

7	6	5	4	3	2	1	0
MUTEC1 0	MUTEC0 0	Reserved 0	P1_A=B 0	P2_A=B 0	P3_A=B 0	Reserved 0	SNGLVOL 0

6.7.1 Mute Pin Control (MUTEC1, MUTEC0)

Default = 00

00 - Six mute control signals

01, 10 - One mute control signal

11 - Three mute control signals

Function:

Selects how the internal mute control signals are routed to the MUTEC1 through MUTEC6 pins. When set to '00', there is one mute control signal for each channel: AOUT1A on MUTEC1, AOUT1B on MUTEC2, etc. When set to '01' or '10', there is a single mute control signal on the MUTEC1 pin. When set to '11', there are three mute control signals, one for each stereo pair: AOUT1A and AOUT1B on MUTEC1, AOUT2A and AOUT2B on MUTEC2, and AOUT3A and AOUT3B on MUTEC3.

6.7.2 Channel A Volume = Channel B Volume (Px_A=B)

Default = 0

0 - Disabled

1 - Enabled

Function:

The AOUTAx and AOUTBx volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTAx and AOUTBx are determined by the A Channel Attenuation and Volume Control Bytes (per A-B pair), and the B Channel Bytes are ignored when this function is enabled.

6.7.3 Single Volume Control (SNGLVOL)

Default = 0

0 - Disabled

1 - Enabled

Function:

The individual channel volume levels are independently controlled by their respective Volume Control Bytes when this function is disabled. The volume on all channels is determined by the A1 Channel Volume Control Byte, and the other Volume Control Bytes are ignored when this function is enabled.

6.8 Ramp and Mute (Address 08h)

7	6	5	4	3	2	1	0
SZC1	SZC0	RMP_UP	RMP_DN	PAMUTE	DAMUTE	MUTE_P1	MUTE_P0
1	0	1	1	1	1	0	0

6.8.1 Soft Ramp and Zero Cross Control (SZC)

Default = 10

00 - Immediate Change

01 - Zero Cross

10 - Soft Ramp

11 - Soft Ramp on Zero Crossings

Function:

Immediate Change

When Immediate Change is selected all level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp on Zero Crossing

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz

sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

6.8.2 **Soft Volume Ramp-Up After Error (RMP_UP)**

Function:

An un-mute will be performed after executing an LRCK/MCLK ratio change or error, and after changing the Functional Mode.

When set to 1 (default), this un-mute is effected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

When set to 0, an immediate un-mute is performed in these instances.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_DN bit.

6.8.3 **Soft Ramp-Down Before Filter Mode Change (RMP_DN)**

Function:

If either the FILT_SEL or DEM bits are changed the DAC will stop conversion for a period of time to change its filter values. This bit selects how the data is effected prior to and after the change of the filter values.

When set to 1 (default), a mute will be performed prior to executing a filter mode change and an un-mute will be performed after executing the filter mode change. This mute and un-mute are effected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

When set to 0, an immediate mute is performed prior to executing a filter mode change.

Note: For best results, it is recommended that this feature be used in conjunction with the RMP_UP bit.

6.8.4 **PCM Auto-Mute (PAMUTE)**

Function:

When set to 1 (default) the Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period.

When set to 0 this function is disabled.

6.8.5 **DSD Auto-Mute (DAMUTE)**

Function:

When set to 1 (default) the Digital-to-Analog converter output will mute following the reception of 256 repeated 8-bit DSD mute patterns (as defined in the SACD specification).

A single bit not fitting the repeated mute pattern (mentioned above) will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained and the Mute Control pin will go active during the mute period.

6.8.6 MUTE Polarity and DETECT (MUTEP1:0)

Default = 00

00 - Auto polarity detect, selected from MUTEC1 pin

01 - Reserved

10 - Active low mute polarity

11 - Active high mute polarity

Function:

Auto mute polarity detect (00)

See [Section 4.11 on page 27](#) for the description.

Active low mute polarity (10)

When $\overline{\text{RST}}$ is low the outputs are high impedance and will need to be biased active. Once reset has been released and after this bit is set, the MUTEC output pins will be active low polarity.

Active high mute polarity (11)

At reset time the outputs are high impedance and will need to be biased active. Once reset has been released and after this bit is set, the MUTEC output pins will be active high polarity.

6.9 Mute Control (Address 09h)

7	6	5	4	3	2	1	0
Reserved	Reserved	MUTE_B3	MUTE_A3	MUTE_B2	MUTE_A2	MUTE_B1	MUTE_A1
0	0	0	0	0	0	0	0

6.9.1 Mute (MUTE_xx)

Default = 0

0 - Disabled

1 - Enabled

Function:

The Digital-to-Analog converter output will mute when enabled. The quiescent voltage on the output will be retained. The muting function is affected, similarly to attenuation changes, by the Soft and Zero Cross bits. The MUTE pins will go active during the mute period according to the MUTEC bits.

6.10 Mixing Control (Address 0Ah, 0Dh, 10h, 13h)

7	6	5	4	3	2	1	0
Reserved	Px_DEM1	Px_DEM0	PxATAPI4	PxATAPI3	PxATAPI2	PxATAPI1	PxATAPI0
0	0	0	0	1	0	0	1

6.10.1 De-Emphasis Control (PX_DEM1:0)

Default = 00

00 - Disabled

01 - 44.1 kHz

10 - 48 kHz

11 - 32 kHz

Function:

Selects the appropriate digital filter to maintain the standard 15 μ s/50 μ s digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (Figure 16 on page 24)

De-emphasis is only available in Single-Speed Mode.

6.10.2 ATAPI Channel Mixing and Muting (ATAPI)

Default = 01001 - AOUTAx=aL, AOUTBx=bR (Stereo)

Function:

The CS4364 implements the channel mixing functions of the ATAPI CD-ROM specification. The ATAPI functions are applied per A-B pair. Refer to Table 9 and Figure 17 for additional information.

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTAx	AOUTBx
0	0	0	0	0	MUTE	MUTE
0	0	0	0	1	MUTE	bR
0	0	0	1	0	MUTE	bL
0	0	0	1	1	MUTE	b[(L+R)/2]
0	0	1	0	0	aR	MUTE
0	0	1	0	1	aR	bR
0	0	1	1	0	aR	bL
0	0	1	1	1	aR	b[(L+R)/2]
0	1	0	0	0	aL	MUTE
0	1	0	0	1	aL	bR
0	1	0	1	0	aL	bL
0	1	0	1	1	aL	b[(L+R)/2]
0	1	1	0	0	a[(L+R)/2]	MUTE
0	1	1	0	1	a[(L+R)/2]	bR
0	1	1	1	0	a[(L+R)/2]	bL
0	1	1	1	1	a[(L+R)/2]	b[(L+R)/2]
1	0	0	0	0	MUTE	MUTE
1	0	0	0	1	MUTE	bR
1	0	0	1	0	MUTE	bL
1	0	0	1	1	MUTE	[(bL+aR)/2]
1	0	1	0	0	aR	MUTE
1	0	1	0	1	aR	bR
1	0	1	1	0	aR	bL
1	0	1	1	1	aR	[(aL+bR)/2]
1	1	0	0	0	aL	MUTE
1	1	0	0	1	aL	bR
1	1	0	1	0	aL	bL
1	1	0	1	1	aL	[(aL+bR)/2]
1	1	1	0	0	[(aL+bR)/2]	MUTE
1	1	1	0	1	[(aL+bR)/2]	bR
1	1	1	1	0	[(bL+aR)/2]	bL
1	1	1	1	1	[(aL+bR)/2]	[(aL+bR)/2]

Table 9. ATAPI Decode

6.11 Volume Control (Address 0Bh, 0Ch, 0Eh, 0Fh, 11h, 12h)

7	6	5	4	3	2	1	0
xx_VOL7	xx_VOL6	xx_VOL5	xx_VOL4	xx_VOL3	xx_VOL2	xx_VOL1	xx_VOL0
0	0	0	0	0	0	0	0

These six registers provide individual volume and mute control for each of the six channels.

The values for “xx” in the bit fields above are as follows:

Register address 0Bh - xx = A1

Register address 0Ch - xx = B1

Register address 0Eh - xx = A2

Register address 0Fh - xx = B2

Register address 11h - xx = A3

Register address 12h - xx = B3

6.11.1 Digital Volume Control (xx_VOL7:0)

Default = 00h (0 dB)

Function:

The Digital Volume Control registers allow independent control of the signal levels in 1/2 dB increments from 0 to -127.5 dB. Volume settings are decoded as shown in Table 10. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Power and Muting Control register. Note that the values in the volume setting column in Table 10 are approximate. The actual attenuation is determined by taking the decimal value of the volume register and multiplying by 6.02/12.

Binary Code	Decimal Value	Volume Setting
00000000	0	0 dB
00000001	1	-0.5 dB
00000110	6	-3.0 dB
11111111	255	-127.5 dB

Table 10. Example Digital Volume Settings

6.12 PCM Clock Mode (Address 16h)

7	6	5	4	3	2	1	0
Reserved	Reserved	MCLKDIV	Reserved	Reserved	Reserved	Reserved	Reserved
0	0	0	0	0	0	0	0

6.12.1 Master Clock Divide by 2 Enable (MCLKDIV)

Function:

When set to 1, the MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2 prior to all other internal circuitry.

When set to 0 (default), MCLK is unchanged.

7. FILTER RESPONSE PLOTS

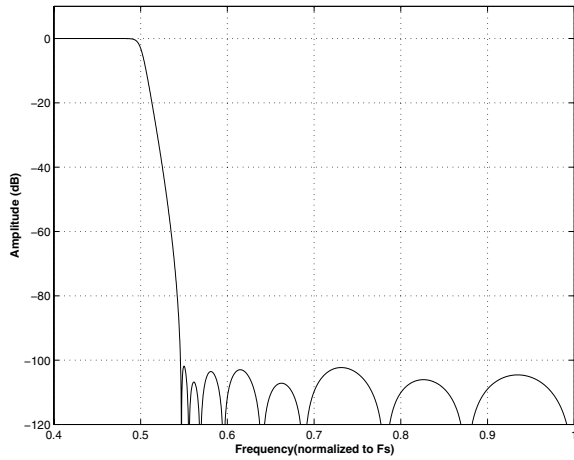


Figure 24. Single-Speed (fast) Stopband Rejection

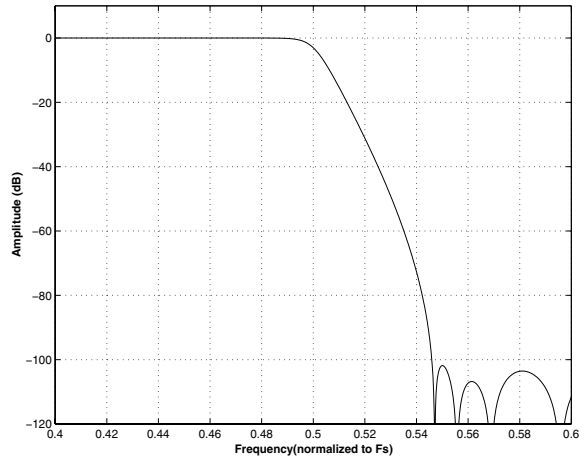


Figure 25. Single-Speed (fast) Transition Band

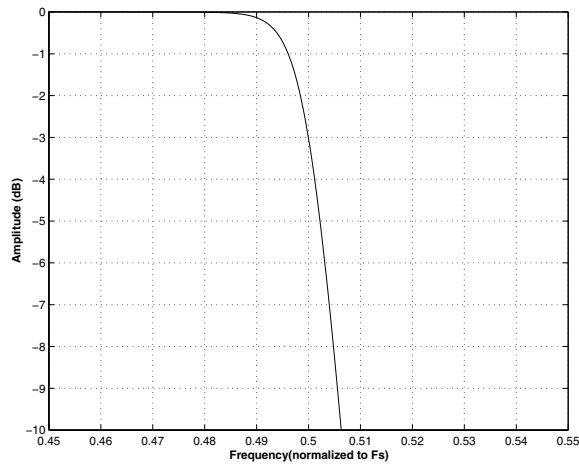


Figure 26. Single-Speed (fast) Transition Band (detail)

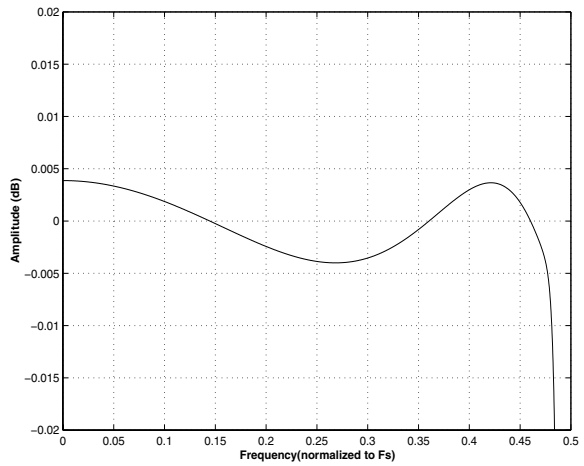


Figure 27. Single-Speed (fast) Passband Ripple

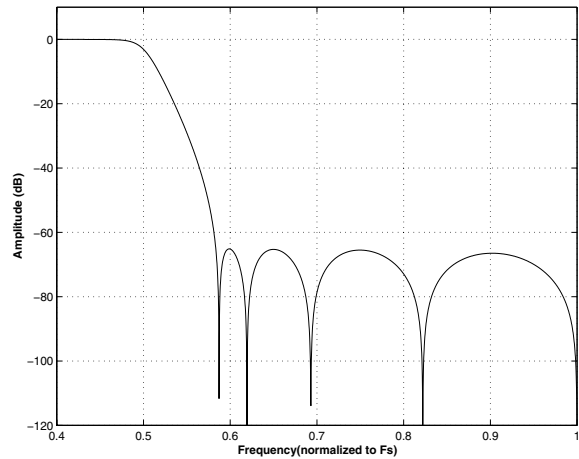


Figure 28. Single-Speed (slow) Stopband Rejection

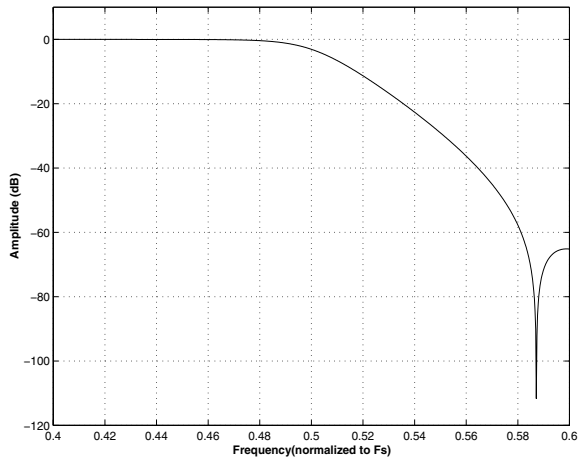
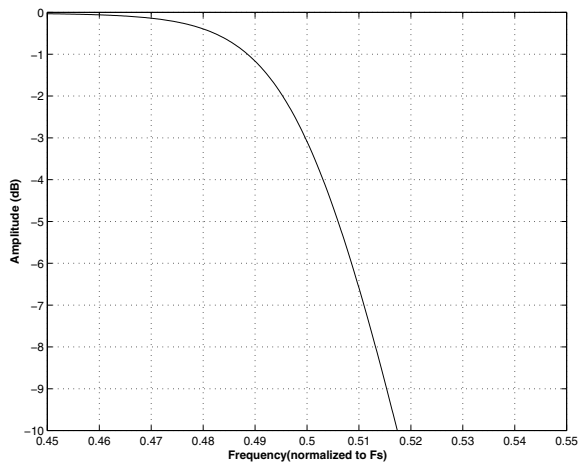
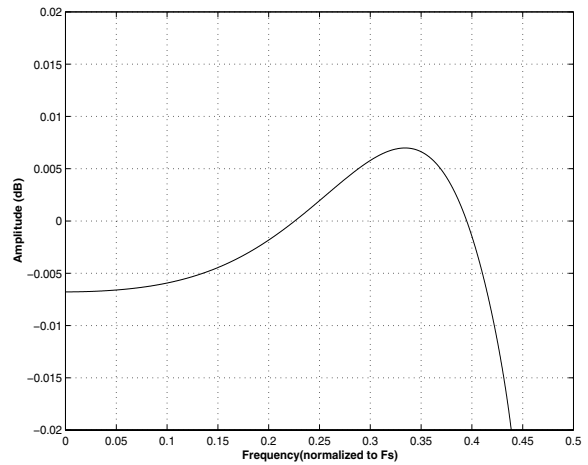
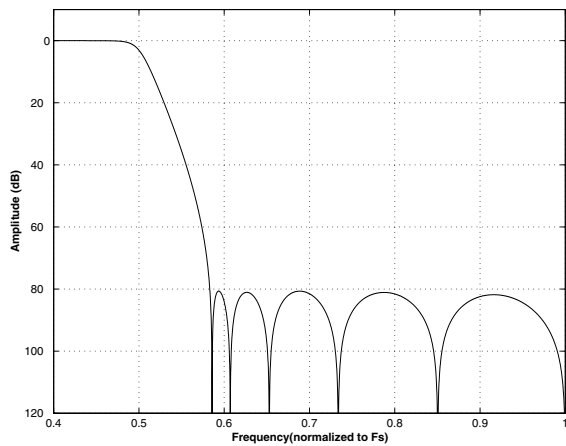
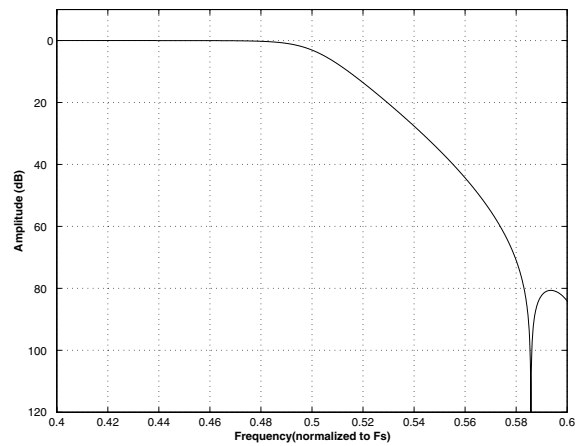
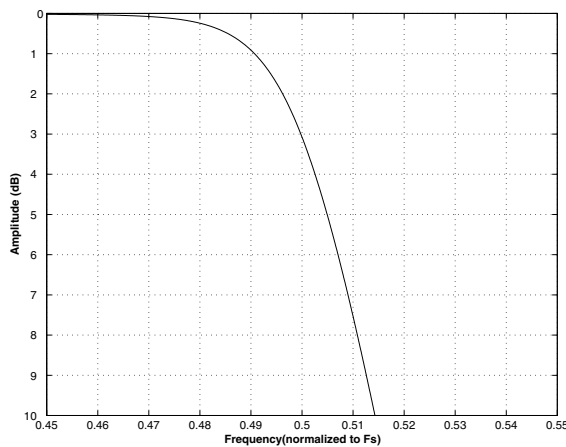
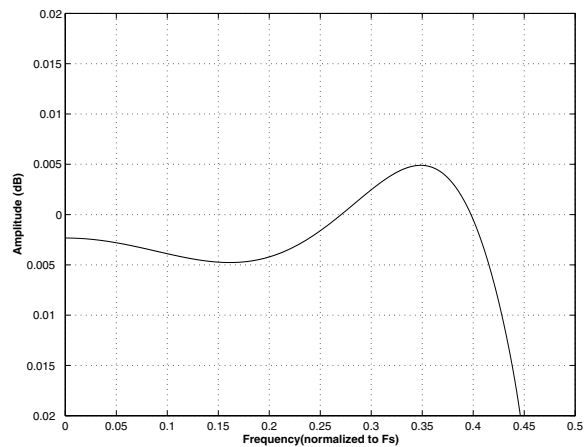
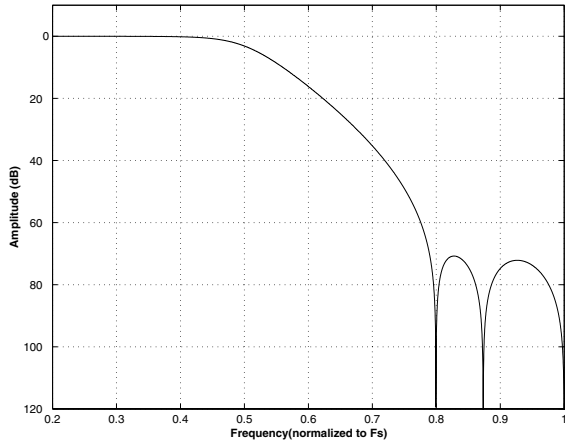
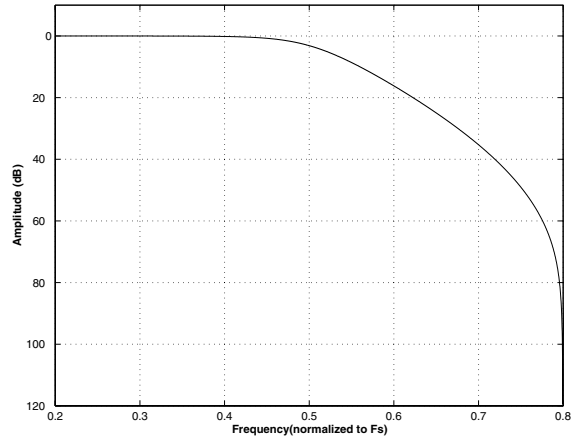
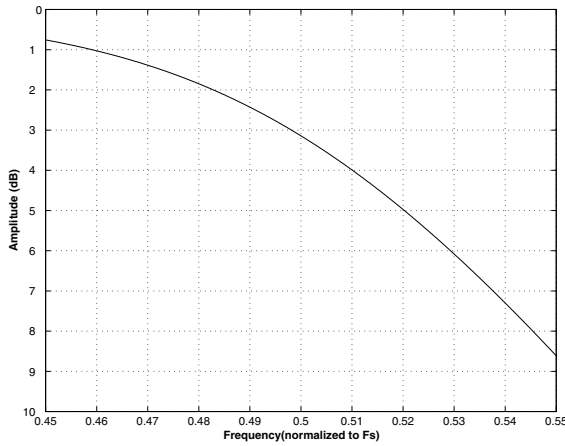
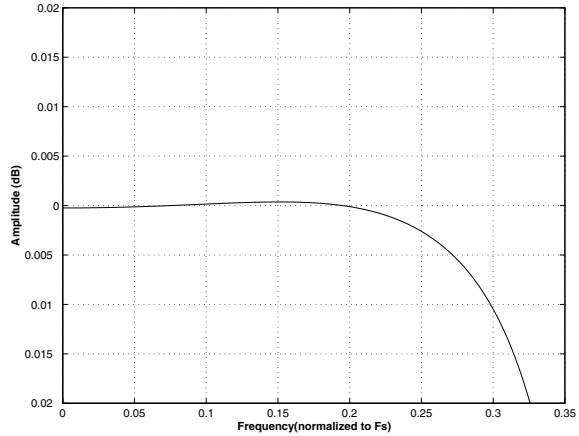
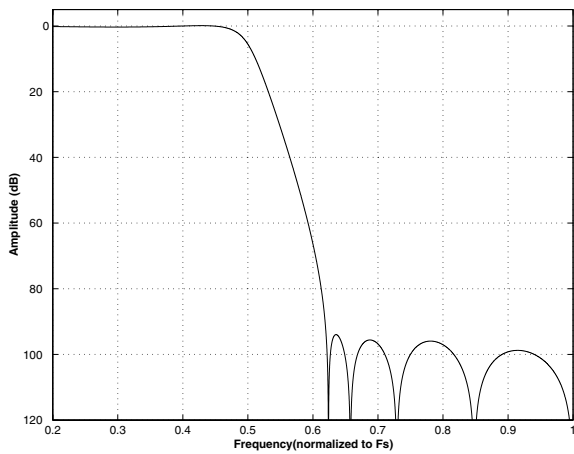
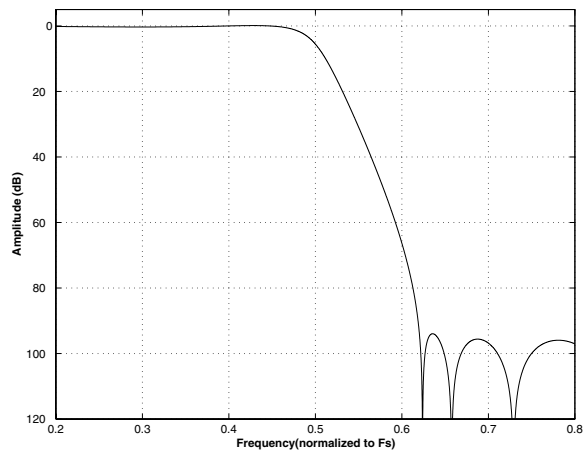
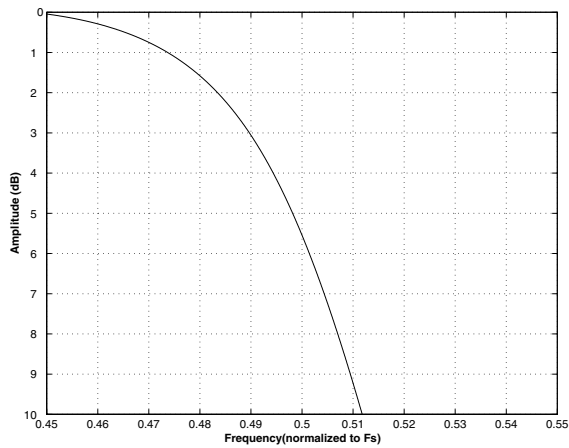
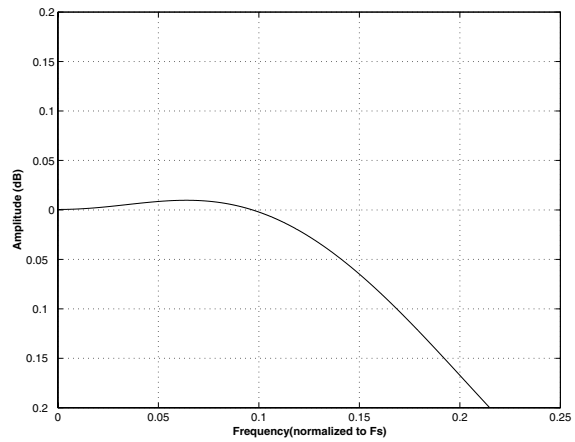
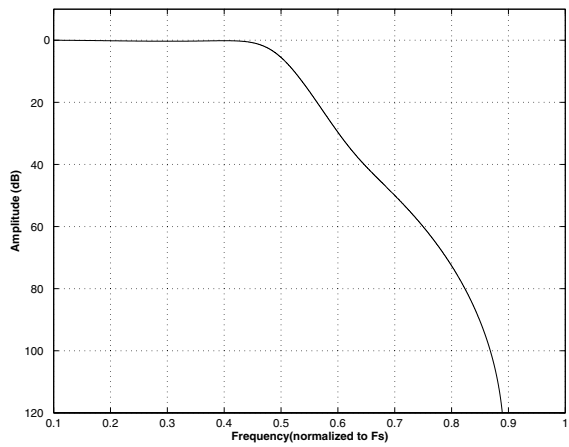
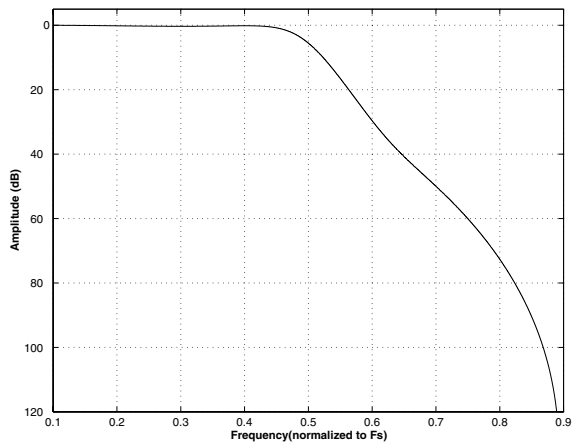
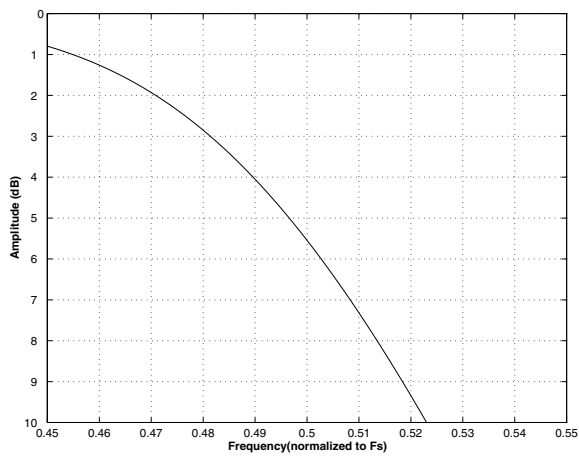
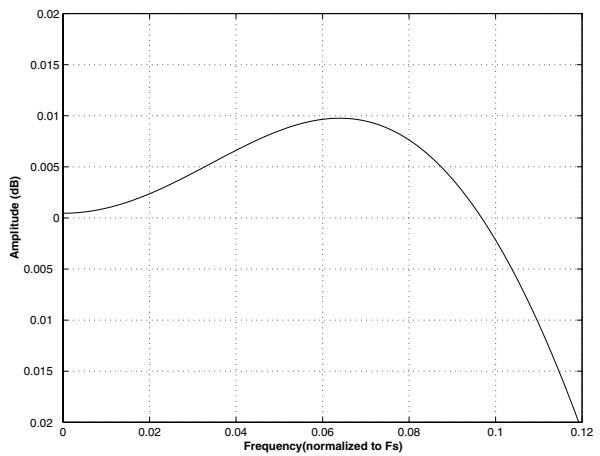


Figure 29. Single-Speed (slow) Transition Band


Figure 30. Single-Speed (slow) Transition Band (detail)

Figure 31. Single-Speed (slow) Passband Ripple

Figure 32. Double-Speed (fast) Stopband Rejection

Figure 33. Double-Speed (fast) Transition Band

Figure 34. Double-Speed (fast) Transition Band (detail)

Figure 35. Double-Speed (fast) Passband Ripple


Figure 36. Double-Speed (slow) Stopband Rejection

Figure 37. Double-Speed (slow) Transition Band

Figure 38. Double-Speed (slow) Transition Band (detail)

Figure 39. Double-Speed (slow) Passband Ripple

Figure 40. Quad-Speed (fast) Stopband Rejection

Figure 41. Quad-Speed (fast) Transition Band


Figure 42. Quad-Speed (fast) Transition Band (detail)

Figure 43. Quad-Speed (fast) Passband Ripple

Figure 44. Quad-Speed (slow) Stopband Rejection

Figure 45. Quad-Speed (slow) Transition Band

Figure 46. Quad-Speed (slow) Transition Band (detail)

Figure 47. Quad-Speed (slow) Passband Ripple

8. REFERENCES

1. *How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters*, by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
2. CDB4364 data sheet, available at <http://www.cirrus.com>.
3. *Design Notes for a 2-Pole Filter with Differential Input*, by Steven Green. Cirrus Logic Application Note AN48
4. *The I²C-Bus Specification: Version 2.0*, Philips Semiconductors, December 1998. <http://www.semiconductors.philips.com>
5. AN282 "The 2-Channel Serial Audio Interface: A Tutorial"

9. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full-scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

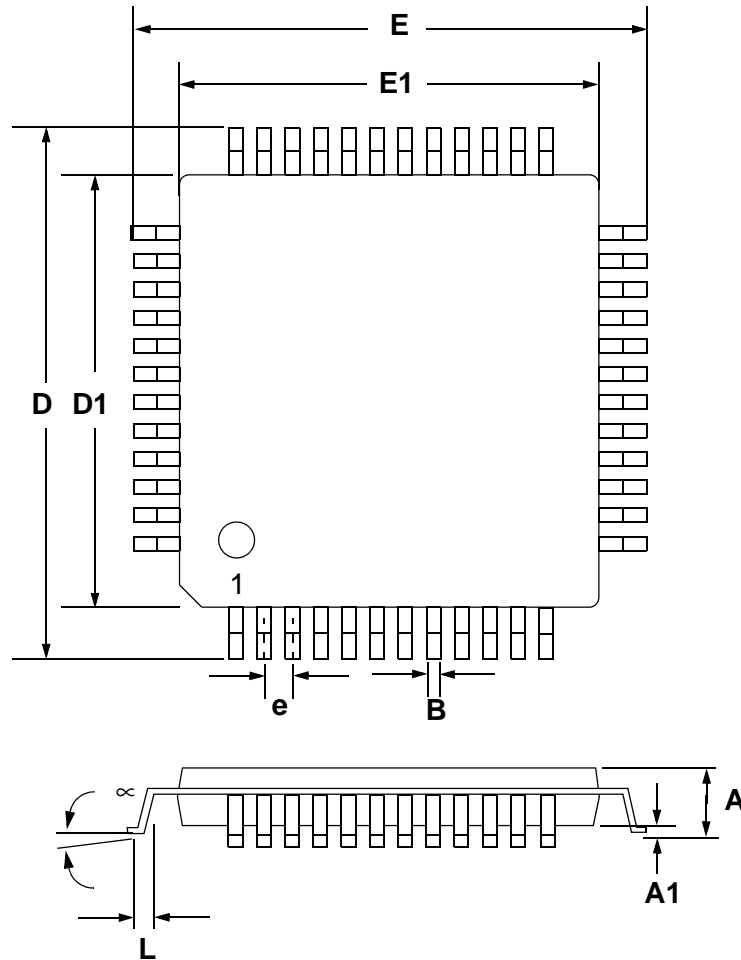
The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

10.PACKAGE DIMENSIONS
48L LQFP PACKAGE DRAWING


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.055	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.009	0.011	0.17	0.22	0.27
D	0.343	0.354	0.366	8.70	9.0 BSC	9.30
D1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
E	0.343	0.354	0.366	8.70	9.0 BSC	9.30
E1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
e*	0.016	0.020	0.024	0.40	0.50 BSC	0.60
L	0.018	0.24	0.030	0.45	0.60	0.75
∞	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm
 Controlling dimension is mm.
 JEDEC Designation: MS022

11.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4364	114 dB, 192 kHz 6-channel D/A Converter	48-pin LQFP	YES	Commercial	-40° to +85° C	Tray	CS4364-CQZ
						Tape & Reel	CS4364-CQZR
CDB4364	CS4364 Evaluation Board		-	-	-	-	CDB4364

12. REVISION HISTORY

Release	Changes
A1	Initial Release
F1	<p>Corrected DAC Pair Disable register description in “DAC Pair Disable (DACx_DIS)” on page 34</p> <p>Added note to Digital Interface Format register description in “Digital Interface Format (DIF)” on page 34</p> <p>Removed TDM Mode functionality</p> <p>Removed Automotive Grade</p> <p>Added PCM mode format changeable in reset only to “Mode Select” on page 21</p> <p>Updated ambient operating temperature range for commercial grade</p> <p>Updated Full Scale Differential Output Voltage in “DAC Analog Characteristics” on page 9</p> <p>Updated VD power supply current and package thermal resistance in Power and Thermal Characteristics</p> <p>Updated “Digital Characteristics” on page 13</p> <p>Updated Legal Information under “IMPORTANT NOTICE” on page 50</p>

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find one nearest you, go to www.cirrus.com.

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