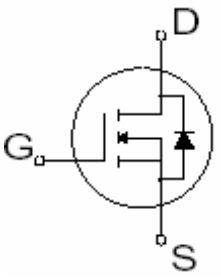
GOOD-ARK

SSFP2N65

StarMOS^T Power MOSFET

- Extremely high dv/dt capability
- Low Gate Charge Qg results in Simple Drive Requirement
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



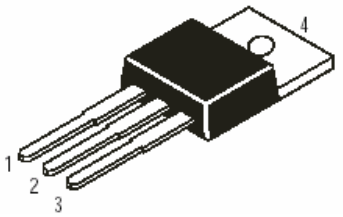
V_{DSS} = 650V

I_{D25} = 2.0A

$R_{DS(ON)}$ = 4.7 Ω

Description

StarMOS is a new generation of high voltage N–Channel enhancement mode power MOSFETs. This new technology minimises the JFET effect, increases packing density and reduces the on-resistance. StarMOS also achieves faster switching speeds through optimised gate layout with planar stripe DMOS technology.



Pin1–Gate
Pin2–Drain
Pin1–Source

Application

- Switching application

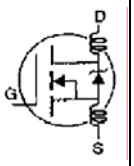
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D@Tc=25˚C	Continuous Drain Current,V_{GS}@10V	2.0	A
I_D@Tc=100˚C	Continuous Drain Current,V_{GS}@10V	1.35	
I_{DM}	Pulsed Drain Current ①	8	
P_D@Tc=25˚C	Power Dissipation	54	W
	Linear Derating Factor	0.43	W/˚C
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy ②	120	mJ
I_{AR}	Avalanche Current ①	2.0	A
E_{AR}	Repetitive Avalanche Energy ①	5.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	－55 to +175	℃
	Soldering Temperature, for 10 seconds	300(1.6mm from case)	
	Mounting Torque,6-32 or M3 screw	10 lbf•in(1.1N•m)	

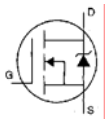
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	—	2.32	℃/W
$R_{\theta CS}$	Case-to-Sink,Flat,Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	50	

Electrical Characteristics @T_J=25˚C(unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	650	—	—	V	V_{GS}=0V,I_D=250μA
△$V_{(BR)DSS}$/△T_J	Breakdown Voltage Temp.Coefficient	—	0.6	—	V/˚C	Reference to 25˚C,I_D=250μA
$R_{DS(on)}$	Static Drain-to-Source On-resistance	—	3.6	4.7	Ω	V_{GS}=10V,I_D=1A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS},I_D=250μA
gfs	Forward Transconductance	—	5.0	—	S	V_{DS}=40V,I_D=1A
I_{DSS}	Drain-to-Source Leakage current	—	—	1	μA	V_{DS}=650V,V_{GS}=0V
		—	—	10		V_{DS}=480V,V_{GS}=0V,T_J=150˚C
I_{GSS}	Gate-to-Source Forward leakage	—	—	100	nA	V_{GS}=30V
	Gate-to-Source Reverse leakage	—	—	-100		V_{GS}=-30V
Qg	Total Gate Charge	—	8.5	12	nC	I_D=2A
Qgs	Gate-to-Source charge	—	1.3	—		V_{DS}=480V
Qgd	Gate-to-Drain("Miller") charge	—	4.1	—		V_{GS}=10V
td(on)	Turn-on Delay Time	—	9	28	nS	V_{DD}=300V
tr	Rise Time	—	25	60		I_D=2A
td(off)	Turn-Off Delay Time	—	24	58		R_G=25Ω
tf	Fall Time	—	28	66		
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm(0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
Ciss	Input Capacitance	—	180	235	pF	V_{GS}=0V
Coss	Output Capacitance	—	20	25		V_{DS}=25V
Crss	Reverse Transfer Capacitance	—	4.3	5.6		f=1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	8		
V_{SD}	Diode Forward Voltage	—	—	1.4	V	T_J=25˚C,I_S=2A,V_{GS}=0V ④
trr	Reverse Recovery Time	—	230	—	nS	T_J=25˚C,I_F=2A
Qrr	Reverse Recovery Charge	—	1.0		nC	di/dt=100A/μs ④
ton	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by Ls + L_D)				

Notes:

① Repetitive rating;pulse width limited by max.junction temperature(see figure 11)

② L = 56mH, IAS =2 A, VDD = 50V, RG = 25 ∧, Starting TJ = 25°C

③ I_{SD}≤2A,di/dt≤200A/μS,V_{DD}≤$V_{(BR)DSS}$, TJ≤25˚C

④ Pulse width≤300μS; duty cycle≤2%