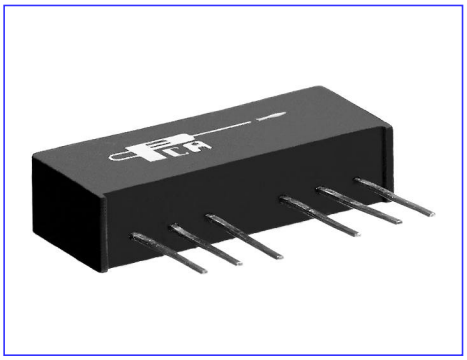
High Speed LAN Interface Module

EPF8076



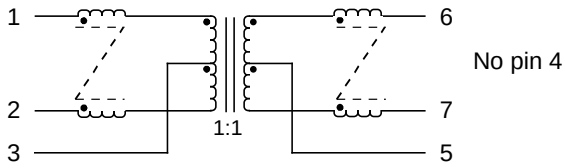
- Optimized for ML6673
- Recommended for 10/100, 100 BX, 155 Mb/s applications (requiring 1:1 magnetics)
- Guaranteed to operate with 8 mA DC bias at 70°C
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards

Electrical Parameters @ 25° C

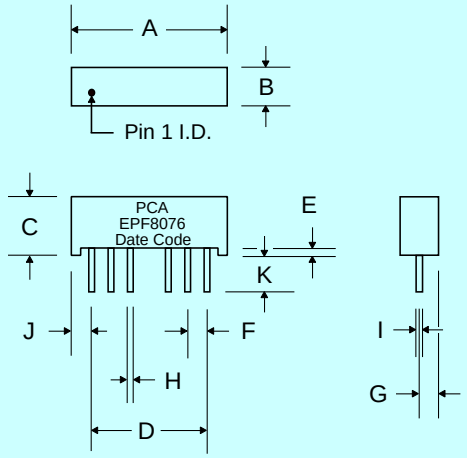
OCL @ 70°C	Insertion Loss (dB Max.)			Return Loss (dB Min.)			Common Mode Rejection (dB Min.)		
100 KHz, 0.1 Vrms 8 mA DC Bias	1-80 MHz	80-100 MHz	100-150 MHz	1-32 MHz	32-62 MHz	62-100 MHz	50 MHz	100 MHz	200 MHz
Cable Side	Xmit	Xmit	Xmit	Xmit	Xmit	Xmit	Xmit	Xmit	Xmit
350µH	-1	-1	-3	-20	-17	-12	-50	-45	-40

• **Isolation** : 1500 Vrms • **Impedance** : 100 Ω • **Rise Time** : 3.0 nS Max. •

Schematic



Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(Millimeters) Min.	Max.	Nom.
A	.790	.810		20.07	20.57	
B	.180	.200		4.57	5.08	
C	.300	.320		7.62	8.13	
D	.700	Typ.		17.78	Typ.	
E	.020	.030		.508	.762	
F	.090	Typ.		2.54	Typ.	
G			.090			2.29
H	.016	.022		.406	.559	
I	.008	.012		.203	.305	
J	.065	Typ.		1.65	Typ.	
K	.125	.145		3.18	3.68	

PCA ELECTRONICS, INC.
16799 SCHOENBORN ST.
NORTH HILLS, CA 91343

CSF8076a Rev. - 8/22/97

TEL: (818) 892-0761
FAX: (818) 894-5791
http://www.pcainc.com

High Speed LAN Interface Module

EPF8076

The circuit below is a guideline for interconnecting PCA's EPF8076 with a typical 100 BX PHY chip for 100 Mb/s applications over UTP cable. Further details of system design, such as chip pin-out, etc. should be obtained from the specific chip manufacturer. The package is a minature SIP, built for convenience of dense board designs for both NIC's and multiport applications. Each port requires two such devices.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 100/155 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the specific chip preset template control resistors to get at least 2.12V pk-pk across the transmit side input pins.

It is recommended that system designers do not ground the receiver side center tap, via a capacitor. This may worsen EMI, specifically if the secondary "common mode termination" is pulled to chassis ground as shown.

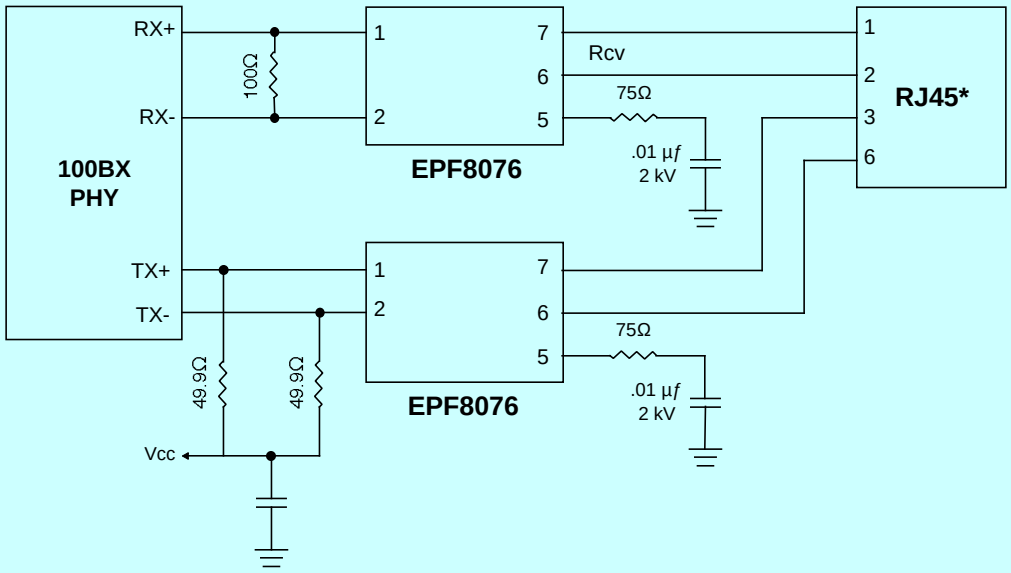
Pulling unused pins on the RJ45 to chassis via 50 Ω has been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75 Ω shown from the center taps of the secondary may be taken to chassis ground via a suitable cap. This depends upon the user's design, EMI margin, etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from pins of EPF8076 the chip side. There need not be any ground plane beyond this point.

For best results, the PCB designer should design the outgoing traces preferably to be 50 Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for 100 BX over UTP



Notes : * Pin-outs shown are for DCE configurations : e.g. Hubs, Repeaters

PCA ELECTRONICS, INC.
16799 SCHOENBORN ST.
NORTH HILLS, CA 91343

TEL: (818) 892-0761
FAX: (818) 894-5791
http://www.pcainc.com