



**AOTF404**  
**N-Channel Enhancement Mode Field Effect Transistor**

**General Description**

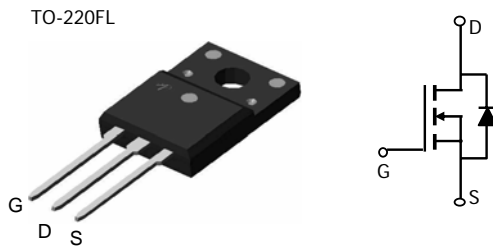
The AOTF404/L uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is suitable for use in high voltage synchronous rectification, load switching and general purpose applications.

- RoHS Compliant
- AOTF404L Halogen Free

**Features**

$V_{DS}$  (V) = 105V  
 $I_D$  = 26 A ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 28 m $\Omega$  ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 31 m $\Omega$  ( $V_{GS}$  = 6V)

**100% UIS Tested!**



**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	105	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	26
		$T_C=100^\circ\text{C}$	18
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	90	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	5.8
		$T_A=70^\circ\text{C}$	4.5
Avalanche Current <sup>C</sup>	$I_{AR}$	37	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	68	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	43
		$T_C=100^\circ\text{C}$	21
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	2.2
		$T_A=70^\circ\text{C}$	1.38
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	10	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	48.5	58
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	2.9	3.5	$^\circ\text{C/W}$

**Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=10\text{mA}$ , $V_{GS}=0\text{V}$	105			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=105\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 25\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	2.5	3.2	4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$	90			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=20\text{A}$		21	28	m $\Omega$
		$T_J=125^\circ\text{C}$		39	47	
		$V_{GS}=6\text{V}$ , $I_D=20\text{A}$		23.5	31	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=20\text{A}$		73		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.72	1	V
$I_S$	Maximum Body-Diode Continuous Current				55	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=25\text{V}$ , $f=1\text{MHz}$	1630	2038	2445	pF
$C_{oss}$	Output Capacitance		142	204	265	pF
$C_{rss}$	Reverse Transfer Capacitance		51	85	119	pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$	0.65	1.3	1.95	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=50\text{V}$ , $I_D=20\text{A}$	30.8	38.5	46	nC
$Q_{gs}$	Gate Source Charge		6.4	8	9.6	nC
$Q_{gd}$	Gate Drain Charge		8	10	14	nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$ , $V_{DS}=50\text{V}$ , $R_L=2.7\Omega$ , $R_{GEN}=3\Omega$		12.7		ns
$t_r$	Turn-On Rise Time			8.2		ns
$t_{D(off)}$	Turn-Off Delay Time			31.5		ns
$t_f$	Turn-Off Fall Time			11.2		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=20\text{A}$ , $dI/dt=500\text{A}/\mu\text{s}$	34	49	64	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=20\text{A}$ , $dI/dt=500\text{A}/\mu\text{s}$	337	481	625	nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B. The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ .

D. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using  $<300 \mu\text{s}$  pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175^\circ\text{C}$ .

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

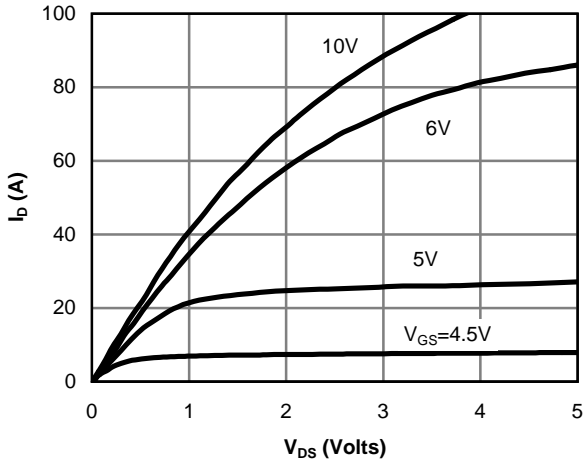


Fig 1: On-Region Characteristics

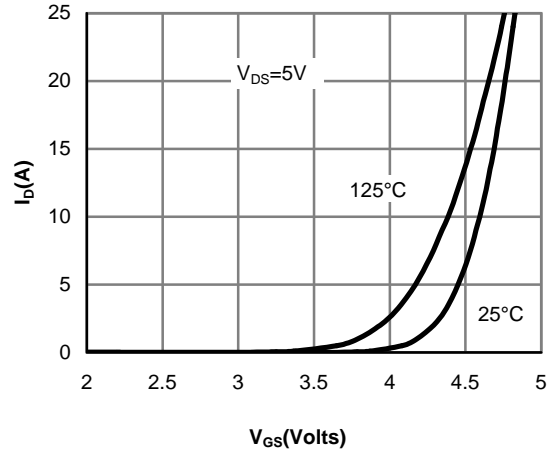


Figure 2: Transfer Characteristics

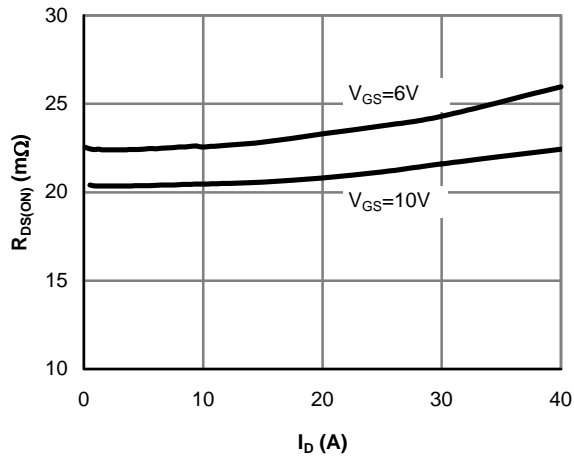


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

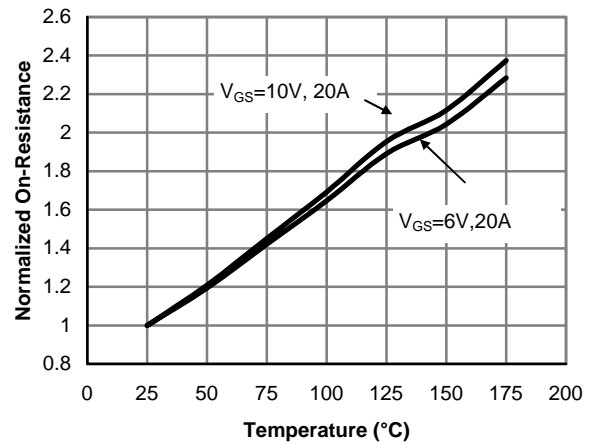


Figure 4: On-Resistance vs. Junction Temperature

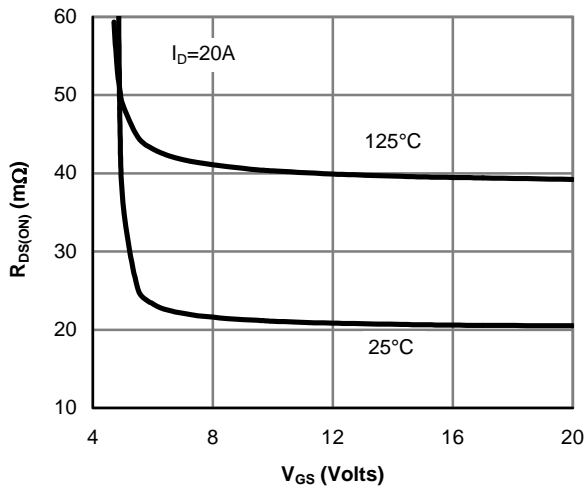


Figure 5: On-Resistance vs. Gate-Source Voltage

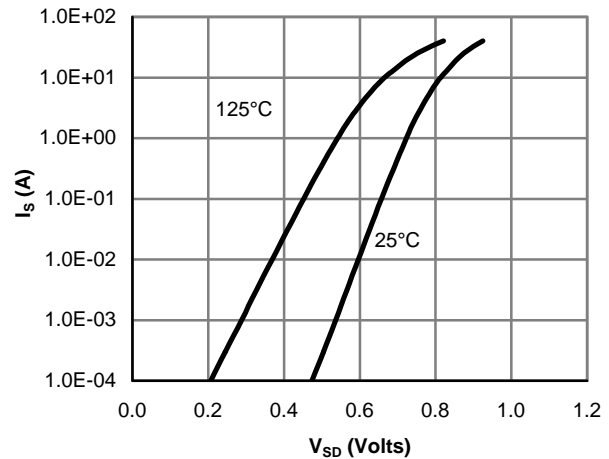


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

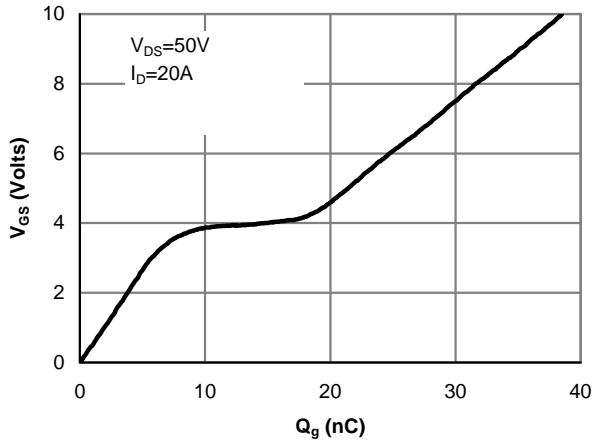


Figure 7: Gate-Charge Characteristics

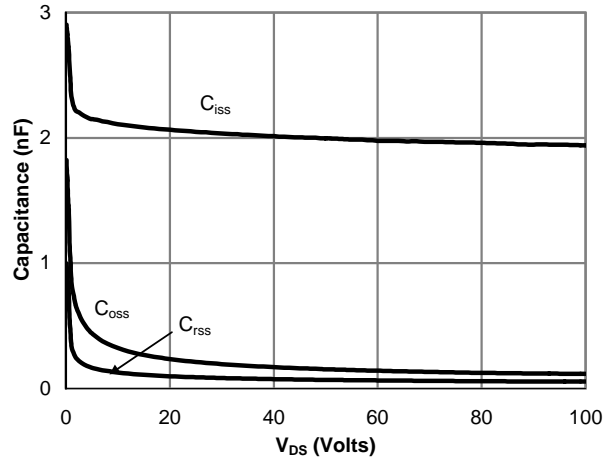


Figure 8: Capacitance Characteristics

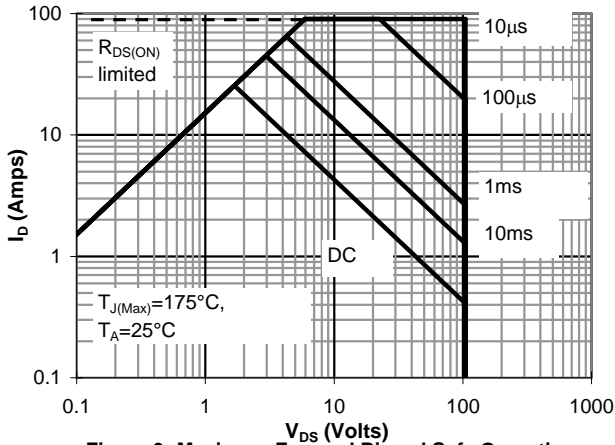


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

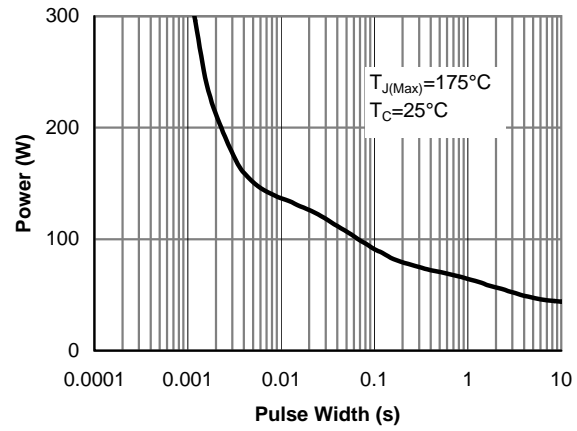


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

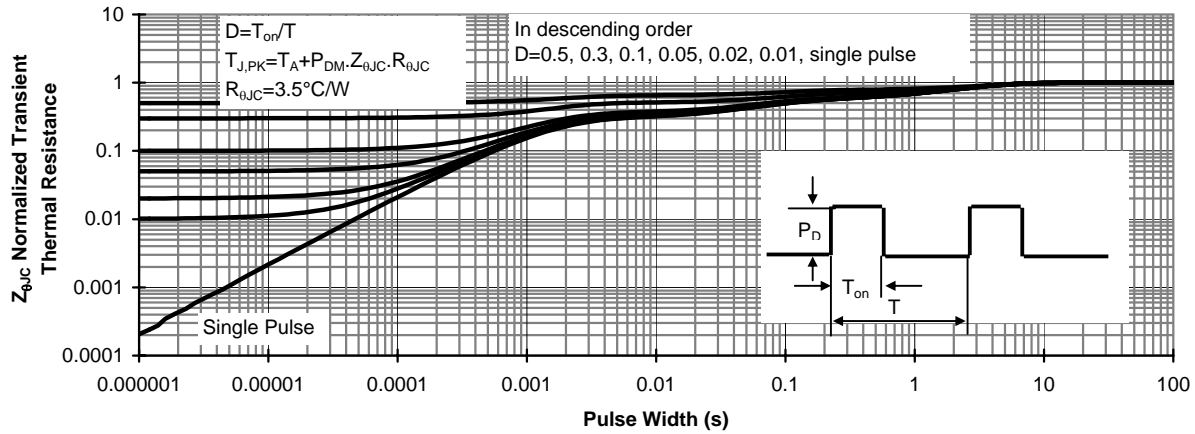


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

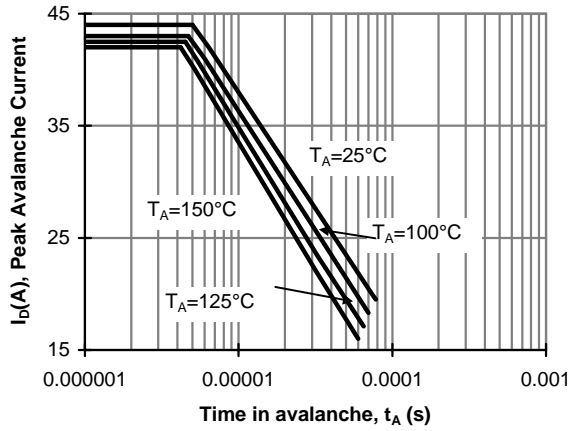


Figure 12: Single Pulse Avalanche capability

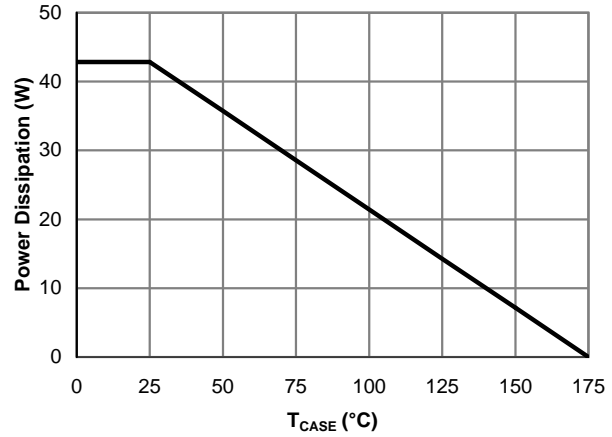


Figure 13: Power De-rating (Note B)

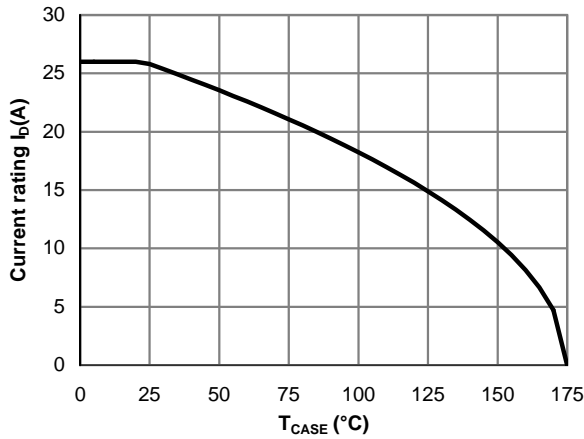


Figure 14: Current De-rating (Note B)

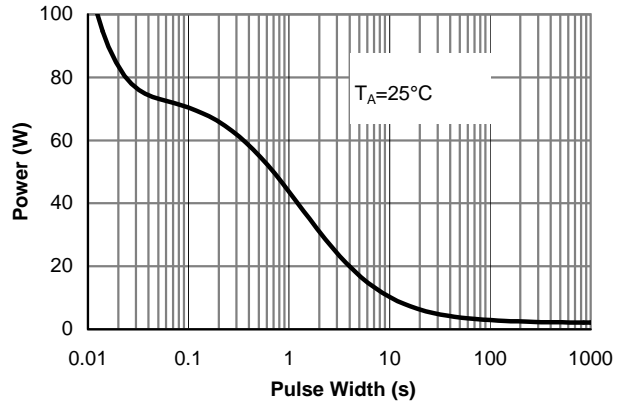


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

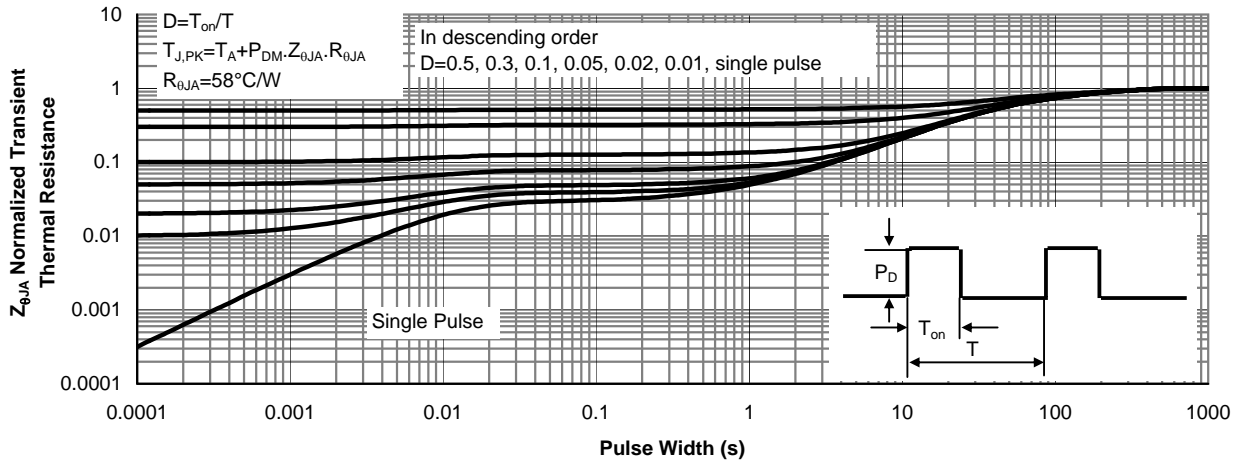
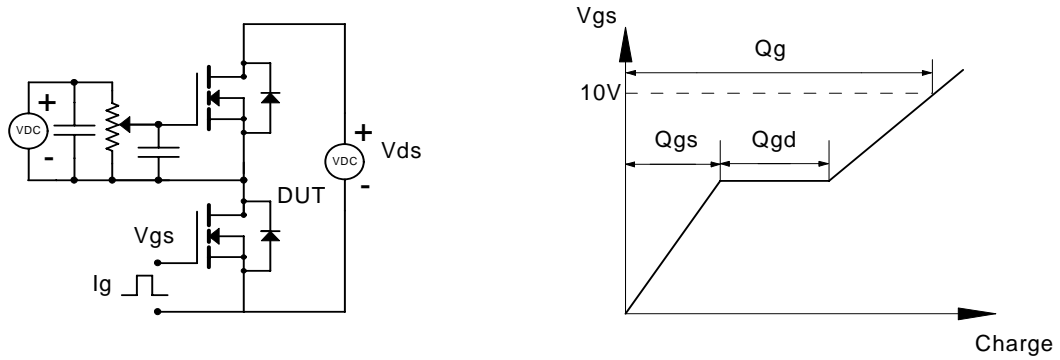
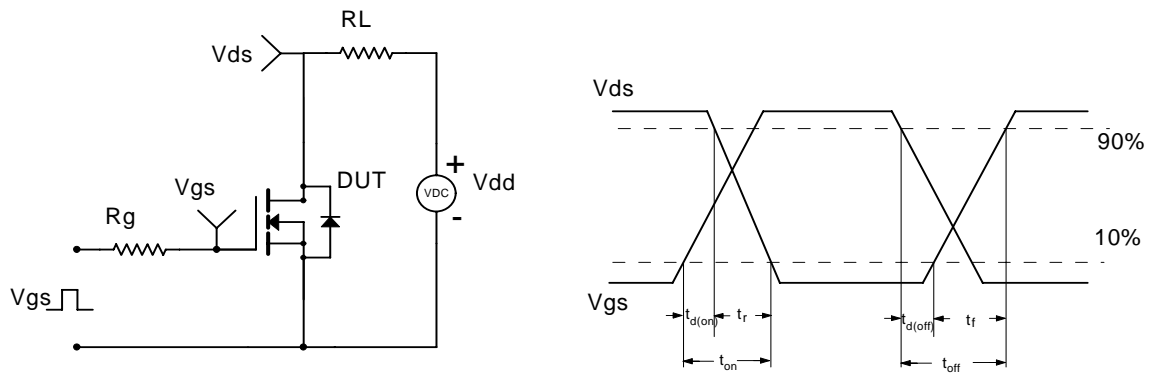


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

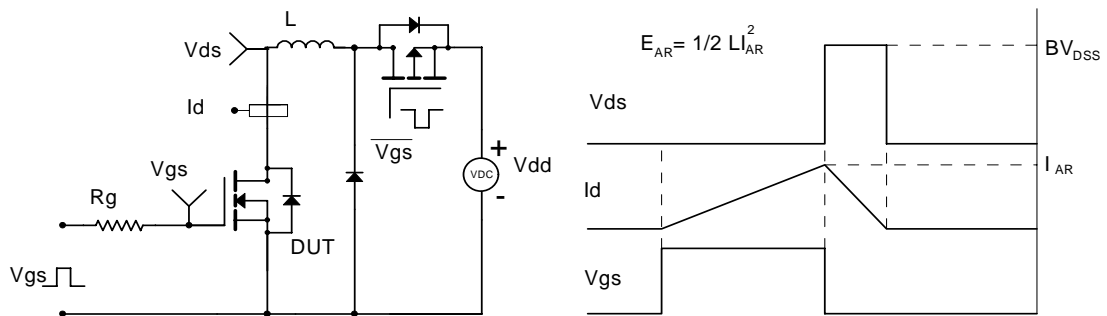
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

