POLA Point-of-Load Alliance

10-A, 12-V Input Non-Isolated Wide-Output Adjust Power Module

REVISION 00 (4DEC2003)

ADVANCE INFORMATION

NOMINAL SIZE = 1 in x 0.62 in (25,4 mm x 15,75 mm)

Features

- Up to 10-A Output Current
- 12-V Input Voltage
- Wide-Output Voltage Adjust (1.2 V to 5.5 V)
- Efficiencies up to 95 %
- 225 W/in³ Power Density
- On/Off Inhibit
- Output Voltage Sense
- Margin Up/Down Controls
- Under-Voltage Lockout
- Auto-Track™ Sequencing
- Output Over-Current Protection (Non-Latching, Auto-Reset)
- Operating Temp: –40 to +85 °C
- IPC Lead Free 2
- Safety Agency Approvals (Pending) UL 1950, CSA 22.2 950, & EN60950
- Point-of-Load Alliance (POLA) Compatible

Description

The ATH10K12 series is a non-isolated power module, and part of a new class of complete DC/DC converters from Texas Instruments. These modules are small in size, and a feature-rich alternative for applications requiring up to 10 A of load current.

Its small footprint, (1 in × 0.62 in) and industry leading features makes this module suitable for space conscious digital systems that incorporate multiple processors.

The ATH10K12 module operates from a 12-V input bus voltage to provide step-down power conversion to any output voltage over the range, 1.2 V to 5.5 V. The output voltage is set using a single resistor.

This product includes Auto-Track™ Sequencing. Auto-Track greatly simplifies the task of supply voltage sequencing in a power system, by enabling modules to track each other, or any other external voltage, during power up and power down.

Other features include an on/off inhibit and margin up/down controls. An output voltage sense ensures tight load regulation. A non-latching over-current trip protects against load faults.

Target applications are complex digital systems that incorporate the industry's latest high-speed DSPs, ASICs, FPGAs, micro-processors, and bus drivers.

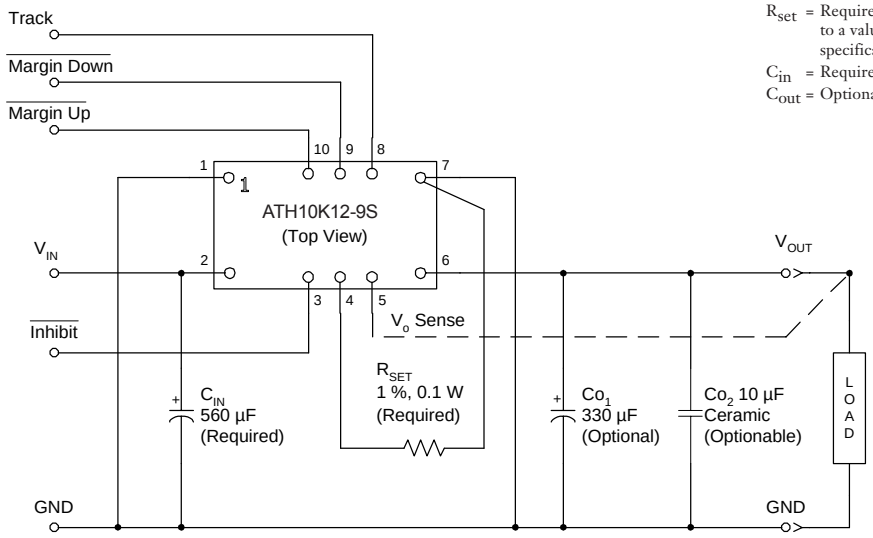
Pin Configuration

Pin	Function
1	GND
2	V_{in}
3	Inhibit *
4	V_o Adjust
5	V_o Sense
6	V_{out}
7	GND
8	Track
9	Margin Down *
10	Margin Up *

* *Denotes negative logic:*
Open = Normal operation
Ground = Function active

Auto-Track™ Sequencing

Standard Application



R_{set} = Required to set the output voltage to a value higher than 1.2 V. (See specification table for values)
C_{in} = Required 560 µF capacitor
C_{out} = Optional 330 µF capacitor

Ordering Information

Input Voltage	Output Voltage	Output Current	Model Number
10.8V to 13.2V	**1.2V[1] to 5.5V**	**10A**	**ATH10K12-9(S)(J)**

Options:
"-J" - Through-hole Termination, Tray Packaging
"-SJ" - SMT Termination, Tray Packaging
"-S" - SMT Termination, T&R Packaging

Notes:
[1]Preset output voltage is 1.2V; externally adjustable to 5.5V through the Vo,Adjust pin

Pin Descriptions

Vin: The positive input voltage power node to the module, which is referenced to common *GND*.

Vout: The regulated positive power output with respect to the *GND* node.

GND: This is the common ground connection for the *Vin* and *Vout* power connections. It is also the 0 VDC reference for the control inputs.

Inhibit: The Inhibit pin is an open-collector/drain negative logic input that is referenced to *GND*. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the *Inhibit* control is active, the input current drawn by the regulator is significantly reduced. If the *Inhibit* pin is left open-circuit, the module will produce an output whenever a valid input source is applied.

Vo Adjust: A 1 % 0.1 W resistor must be directly connected between this pin and pin 7 (*GND*) to set output voltage to a value higher than 1.2 V. The temperature stability of the resistor should be 100 ppm/°C or better. The set point range is from 1.2 V to 5.5 V. The resistor value required for a given output voltage may be calculated from the following formula. If left open circuit the output voltage will default to its lowest value. For further information on output voltage adjustment consult the related application note.

$$R_{set} = 10\ k\Omega \cdot \frac{0.8\ V}{V_{out} - 1.2\ V} - 1.82\ k\Omega$$

The specification table gives the preferred resistor values for a number of standard output voltages.

Vo Sense: The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy *Vo Sense* should be connected to *Vout*. It can also be left disconnected.

Track: This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the output will follow the voltage at the *Track* pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, the input may be left unconnected. *Note: Due to the under-voltage lockout, this feature does not allow the output from the module to follow its own input voltage during power up. For more information, consult the related application note.*

Margin Down: When this input is asserted to *GND*, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is not TTL compatible. A lower percent change can be accomodated with a series resistor. For further information, consult the related application note.

Margin Up: When this input is asserted to *GND*, the output voltage is increased by 5%. The input requires an open-collector (open-drain) interface. It is not TTL compatible. The percent change can be reduced with a series resistor. For further information, consult the related application note.

ADVANCE INFORMATION

ADVANCE INFORMATION

Environmental & Absolute Maximum Ratings (Voltages are with respect to GND)

Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Track Input Voltage	V_{track}		–0.2	—	V_{in}	V
Operating Temperature Range	T_a	Over V_{in} Range	–40 (i)	—	85	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module body or pins			215 (ii)	°C
Storage Temperature	T_s	—	–40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	—	TBD	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	—	TBD	—	G's
Weight	—		—	5	—	grams
Flammability	—	Meets UL 94V-O				

Notes: *(i) For operation below 0 °C the external capacitors must have stable characteristics. Use either a low ESR tantalum, Os-Con, or ceramic capacitor.*
(ii) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum. For further guidance refer to the application note, "Reflow Soldering Requirements for Plug-in Power Surface Mount Products."

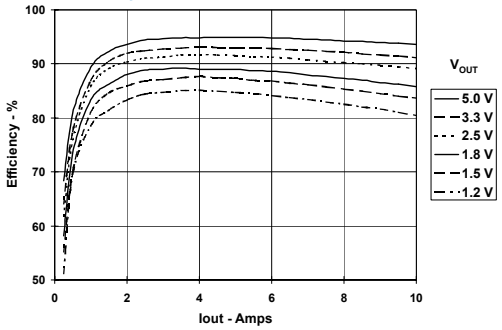
Specifications (Unless otherwise stated, T_a =25 °C, V_{in} =12 V, V_{out} =3.3 V, C_{in} =560 µF, Co_1 =0 µF, and I_o =I_o max)

Characteristics	Symbols	Conditions	ATH10K12 Min	ATH10K12 Typ	ATH10K12 Max	Units
Output Current	I_o	1.2 V ≤ V_o ≤ 5.5 V, 85 °C, 200 LFM airflow 25 °C, natural convection	0 0	— —	10 (1) 10 (1)	A
Input Voltage Range	V_{in}	Over I_o range	10.8	—	13.2	V
Set-Point Voltage Tolerance	V_o tol		—	—	±2 (2)	%V_o
Temperature Variation	ΔReg_{temp}	–40 °C <T_a < +85 °C	—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	Over V_{in} range	—	±10	—	mV
Load Regulation	ΔReg_{load}	Over I_o range	—	±12	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40 °C ≤ T_a ≤ +85 °C	—	—	±3	%V_o
Efficiency	η	I_o =8 A, R_{SET} = 280 Ω, V_o = 5.0 V	—	94	—	%
		R_{SET} = 2.0 kΩ, V_o = 3.3 V	—	92	—	
		R_{SET} = 4.32 kΩ, V_o = 2.5 V	—	90	—	
		R_{SET} = 8.06 kΩ, V_o = 2.0 V	—	88	—	
		R_{SET} = 11.5 kΩ, V_o = 1.8 V	—	87	—	
		R_{SET} = 24.3 kΩ, V_o = 1.5 V	—	85	—	
		R_{SET} = open cct, V_o = 1.2 V	—	83	—	
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth, V_o≤2.5 V	—	25 (3)	—	mVpp
		Co_2 =10µF ceramic, V_o >2.5 V	—	1 (3)	—	% V_o
Over-Current Threshold	I_o trip	Reset, followed by auto-recovery	—	20	—	A
Transient Response		1 A/µs load step, 50 to 100 % $I_o$max, Co_1 =330 µF				
	t_{tr}	Recovery Time	—	70	—	µSec
	ΔV_{tr}	V_o over/undershoot	—	100	—	mV
Margin Up/Down Adjust	V_o adj		—	± 5	—	%
Margin Input Current (pins 9 /10)	I_{IL} margin	Pin to GND	—	– 8 (4)	—	µA
Track Input Current (pin 8)	I_{IL} track	Pin to GND	—	—	–0.13 (5)	mA
Track Slew Rate Capability	dV_{track}/dt	$\lvert V_{track} - V_o \rvert$ ≤ 50 mV and V_{track} < V_o(nom)	5	—	—	V/ms
Under-Voltage Lockout	UVLO	V_{in} increasing V_{in} decreasing	— 8.8	9.5 9	10.4 —	V
Inhibit Control (pin3)		Referenced to GND				
Input High Voltage	V_{IH}		V_{in} –0.5	—	Open (5)	V
Input Low Voltage	V_{IL}		–0.2	—	0.5	
Input Low Current	I_{IL} inhibit	Pin to GND	—	–0.24	—	mA
Input Standby Current	I_{in} inh	Inhibit (pin 3) to GND, Track (pin 8) open	—	10	—	mA
Switching Frequency	f_s	Over V_{in} and I_o ranges	300	350	400	kHz
External Input Capacitance	C_{in}		560 (6)	—	—	µF
External Output Capacitance	C_{out}		0	330 (7)	TBD	µF
Reliability	MTBF	Per Bellcore TR-332 50 % stress, T_a =40 °C, ground benign	TBD	—	—	10^6 Hrs

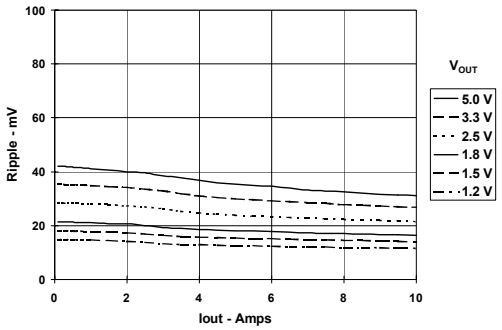
Notes: *(1) See SOA curves or consult factory for appropriate derating.*
(2) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1 % with 100 ppm/°C or better temperature stability.
(3) The pk-pk output ripple voltage is measured with an external 10 µF ceramic capacitor. See the standard application schematic.
(4) A small low-leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.
(5) This control pin has an internal pull-up to the input voltage Vin (7.5 V for pin 8). If it is left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.
(6) A 560 µF input capacitor are required for proper operation. The electrolytic capacitor must be rated for a minimum of 800 mA rms of ripple current. For further information, consult the related application note regarding capacitor selection.
(7) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load will improve the transient response.

Characteristic Data; V_{in} =12 V *(See Note A)*

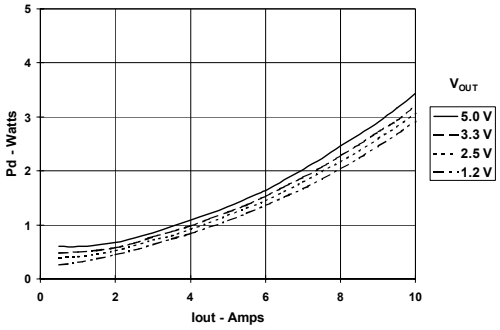
Efficiency vs Load Current



Output Ripple vs Load Current *(See Note 3 of Table)*

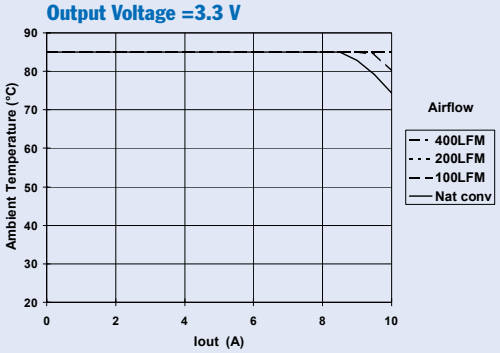


Power Dissipation vs Load Current



Safe Operating Area; V_{in} =12 V *(See Note B)*

Output Voltage =3.3 V



ADVANCE INFORMATION

The products listed hereunder are prototype or pre-production devices which have not been fully qualified to Astec's specifications. Product specifications are subject to change without notice. Astec makes no warranty, either expressed, implied, or statutory, including implied warranty of merchantability or fitness for a specific purpose, of these products.

Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.*

Adjusting the Output Voltage of the ATH10K12 Wide-Output Adjust Power Module

The *V_o Adjust* control (pin 4) is used to set the output voltage to a value higher than 1.2 V. The adjustment method requires the addition of a single external resistor, R_{set}, that must be connected directly between the *V_o Adjust* and *GND* pins [1]. Table 1-1 gives the preferred value for the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 1-2. Figure 1-1 shows the placement of the required resistor.

$$R_{set} = 10\,k\Omega \cdot \frac{0.8\ V}{V_{out} - 1.2\ V} - 1.82\,k\Omega$$

Table 1-1; Preferred Values of R_{set} for Standard Output Voltages

V_{out} (Standard)	R_{set} (Pref'd Value)	V_{out} (Actual)
5 V	280 Ω	5.009 V
3.3 V	2 kΩ	3.294V
2.5 V	4.32 kΩ	2.503 V
2 V	8.06 kΩ	2.010V
1.8 V	11.5 kΩ	1.801 V
1.5 V	24.3 kΩ	1.506 V
1.2 V	Open	1.200 V

Figure 1-1; V_o Adjust Resistor Placement

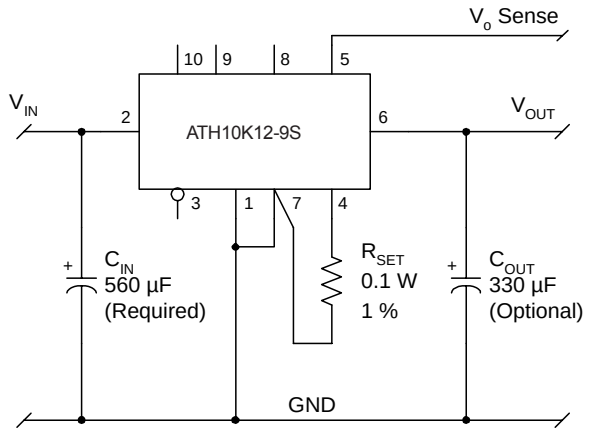


Table 1-2; Output Voltage Set-Point Resistor Values

V_a Req'd	R_{set}	V_a Req'd	R_{set}
1.200	Open	2.75	3.34 kΩ
1.225	318 kΩ	2.80	3.18 kΩ
1.250	158 kΩ	2.85	3.03 kΩ
1.275	105 kΩ	2.90	2.89 kΩ
1.300	78.2 kΩ	2.95	2.75 kΩ
1.325	62.2 kΩ	3.00	2.62 kΩ
1.350	51.5 kΩ	3.05	2.5 kΩ
1.375	43.9 kΩ	3.10	2.39 kΩ
1.400	38.2 kΩ	3.15	2.28 kΩ
1.425	33.7 kΩ	3.20	2.18 kΩ
1.450	30.2 kΩ	3.25	2.08 kΩ
1.475	27.3 kΩ	3.30	1.99 kΩ
1.50	24.8 kΩ	3.35	1.9 kΩ
1.55	21 kΩ	3.40	1.82 kΩ
1.60	18.2 kΩ	3.45	1.74 kΩ
1.65	16 kΩ	3.50	1.66 kΩ
1.70	14.2 kΩ	3.55	1.58 kΩ
1.75	12.7 kΩ	3.6	1.51 kΩ
1.80	11.5 kΩ	3.7	1.38 kΩ
1.85	10.5 kΩ	3.8	1.26 kΩ
1.90	9.61 kΩ	3.9	1.14 kΩ
1.95	8.85 kΩ	4.0	1.04 kΩ
2.00	8.18 kΩ	4.1	939 Ω
2.05	7.59 kΩ	4.2	847 Ω
2.10	7.07 kΩ	4.3	761 Ω
2.15	6.6 kΩ	4.4	680 Ω
2.20	6.18 kΩ	4.5	604 Ω
2.25	5.8 kΩ	4.6	533 Ω
2.30	5.45 kΩ	4.7	466 Ω
2.35	5.14 kΩ	4.8	402 Ω
2.40	4.85 kΩ	4.9	342 Ω
2.45	4.85 kΩ	5.0	285 Ω
2.50	4.33 kΩ	5.1	231 Ω
2.55	4.11 kΩ	5.2	180 Ω
2.60	3.89 kΩ	5.3	131 Ω
2.65	3.7 kΩ	5.4	85 Ω
2.70	3.51 kΩ	5.5	41 Ω

Notes:

1. Use a 0.1 W resistor. The tolerance should be 1 %, with temperature a stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 7 using dedicated PCB traces.
2. Never connect capacitors from *V_o Adjust* to either *GND* or *V_{out}*. Any capacitance added to the *V_o Adjust* pin will affect the stability of the regulator.

ATH10K12: Capacitor Recommendations

Input Capacitor

The recommended input capacitance is determined by 560 µF minimum capacitance and 1050 mArms minimum ripple current rating. A 10-µF ceramic capacitor can be used to reduce input ripple. This should be located between the input electrolytic and the module. A suggested ceramic part number is the Murata GRM31CR61C106K or similar 'X7R' capacitor.

Ripple current and <100 mΩ equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors. Tantalum capacitors have a recommended minimum voltage rating of 2 × (max. dc voltage + ac ripple). Tantalum capacitors are not recommended on the input bus as there are none with a sufficient voltage rating.

Output Capacitors: Optional

The recommended ESR of the output capacitor is less than or equal to 150 mΩ. Electrolytic capacitors have marginal ripple performance at frequencies above 400 kHz but excellent low frequency transient response. Above the ripple frequency, ceramic capacitors are necessary to improve the transient response and reduce any high frequency noise components apparent during higher current excursions. Tantalum or Os-con types are recommended for applications where ambient temperatures fall below 0°C.

Tantalum Capacitors

Tantalum type capacitors can be used for the output but only the AVX TPS, Sprague 593D/594/595 or Kemet T495/T510 series. These capacitors are recommended over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution the TAJ series by AVX is not recommended. This series has considerably higher ESR, reduced power dissipation, and lower ripple current capability. The TAJ series is also less reliable than the AVX TPS series when determining power dissipation capability.

Ceramic Capacitors

Ceramic capacitors will compliment electrolytic types. Adding 10 µF or more ceramic capacitance will reduce ripple on the input and output bus. Output ripple and transient measurement accuracy is improved by measuring directly across a 10 µF ceramic capacitor.

Capacitor Table

Table 2-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The number of capacitors required at both the input and output buses is identified for each part type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Table 2-1: Input/Output Capacitors

Capacitor Vendor/ Series	Capacitor Characteristics					Quantity		
	Working Voltage	Value (µF)	(ESR) Equivalent Series Resistance	105°C Maximum Ripple Current (Irms)	Physical Size (mm)	Input Bus	Optional Output Bus	Vendor Part Number
Panasonic WA (SMT)	16 V	330	0.022 Ω	>4100 mA	10×10.2	2	1	EEFWA1C331P
FC-Radial	25 V	560	0.065 Ω	1205 mA	12.5×15	1	1	EEUFC1E561S
	25 V	1000	0.060 Ω	1100 mA	12.5×13.5	1	1	EEVFK1E102Q
FK (SMT)	35 V	680	0.060 Ω	1100 mA	12.5×13.5	1	1	EEVFK1V681Q
United Chemi-Con-FX	16 V	330	0.018 Ω	4500 mA	10×10.5	2	1	16FX330M
PS Series	16 V	330	0.014 Ω	>5050 mA	10×12.5	2	1	16PS330MJ12
LXZ	16 V	680	0.068 Ω	1050 mA	10×16	1	1	LXZ16VB681M10X16LL
PXA (SMT)	16 V	180x3	0.026 Ω	>3400 mA	10×7.7	3	1	PXA16VC181MJ80TP
Nichicon	25 V	560	0.060 Ω	1060 mA	12.5×15	1	1	UPM1E561MHH6
PM Series	25 V	680	0.055 Ω	1270 mA	16×15	1	1	UPM1E681MHH6
	35 V	560	0.048 Ω	1360 mA	16×15	1	1	UPM1V561MHH6
WG	25 V	330	0.15÷2 Ω	>1100 mA	10×10	2	2	UWG1E331MNR1GS
Os-con:								
SP	16 V	270	0.018 Ω	>3500 mA	10×10.5	2	1	16SP270M
SVP (SMT)	16 V	330	0.016 Ω	4700 mA	11×12	2	1	16SVP330M
AVX Tantalum	10 V	330	0.10 Ω	>2500 mA	7.3L ×5.7W	N/R (1)	1	TPSE337M010R0100 **(V_O<5.1V)**
TPS (SMT)	10 V	330	0.06 Ω	>3000 mA	×4.1H	N/R (1)	1	TPSV337M010R0060 **(V_O<5.1V)**
Kemet Tantalum	10 V	330	0.04 Ω	1600 mA	4.3W	N/R (1)	1	520X337M010AS **(V_O<5.1V)**
T520/T495 Series	10 V	220	0.07 Ω	>2000 mA	×7.3L	N/R (1)	1	T495X227M0100AS **(V_O<5.1V)**
(SMT)					×4.0H			
Sprague Tantalum	10 V	330	0.045 Ω	2360 mA	7.2L	N/R (1)	1	594D337X0010R2T **(V_O<5.1V)**
594D Series					×6W			
(SMT)					×4.1H			

(1) N/R –Not recommended. The voltage rating does not meet the minimum operating limits.

Features of the ATH Family of Non-Isolated Wide Output Adjust Power Modules

Point-of-Load Alliance

The ATH family of non-isolated, wide-output adjust power modules from Texas Instruments are optimized for applications that require a flexible, high performance module that is small in size. These products are part of the "Point-of-Load Alliance" (POLA), which ensures compatible footprint, interoperability and true second sourcing for customer design flexibility. The POLA is a collaboration between Texas Instruments, Artesyn Technologies, and Astec Power to offer customers advanced non-isolated modules that provide the same functionality and form factor. Product series covered by the alliance includes the ATH06 (6 A), ATH10 (10 A), ATH12/15 (12/15 A), ATH18/22 (18/22 A), and the ATH26/30 (26/30 A).

From the basic, "Just Plug it In" functionality of the 6-A modules, to the 30-A rated feature-rich ATH30 Series, these products were designed to be very flexible, yet simple to use. The features vary with each product. Table 3-1 provides a quick reference to the available features by product and input bus voltage.

Table 3-1; Operating Features by Series and Input Bus Voltage

Series	Input Bus	I_{OUT}	Adjust (Trim)	On/Off Inhibit	Over-Current	Pre-Bias Startup	Auto-Track™	Margin Up/Down	Output Sense	Thermal Shutdown
ATH06	3.3 V	6 A	•	•	•	•	•			
	5 V	6 A	•	•	•	•	•			
	12 V	6 A	•	•	•		•			
ATH10	3.3 V / 5 V	10 A	•	•	•	•	•	•	•	
	12 V	10 A	•	•	•		•	•	•	
ATH12/15	3.3 V / 5 V	15 A	•	•	•	•	•	•	•	
	12 V	12 A	•	•	•		•	•	•	
ATH18/22	3.3 V / 5 V	22 A	•	•	•	•	•	•	•	•
	12 V	18 A	•	•	•		•	•	•	•
ATH26/30	3.3 V / 5 V	30 A	•	•	•	•	•	•	•	•
	12 V	26 A	•	•	•	•	•	•	•	•

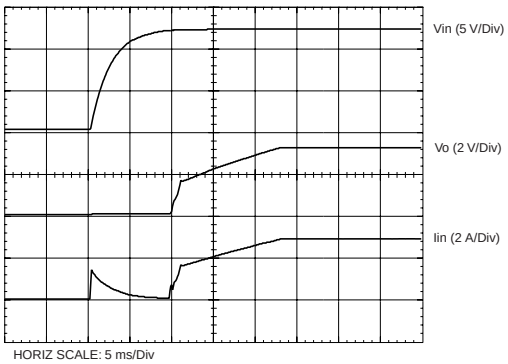
For simple point-of-use applications, the ATH06 (6A) provides operating features such as an on/off inhibit, output voltage trim, pre-bias startup (3.3/5-V input only), and over-current protection. The ATH10 (10 A), and ATH12/15 (12/15 A) include an output voltage sense, and margin up/down controls. Then the higher output current, ATH18/22 (18/22A) and ATH26/30 (26/30A) products incorporate over-temperature shutdown protection. All of the products referenced in Table 3-1 include Auto-Track™.

This is a feature unique to the ATH family, and was specifically designed to simplify the task of sequencing the supply voltage in a power system. These and other features are described in the following sections.

Power-Up Characteristics

When configured per their standard application all the ATH products will produce a regulated output voltage following the application of a valid input source voltage. All the modules include soft-start circuitry. This slows the initial rate in which the output voltage can rise, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry also introduces a short time delay (typically 5 ms-10 ms) into the power-up characteristic. This delay is from the point that a valid input source is recognized, to the initial rise of the output voltage. Figure 3-1 shows the power-up characteristic of the 10-A output product (ATH10K12), operating from a 12-V input bus and configured for a 3.3-V output. The waveforms were measured with a 5-A constant current load. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors.

Figure 3-1



Over-Current Protection

For protection against load faults, all modules incorporate output over-current protection. Applying a load that exceeds the regulator's over-current threshold will cause the regulated output to shut down. Following shutdown, a module will periodically attempt to recover by initiating a soft-start power-up. This is described as a "hiccup" mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Output On/Off Inhibit

For applications requiring output voltage on/off control, each series of the ATH family incorporates an output *Inhibit* control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the *Inhibit* pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_{in} with respect to *GND*.

Figure 3-2 shows the typical application of the inhibit function. Note the discrete transistor (Q_1). The *Inhibit* input has its own internal pull-up to V_{in} potential (12 V). The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

Turning Q_1 on applies a low voltage to the *Inhibit* control pin and disables the output of the module. If Q_1 is then turned off, the module will execute a soft-start power-up sequence. A regulated output voltage is produced within 20 msec. Figure 3-3 shows the typical rise in both the output voltage and input current, following the turn-off of Q_1. The turn off of Q_1 corresponds to the rise in the waveform, Q_1 V_{ds}. The waveforms were measured with a 5-A constant current load.

Figure 3-2

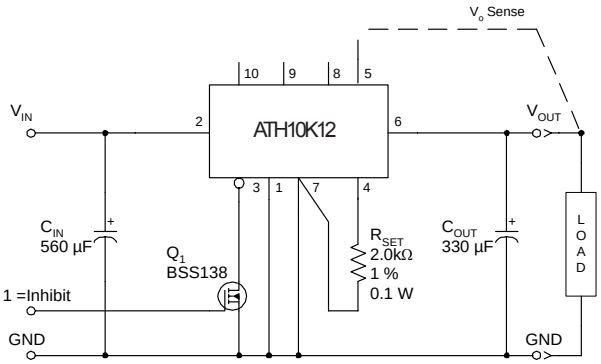
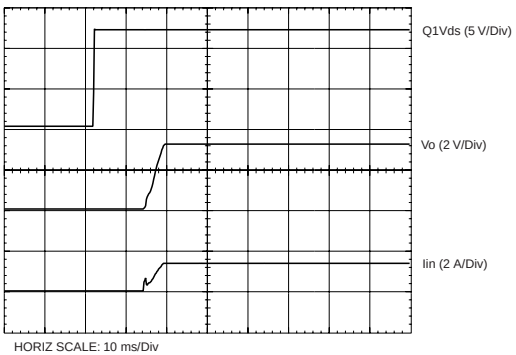


Figure 3-3



Remote Sense

The ATH10 (10A), ATH12/15 (12/15A), ATH18/22 (18/22A), and ATH26/30 (26/30A) products incorporate an output voltage sense pin, V_o *Sense*. The V_o *Sense* pin should be connected to V_{out} at the load circuit (see data sheet standard application). A remote sense improves the load regulation performance of the module by allowing it to compensate for any 'IR' voltage drop between itself and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance. Use of the remote sense is optional. If not used, the V_o *Sense* pin can be left open-circuit. An internal low-value resistor (15-Ω or less) is connected between the V_o *Sense* and V_{out}. This ensures the output voltage remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_{out} and *GND* pins, and that measured from V_o *Sense* to *GND*, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Over-Temperature Protection (OTP)

The ATH18/22 (18/22A) and ATH26/30 (26/30A) series of products have over-temperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's *Inhibit* control is automatically pulled low. This turns the output off. The output voltage will drop as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10 °C below the trip point.

Note: The over-temperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Auto-Track™ Function

The Auto-Track™ function is unique to the ATH family, and is available with the all "Point-of-Load Alliance" (POLA) products. Auto-Track™ was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, micro-processors, and ASICs.

How Auto-Track™ Works

Auto-Track™ works by forcing the module's output voltage to follow a voltage presented at the *Track* control pin. This control range is limited to between 0 V and the module's set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module's output remains at its set-point [1]. As an example, if the Track pin of a 2.5-V regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the Track pin rises to 3 V, the regulated output will not go higher than 2.5 V.

When under track control, the regulated output from the module follows the voltage at its Track pin on a volt-for-volt basis. By connecting the Track pin of a number of these modules together, the output voltages will follow a common signal during power-up and power-down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit [3]. The Track control also incorporates an internal RC charge circuit. This operates off the module's input voltage to produce a suitable rising waveform at power up.

Typical Application

The basic implementation of Auto-Track™ allows for simultaneous voltage sequencing of a number of Auto-Track™ compliant modules. Connecting the Track control pins of two or more modules forces the Track control of all modules to follow the same collective RC ramp waveform, and allows them to be controlled through a single transistor or switch; Q_1 in Figure 3-4.

To initiate a power-up sequence, it is recommended that the Track control be first pulled to ground potential. This should be done at or before input power is applied to the modules, and then held for at least 10 ms thereafter. This brief period gives the modules time to complete their internal soft-start initialization. Applying a logic-level high signal to the circuit's On/Off Control turns Q_1 on and applies a ground signal to the Track pins. After completing their internal soft-start intialization, the output of all modules will remain at zero volts while Q_1 is on.

10 ms after a valid input voltage has been applied to the modules, Q_1 may be turned off. This allows the track control voltage to automatically rise toward to the modules' input voltage. During this period the output voltage of each module will rise in unison with other modules, to its respective set-point voltage.

Figure 3-5 shows the output voltage waveforms from the circuit of Figure 3-4 after the On/Off Control is set from a high to a low-level voltage. The waveforms, Vo_1 and Vo_2 represent the output voltages from the two power modules, U_1 (3.3 V) and U_2 (2.0 V) respectively. Vo_1 and Vo_2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. Power down is the reverse of power up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power down is complete. It also requires that Q_1 be turned off relatively slowly. This is so that the Track control voltage does not fall faster than Auto-Track's slew rate capability, which is 5 V/ms. The components R_1 and C_1 in Figure 3-4 limit the rate at which Q_1 can pull down the Track control voltage. The values of 100 k-ohm and 0.047 µF correlate to a decay rate of about 0.6 V/ms.

The power-down sequence is initiated with a low-to-high transition at the On/Off Control input to the circuit. Figure 3-6 shows the power-down waveforms. As the Track control voltage falls below the nominal set-point voltage of each power module, then its output voltage decays with all the other modules under Auto-Track™ control.

Notes on Use of Auto-Track™

1. The Track pin voltage must be allowed to rise above the module's set-point voltage before the module can regulate at its adjusted set-point voltage.
2. The Auto-Track™ function will track almost any voltage ramp during power up, and is compatible with ramp speeds of up to 5 V/ms.
3. The absolute maximum voltage that may be applied to the Track pin is V_{in}. The open-circuit voltage is 0.56 × V_{in}, or 7.5 VDC maximum.
4. The module will not follow a voltage at its Track control input until it has completed its soft-start initialization. This takes about 10 ms from the time that the module has sensed that a valid voltage has been applied its input. During this period, it is recommended that the Track pin be held at ground potential.
5. Once its soft-start initialization is complete, the module is capable of both sinking and sourcing current when following the voltage at the Track pin.
6. The Auto-Track™ function can be disabled by connecting the *Track* pin to the input voltage (V_{in}) through a 1-kΩ resistor. When Auto-Track™ is disabled, the output voltage will rise faster following the application of input power.

***Auto-Track is a trademark of Texas Instruments, Inc.*

Figure 3-4; Sequenced Power Up & Power Down Using Auto-Track

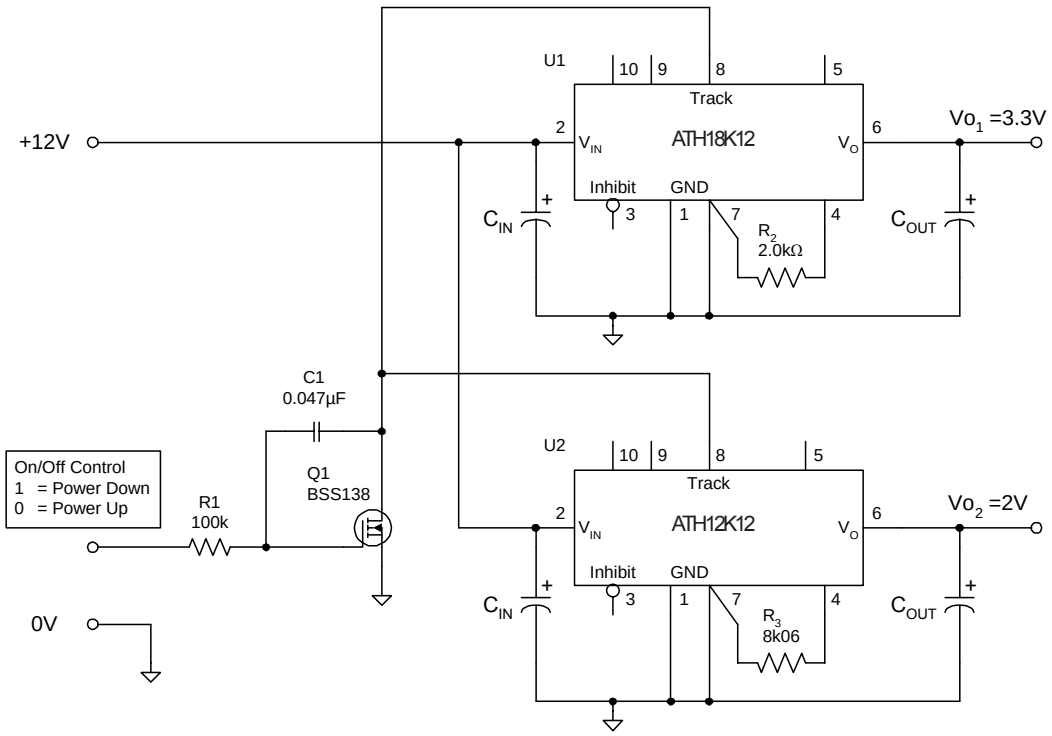


Figure 3-5; Simultaneous Power Up with Auto-Track Control

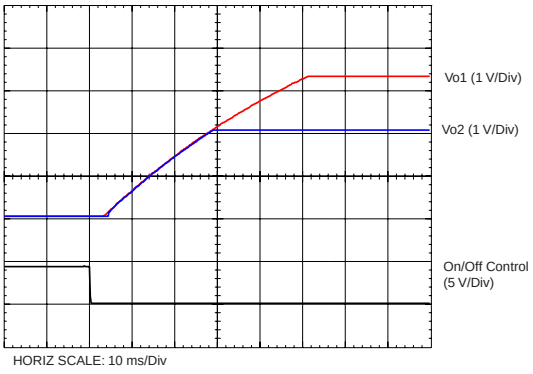
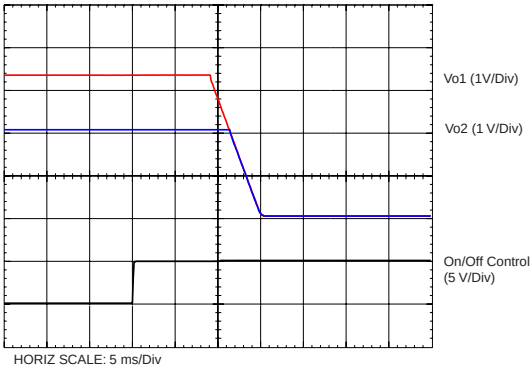


Figure 3-6; Simultaneous Power Down with Auto-Track Control



Margin Up/Down Controls

The ATH10 (10A), ATH12/15 (12/15A), ATH18/22 (18/22A), and ATH26/30 (26/30A) products incorporate *Margin Up* and *Margin Down* control inputs. These controls allow the output voltage to be momentarily adjusted [1], either up or down, by a nominal 5 %. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The ±5 % change is applied to the adjusted output voltage, as set by the external resistor, R_{set} at the *V_o Adjust* pin.

The 5 % adjustment is made by pulling the appropriate margin control input directly to the *GND* terminal [2]. A low-leakage open-drain device, such as an n-channel MOSFET or p-channel JFET is recommended for this purpose [3]. Adjustments of less than 5 % can also be accommodated by adding series resistors to the control inputs (See Figure 3-4). The value of the resistor can be selected from Table 3-2, or calculated using the following formula.

Up/Down Adjust Resistance Calculation

To reduce the margin adjustment to something less than 5 %, series resistors are required (See R_D and R_U in Figure 3-7). For the same amount of adjustment, the resistor value calculated for R_U and R_D will be the same. The formulas is as follows.

$$R_U \text{ or } R_D = \frac{499}{\Delta\%} - 99.8 \quad k\Omega$$

Where $\Delta\%$ = The desired amount of margin adjust in percent.

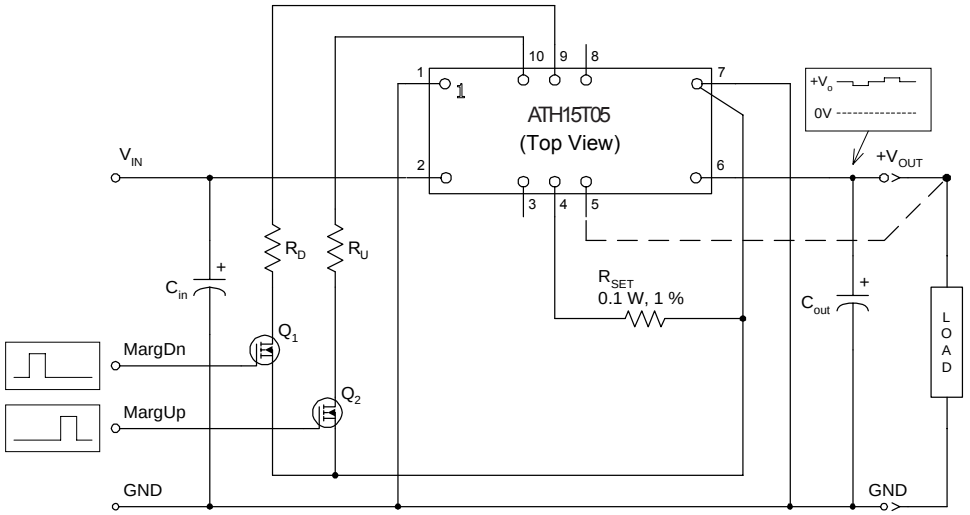
Notes:

1. The *Margin Up** and *Margin Dn** controls were not intended to be activated simultaneously. If they are their affects on the output voltage may not completely cancel, resulting in the possibility of a slightly higher error in the output voltage set point.
2. The ground reference should be a direct connection to the module *GND* at pin 7 (pin 1 for the ATH06). This will produce a more accurate adjustment at the load circuit terminals. The transistors Q_1 and Q_2 should be located close to the regulator.
3. The Margin Up and Margin Dn control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 µA when grounded, and has an open-circuit voltage of 0.8 V.

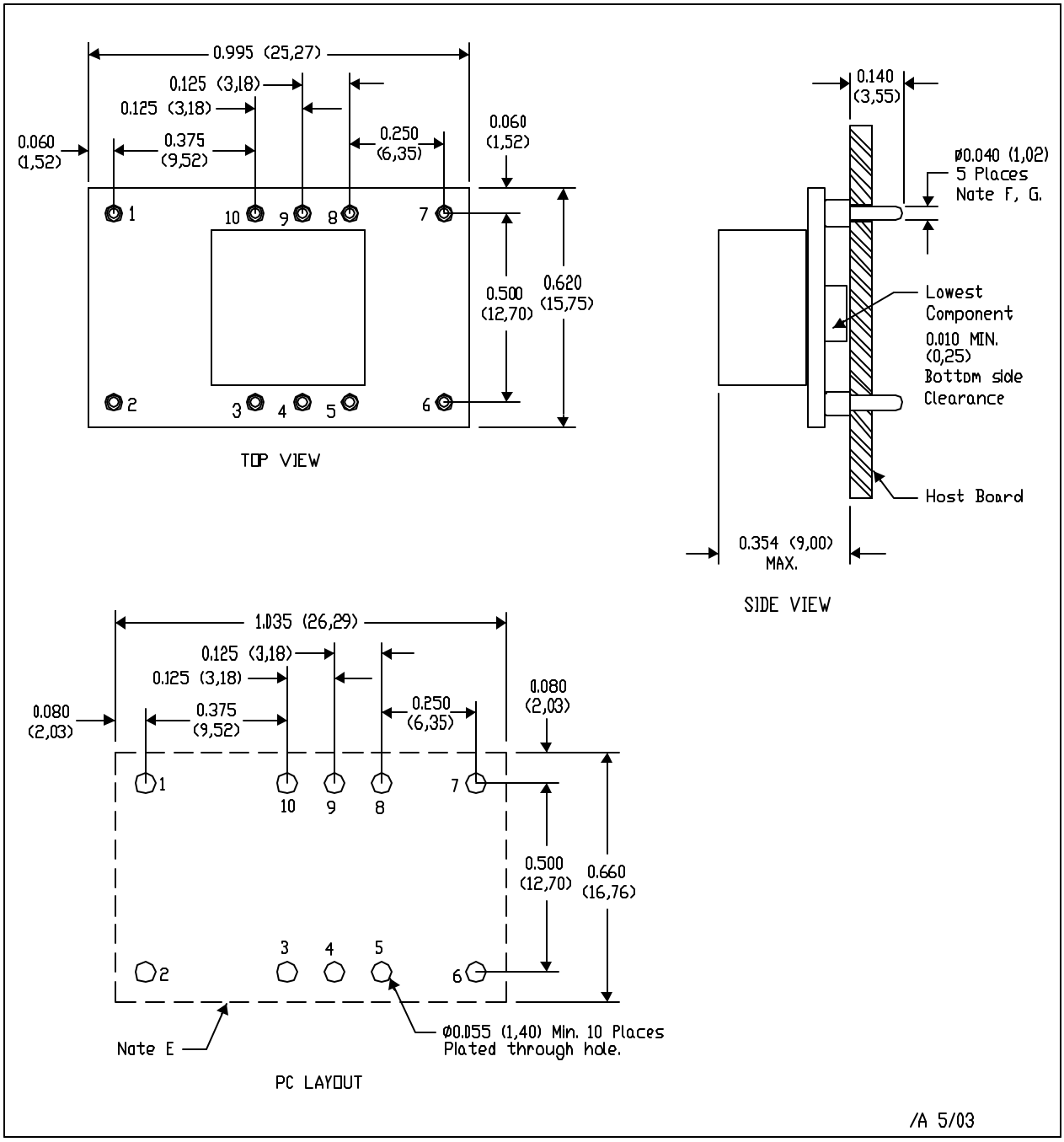
Table 3-2; Margin Up/Down Resistor Values

% Adjust	R_U / R_D
5	0.0 kΩ
4	24.9 kΩ
3	66.5 kΩ
2	150.0 kΩ
1	397.0 kΩ

Figure 3-7; Margin Up/Down Application Schematic

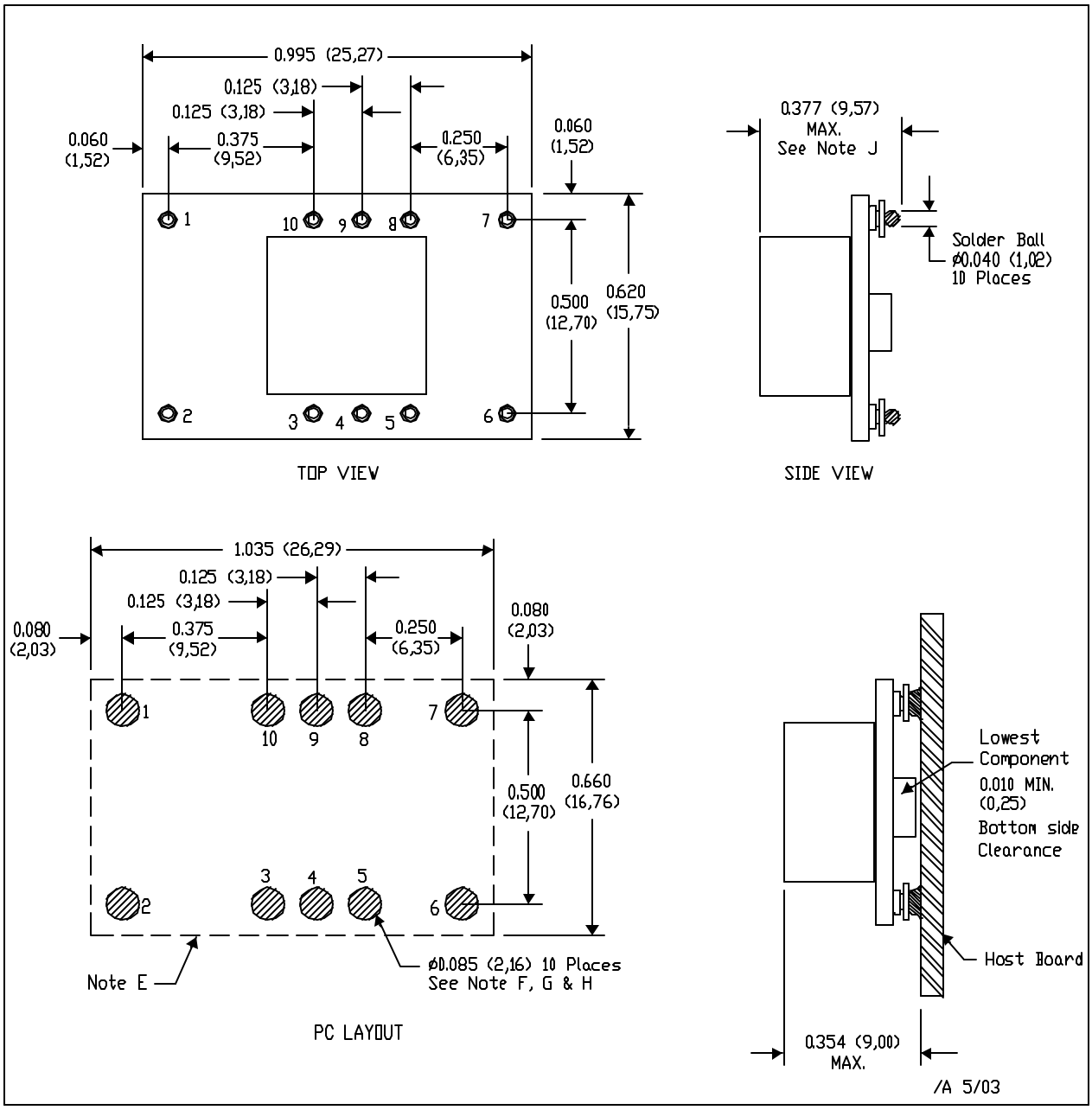


Through Hole Termination



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components
E. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
F. All pins: Material - Copper Alloy
Finish - Tin (100%) over Nickel plate

Surface Mount Termination



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.