

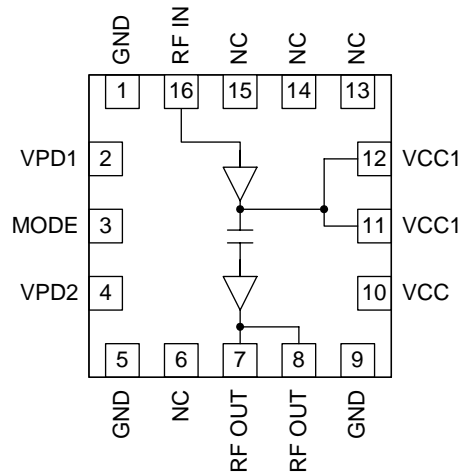


Features

- Single 3V Supply
- 29dBm Linear Output Power
- 35% Linear Efficiency
- Low Power Mode (Up to 20dBm)
- 55mA Idle Current

Applications

- 3V CDMA PCS Handsets
- 3V CDMA KPCS Handsets
- 3V TDMA/GAIT PCS Handsets
- 3V CDMA 2000 PCS Handsets
- Spread-Spectrum Systems
- Portable Battery-Powered Equipment



Functional Block Diagram

Product Description

The RF2196 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide process, and has been designed for use as the final RF amplifier in 3V CDMA and CDMA2000 handsets as well as other applications in the 1750MHz to 1910MHz band. The RF2196 has a low power mode to extend battery life under low output power conditions. The package is an ultra small 4 mmx4 mm, 16-pin QFN plastic package with back-side ground.

Ordering Information

RF2196 3V PCS Linear Power Amplifier
 RF2196PCBA-41X Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

- | | | | |
|--|--------------------------------------|-------------------------------------|-----------------------------------|
| <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS | <input type="checkbox"/> Si CMOS | |
| <input type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si BJT | |

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V _{DC}
Supply Voltage (P _{OUT} ≤31dBm)	+5.2	V _{DC}
Mode Voltage (V _{MODE})	+4.2	V _{DC}
Control Voltage (V _{REG})	+3.0	V _{DC}
Input RF Power	+10	dBm
Operating Case Temperature	-30 to +110	°C
Storage Temperature	-30 to +150	°C



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

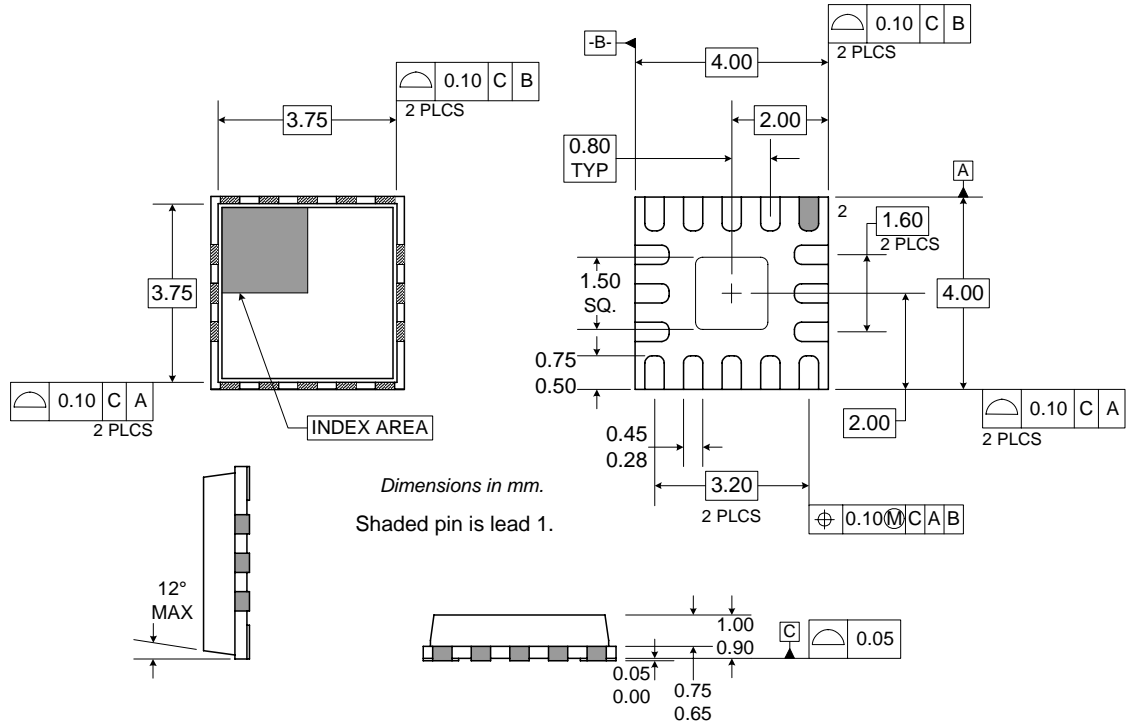
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power State (V _{MODE} Low)					Case T=25°C, V _{CC} =3.4V, V _{REG} =2.85V, V _{MODE} =0V to 0.5V, Freq=1850MHz to 1910MHz (unless otherwise specified)
Frequency Range	1850		1910	MHz	
Linear Gain	25	27		dB	
Second Harmonic		-50		dBc	
Third Harmonic		-63		dBc	
Maximum Linear Output Power (CDMA Modulation)	29			dBm	
Total Linear Efficiency		35		%	P _{OUT} =29dBm
Adjacent Channel Power Rejection		-46	-44	dBc	ACPR@1.25MHz
		-62	-56	dBc	ACPR@2.25MHz
Input VSWR		<2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc
Noise Power		-141		dBm/Hz	At 80MHz offset.
Low Power State (V _{MODE} High)					Case T=25°C, V _{CC} =3.4V, V _{REG} =2.85V, V _{MODE} =2V to 3V, Freq=1850MHz to 1910MHz (unless otherwise specified)
Frequency Range	1850		1910	MHz	
Linear Gain	16	20		dB	
Second Harmonic		-45		dBc	
Third Harmonic		-60		dBc	
Maximum Linear Output Power (CDMA Modulation)	16	20		dBm	
Max I _{CC}		160		mA	P _{OUT} =+16dBm (all currents included)
Adjacent Channel Power Rejection		<-50	-46	dBc	ACPR@1.25MHz
		<-60	-58	dBc	ACPR@2.25MHz
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc

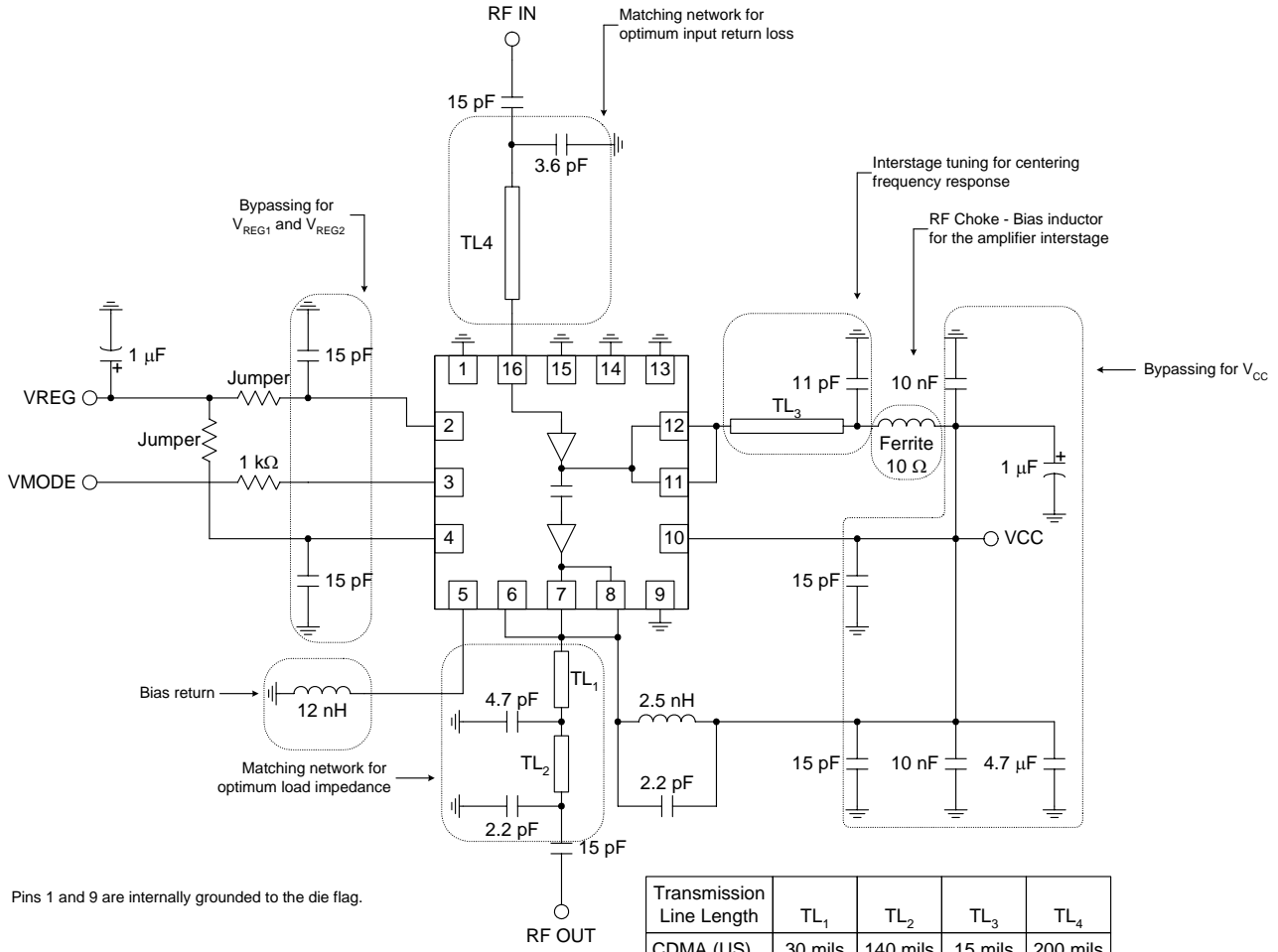
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power State CDMA 2000 1x (V_{MODE} LOW)					Case T=25 °C, V _{CC} =3.4V, V _{REG} =2.85V, V _{MODE} =0V to 0.5V, Freq=1850MHz to 1910MHz (unless otherwise specified)
Frequency Range	1850		1910	MHz	
Linear Gain		27		dB	
Pilot+DCCH 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	26.5			dBm	2.5 dB Backoff included in IS95D 5.4dB peak to average at CCDF of 1%
Adjacent Channel Power Rejection		-49		dBc	ACPR@1.25MHz
		-61		dBc	ACPR@2.25MHz
Pilot+ FCH 9600+SCHO 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	29			dBm	4.5 dB peak to average at CCDF of 1%
Adjacent Channel Power Rejection		-46		dBc	ACPR@1.25MHz
		-63		dBc	ACPR@2.25MHz
Low Power State CDMA 2000 1x (V_{MODE} HIGH)					Case T=25 °C, V _{CC} =3.4V, V _{REG} =2.85V, V _{MODE} =2V to 3V, Freq=1850MHz to 1910MHz
Frequency Range	1850		1910	MHz	
Linear Gain		19		dB	
Pilot+DCCH 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	16	20		dBm	5.4dB peak to average at CCDF of 1%
Adjacent Channel Power Rejection		-52		dBc	ACPR@1.25MHz
		-65		dBc	ACPR@2.25MHz
Pilot+ FCH 9600+SCHO 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	16	20		dBm	4.5 dB peak to average at CCDF of 1%
Adjacent Channel Power Rejection		-52		dBc	ACPR@1.25MHz
		-65		dBc	ACPR@2.25MHz
DC Supply					
Supply Voltage	3.0	3.4	4.2	V	
Quiescent Current		185		mA	V _{MODE} =Low
		55		mA	V _{MODE} =High
V _{REG} Current		5	10	mA	
V _{MODE} Current			1	mA	
Total Current (Power Down)			10	μA	V _{REG} =Low
V _{REG} "Low" Voltage	0		0.5	V	
V _{REG} "High" Voltage	2.75	2.85	2.95	V	
V _{MODE} "Low" Voltage	0		0.5	V	
V _{MODE} "High" Voltage	2.0		3.0	V	

Pin	Function	Description	Interface Schematic
1	GND	This pin is internally grounded to the die flag.	
2	VREG1	Power Down control for first stage. Regulated voltage supply for amplifier bias. In Power Down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
3	MODE	For nominal operation (High Gain Mode), V_{MODE} is set LOW. When set HIGH, the driver and final are dynamically scaled to reduce the device size and as a result to reduce idle current.	
4	VREG2	Power Down control for the second stage. Regulated voltage supply for amplifier bias. In Power Down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
5	GND	Connect to ground plane via 15 nH inductor. DC return for the second stage bias circuit.	
6	NC	This pin has no internal bonding; therefore, this pin can be connected to output pin 7, connected to the ground plane, or not connected. Slight tuning of the output match may be required due to stray capacitance of the pin.	
7	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the second stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1710MHz to 1910MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
8	RF OUT	Same as pin 7.	See pin 7.
9	GND	This pin is internally grounded to the die flag.	
10	VCC	Supply for bias reference and control circuits. High frequency bypassing may be necessary.	
11	VCC1	Power supply for first stage and interstage match. Pins 11 and 12 should be connected by a common trace where the pins contact the printed circuit board.	
12	VCC1	Same as pin 11.	
13	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
14	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
15	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
16	RF IN	RF input. An external 15 pF series capacitor is required as a DC block. In addition, the matching circuit shown is required to improve input VSWR.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

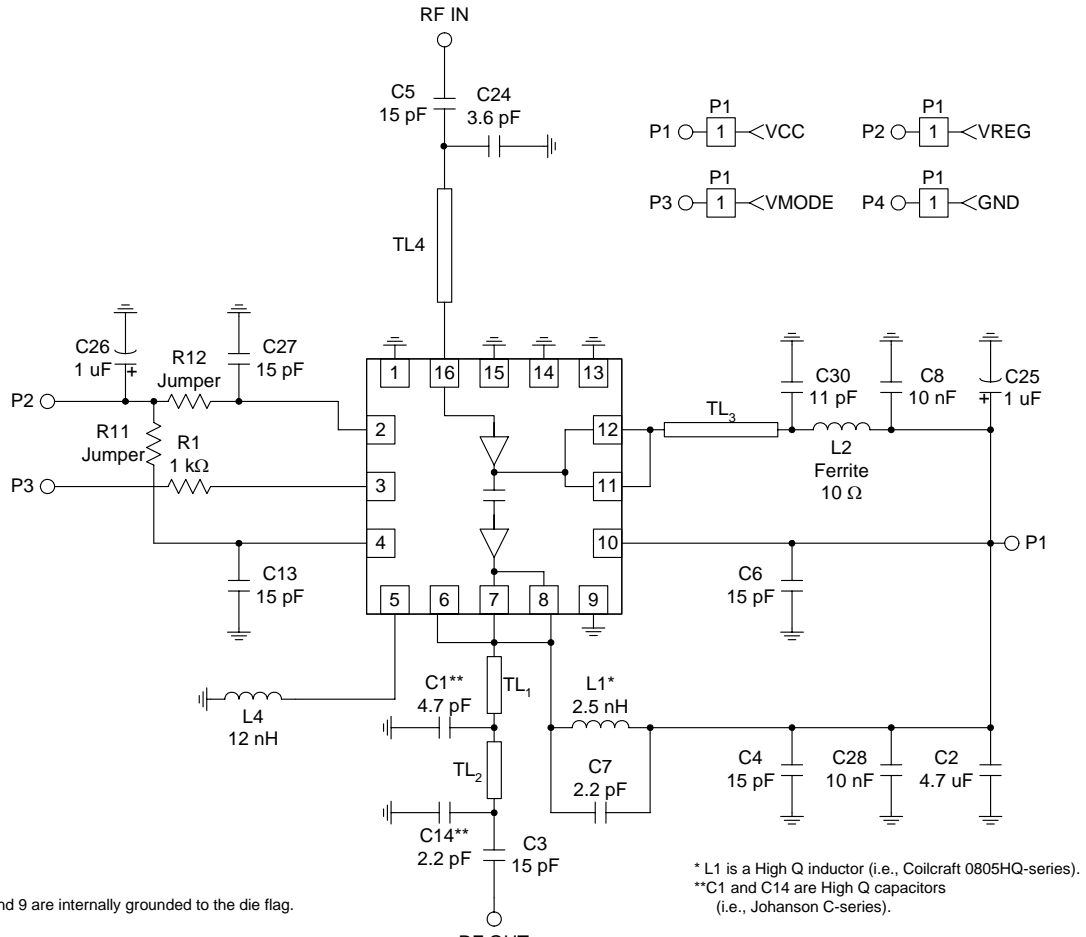
Package Drawing



Application Schematic US - CDMA



Evaluation Board Schematic
US - CDMA

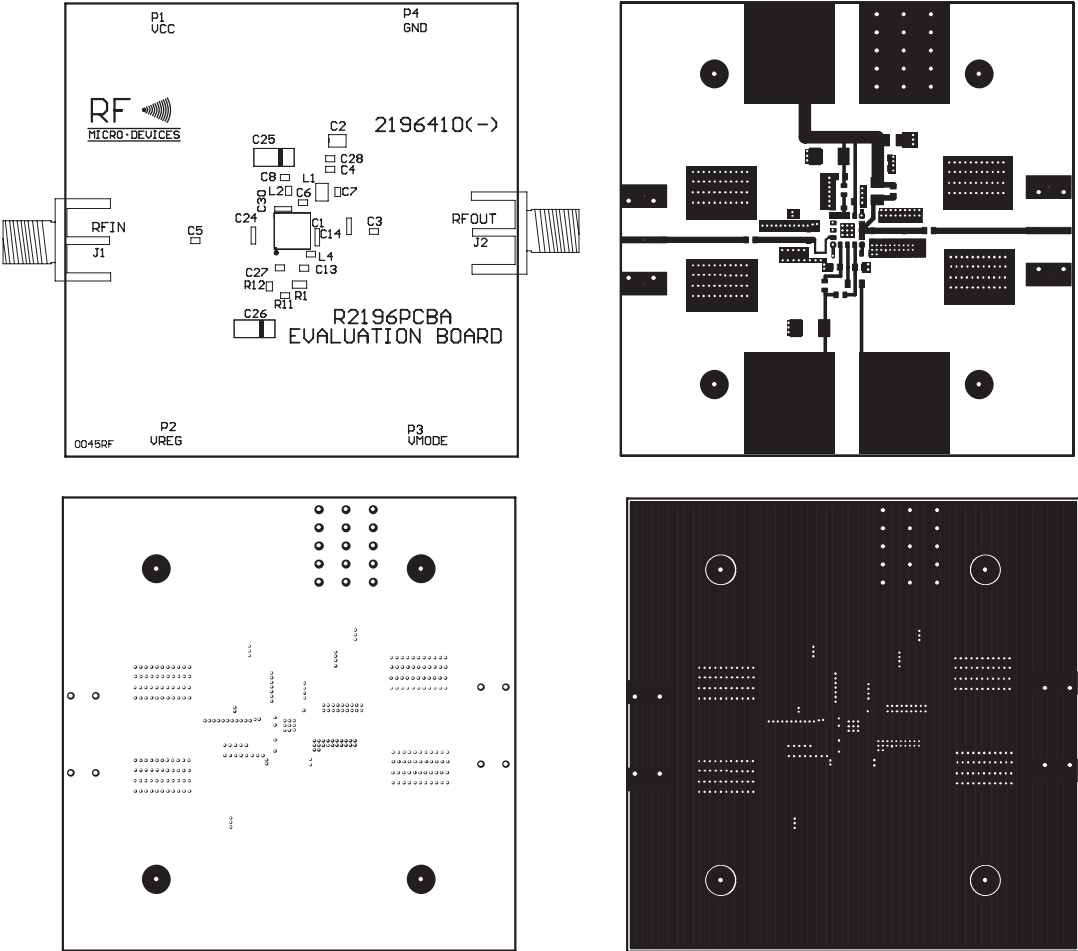


Board	C30 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (US)	11	4.7	2.5	2.2

Transmission Line Length	TL ₁	TL ₂	TL ₃	TL ₄
CDMA (US)	30 mils	140 mils	15 mils	200 mils

Evaluation Board Layout
Board Size 2.0" x 2.0"

Board Thickness 0.028"; Board Material FR-4; Multi-Layer; Ground Plane at 0.014"



PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

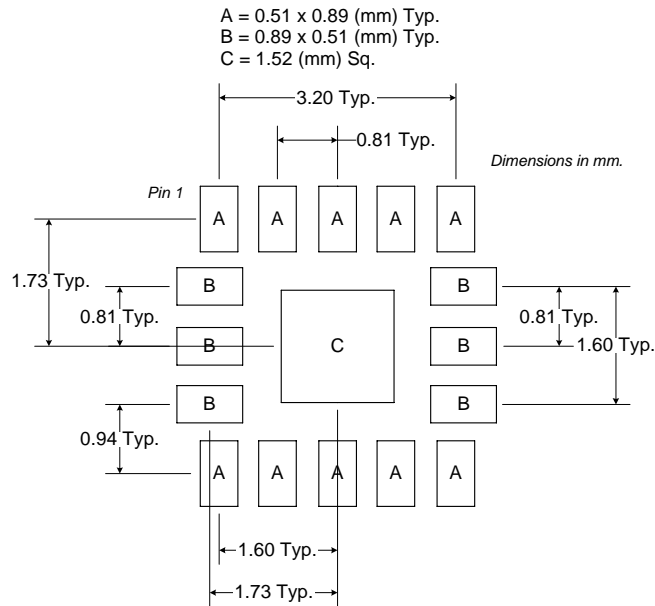


Figure 1. PCB Metal Land Pattern (Top View)

RoHS* Banned Material Content

RoHS Compliant: Yes
 Package total weight in grams (g): 0.038
 Compliance Date Code: 634
 Bill of Materials Revision: -
 Pb Free Category: e3

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Lead Frame	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted

* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

