Freescale Semiconductor
Advance Information

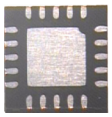
Document Number: MC34825
Rev 1.0, 8/2009

RoHS

Micro-USB Interface IC Supporting Universal Charging Solution and Wired Accessories

34825

INTERFACE IC



(PB-FREE)
98ASA00037D
20-PIN QFN

The 34825 is designed to support the Universal Charging Solution (UCS) recommended by the OMTP (Open Mobile Terminal Platform), as well as to use the same 5-pin micro or mini-USB connector for other wired accessories. The 34825 supports various types of external power supplies, such as a dedicated ac/dc adapter or a USB port, to charge the battery. It has functions built in to identify the type of the power supply, and sets low or high charging current, based on the current capability of the power supply. The 34825 monitors the power supply, and offers an up to 28 V of over-voltage protection (OVP) to the cell phone against failed power supplies. The 34825 also contains analog switches to multiplex the 5 pins, to support UART and high speed USB data communication, mono or stereo audio headset with or without a microphone and a cord remote controller, manufacturing or research-and-development (R/D) test cables, and other accessories.

The 34825 monitors both the VBUS status and the resistance between the ID pin and the ground to identify the accessory being plugged into the mini or micro-USB connector. A high-accuracy 5-bit ADC is offered to distinguish 32 levels of ID resistance that are assigned to buttons in a cord remote controller or to identification (ID) resistors of accessories. After identifying the attached accessory, the 34825 sends an interrupt signal to a host IC and the host IC can configure the analog switches via an I^2C serial bus for further actions. When the accessory is detached from the cell phone, an interrupt signal is also sent to inform the host.

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC34825EP/R2	-40°C to 85°C	3mm X 3mm UTQFN

Features

- Identifies various types of power supplies to set low or high battery-charging-current levels
- Internal power switch to offer OVP against up to 28 V failed power supply input
- Supports stereo/mono headset with or without microphone and remote controller with pure passive components
- Supports USB or UART R/D test cables
- High speed (480 Mbps) USB 2.0 compliant
- Supports 32 ID resistance values with a high accuracy 5-bit ADC
- Accessory attachment and detachment detection with an interrupt signal to the host IC
- I^2C interface
- 10 µA quiescent current in Standby mode
- Pb-free packaging designated by suffix code EP

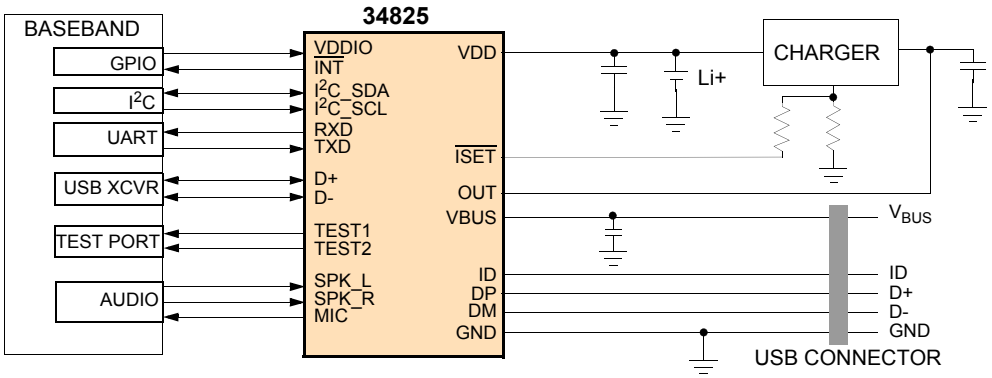


Figure 1. 34825 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale semiconductor

INTERNAL BLOCK DIAGRAM

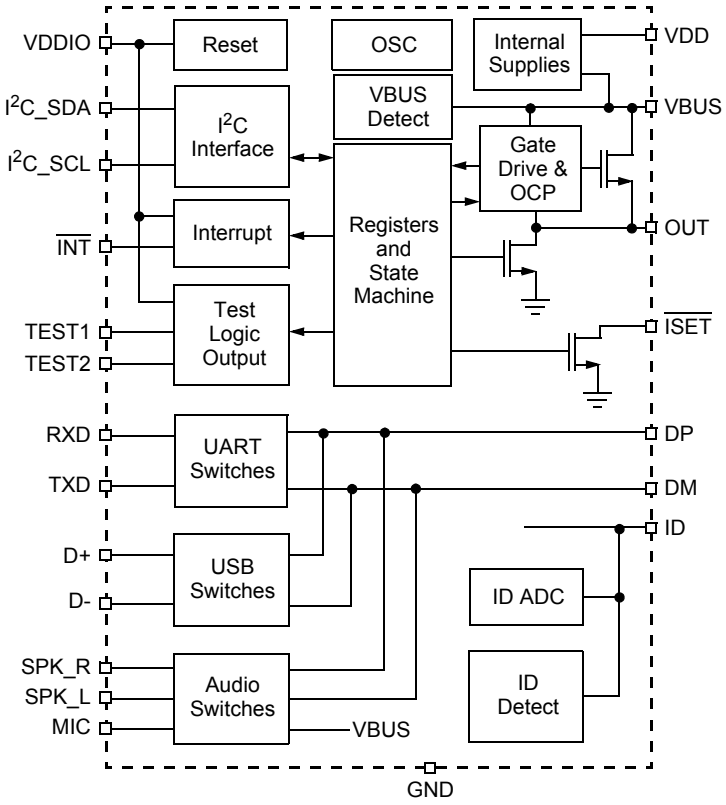


Figure 2. 34825 Simplified Internal Block Diagram

PIN CONNECTIONS

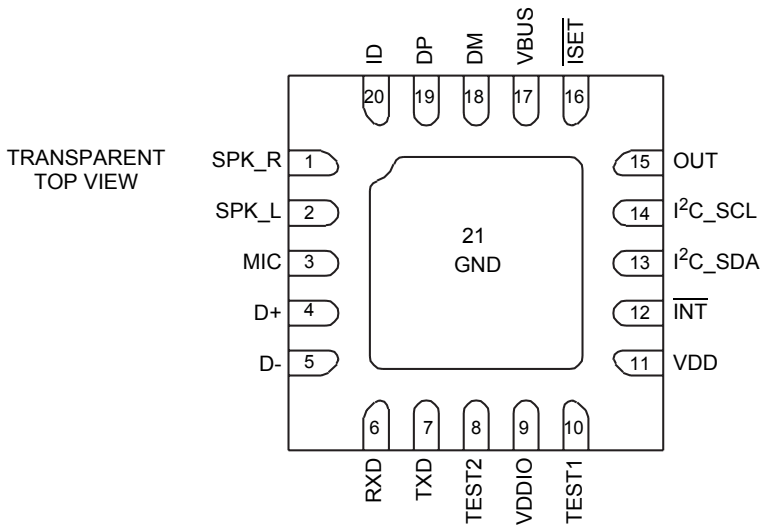


Figure 3. 34825 Pin Connections

Table 1. 34825 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section on page 13.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	SPK_R	Input	Speaker right channel	Right channel input for speaker signals
2	SPK_L	Input	Speaker left channel	Left channel input for speaker signals
3	MIC	Output	Microphone output	Microphone output to the baseband of the cell phone system
4	D+	IO	D+ of the USB transceiver	D+ line of the USB transceiver
5	D-	IO	D- of the USB transceiver	D- line of the USB transceiver
6	RXD	Output	UART receiver	Receive line of the UART
7	TXD	Input	UART transmitter	Transmit line of the UART
8	TEST2	Output	TEST cable type indicator	Push-pull output to indicate the type of the test cable. This pin is internally pulled up to the VDDIO voltage.
9	VDDIO	Input	IO power supply	IO supply voltage. The VDDIO voltage is used as the reference voltage for the I^2C bus signals and the pull-up voltage for the TEST2 output. This pin also functions as a hardware reset to the IC.
10	TEST1	Output	TEST cable indicator	Open-drain output to indicate the connection of a test cable
11	VDD	Input	Power supply	IC power supply input
12	$\overline{\text{INT}}$	Output	Interrupt output	Open-drain interrupt output
13	I^2C_SDA	IO	I^2C data	Data line of the I^2C interface
14	I^2C_SCL	Input	I^2C clock	Clock line of the I^2C interface
15	OUT	Output	Power output	The output of the power MOSFET pass switch
16	$\overline{\text{ISET}}$	Output	Charge current setting	Open-drain output to set the charger current
17	VBUS	Input	VBUS power supply	VBUS line of the Mini or micro-USB connector

Table 1. 34825 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section on page 13.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
18	DM	IO	D- of the USB connector	D- line of the mini or micro-USB connector
19	DP	IO	D+ of the USB connector	D+ line of the mini or micro-USB connector
20	ID	Input	ID of the USB connector	ID pin of the mini or micro-USB connector
21	GND	Ground	Ground	Ground

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Input Voltage Range			V
VBUS Pin	V_{BUS}	-0.3 to 28	
OUT Pin	V_{OUT}	-0.3 to 8.0	
SPK_L, SPK_R, DP, and DM Pins		-2.0 to V_{DD}+0.3	
All Other Pins		-0.3 to 5.5	
ESD Voltage (1)	V_{ESD}		V
Human Body Model (HBM) for VBUS, DP, DM, ID Pins		±8000	
Human Body Model (HBM) for all other pins		±2000	
Machine Model (MM)		±200	
THERMAL RATINGS			
Operating Temperature			°C
Ambient	T_A	-40 to +85	
Junction	T_J	150	
Storage Temperature	T_{STG}	-65 to +150	°C
Thermal Resistance (2)			°C/W
Junction-to-Case	$R_{\theta JC}$	6.0	
Junction-to-Ambient	$R_{\theta JA}$	45	
Peak Package Reflow Temperature During Reflow (3), (4)	T_{PPRT}	Note 4	°C

Notes

1. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
2. Device mounted on the Freescale EVB test board per JEDEC DESD51-2.
3. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx)], and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions V_{DD} = 3.6 V, V_{BUS} = 5.0 V, V_{DDIO} = 3.0 V, -40°C ≤ T_A ≤ 85°C (see Figure 1), unless otherwise noted. Typical values noted reflect the approximate parameter means at V_{DD} = 3.6 V and T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
VDD Supply Voltage	V_{DD}	2.7	-	5.5	V
VDD Power-On-Reset Threshold	V_{VDDPOR}				
Rising edge		-	2.5	2.65	V
Hysteresis		-	100	-	mV
VDD Quiescent Current	I_{VDD}				µA
In Standby mode		-	9.0	12	
In Power Save mode		-	16	22	
In Active mode (V_{DD} < V_{BUS})		-	550	650	
In Active mode (V_{DD} > V_{BUS})		-	850	1000	
VBUS Supply Voltage	V_{BUS}	2.8	5.0	28	V
VBUS Detection Threshold Voltage	V_{BUS_DET}				
Rising edge		-	2.65	2.80	V
Hysteresis		-	150	-	mV
VBUS Supply Quiescent Current	I_{VBUS}				
In VBUS Power mode		-	-	1.2	mA
In Active mode - Dedicated Charger		-	-	1.2	mA
In Active mode - power MOSFET is off (V_{BUS} < V_{DD})		-	-	0.5	µA
VBUS Over-voltage Protection Threshold	V_{BUS_OVP}				
Rising edge		6.8	7.0	7.2	V
Hysteresis		-	150	-	mV
VBUS Over-current Protection Threshold	I_{BUS_OCP}				
Triggering threshold (at onset of OTP shutoff)		1.2	1.8	2.2	A
Over-temperature Protection Threshold	T_{OTP}				°C
Rising threshold		115	130	145	
Falling threshold		-	95	-	
VDDIO Supply Voltage	V_{DDIO}	1.65	-	3.6	V
SWITCH					
$\overline{ISET}$ Open-Drain Output MOSFET					
On resistance (loaded by 3.0 mA current)	R_{ISETB}	-	-	100	Ω
Leakage current (when the MOSFET is off at 5.0 V bias voltage)	I_{ISET_OFF}	-	-	0.5	µA
OUT Pin Discharge MOSFET(1)					
On resistance (loaded by 3.0 mA current)	R_{OUT_DISC}	-	-	100	Ω
Leakage current (when the MOSFET is off at 5.0 V bias voltage)	I_{OUT_OFF}	-	0.5	-	µA
Power MOSFET	R_{PSW}				mΩ
On resistance (when V_{BUS} = 5.0 V, T_A< 50°C)		-	200	250	

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{DD} = 3.6 V, V_{BUS} = 5.0 V, V_{DDIO} = 3.0 V, -40°C ≤ T_A ≤ 85°C (see Figure 1), unless otherwise noted. Typical values noted reflect the approximate parameter means at V_{DD} = 3.6 V and T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPK_L and SPK_R Switches					Ω
On resistance (20 Hz to 470 kHz)	R_{SPK_ON}	-	1.6	3.0	
Matching between channels	R_{SPK_ONMCT}	-	0.05	0.15	
On resistance flatness (from -1.2 to 1.2 V)	R_{SPK_ONFLT}	-	0.01	0.05	
D+ and D- Switches					Ω
On resistance (0.1 Hz to 240 MHz)	R_{USB_ON}	-	-	5.0	
Matching between channels	R_{USB_ONMCT}	-	0.1	0.5	
On resistance flatness (from 0.0 to 3.3 V)	R_{USB_ONFLT}	-	0.02	0.1	
RXD and TXD Switches					Ω
On resistance	R_{UART_ON}	-	-	60	
On resistance flatness (from 0.0 to 3.3V)	R_{UART_ONFLT}	-	-	5.0	
MIC Switch					Ω
On resistance (at below 2.5 V MIC bias voltage)	R_{MIC_ON}	-	-	100	
On resistance flatness (from 1.8 to 2.3 V)	R_{MIC_ONFLT}	-	-	5.0	
Pull-down Resistors between SPK_L or SPK_R Pins to GND	R_{PD_AUDIO}	-	100	-	kΩ
Signal Voltage Range					V
SPK_L, SPK_R,		-1.5	-	1.5	
D+, D-, RXD, TXD, MIC		-0.3	-	3.6	
PSRR - From VDD (100 mVrms) to DP/DM Pins[4]	V_{A_PSRR}				dB
20 Hz to 20 kHz with 32/16 Ω load.		-	-	-60	
Total Harmonic Distortion[4]	THD				%
20 Hz to 20 kHz with 32/16 Ω load.		-	-	0.05	
Crosstalk between Two Channels	V_{A_CT}				dB
less than 1.0MHz		-	-60	-	
Off-Channel Isolation	V_{A_ISO}				dB
Less than 1.0 MHz		-	-80	-	
POWER SUPPLY TYPE IDENTIFICATION					
Data Source Voltage	V_{DAT_SRC}				V
Loaded by 0~200 µA		0.5	0.6	0.7	
Data Source Current	I_{DAT_SRC}	0	-	200	µA
Data Detect Voltage	V_{DAT_REF}				V
Low threshold		0.3	0.35	0.4	
High threshold		0.8	0.9	1.0	
Data Sink Current	I_{DAT_SINK}				µA
DM pin is biased between 0.15 to 3.6 V		65	100	135	
DP, DM Pin Capacitance	$C_{DP/DM}$	-	8	-	pF
DP, DM Pin Impedance	$R_{DP/DM}$				MΩ
All switches are off		-	50	-	

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions V_{DD} = 3.6 V, V_{BUS} = 5.0 V, V_{DDIO} = 3.0 V, -40°C ≤ T_A ≤ 85°C (see Figure 1), unless otherwise noted. Typical values noted reflect the approximate parameter means at V_{DD} = 3.6 V and T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ID DETECTION					
ID_Float Threshold	V_{FLOAT}				V
Detection threshold		-	2.3	-	
Pull-up Current Source	I_{ID}				µA
When ADC result is 1xxxx		1.9	2.0	2.1	
When ADC result is 0xxxx		30.4	32	33.6	
ID Shorted to Ground Detection					
Detection current	I_{VCBL}	1.0	1.2	1.4	mA
Detection voltage threshold	V_{VCBL_L}	-	50	-	mV
LOGIC INPUT AND OUTPUT					
VDDIO Logic Input Level					
Input LOW level	V_{DDIO_IL}	-	-	0.5	V
Input HIGH level	V_{DDIO_IH}	1.5	-	-	V
Push-pull Logic Output (TEST2)					V
Output HIGH level (loaded by 1.0 mA current)	V_{OH}	$0.7V_{DDIO}$	-	-	
Output LOW level (loaded by 4.0 mA current)	V_{OL}	-	-	0.4	
Open-Drain Logic Output (TEST1, $\overline{INT}$)	V_{ODOL}				V
Output LOW level (loaded by 4.0 mA current)		-	-	0.4	
I^2C INTERFACE(4)					
Low Voltage on I^2C_SDA, I^2C_SCL Inputs	V_{I2C_IL}	-0.2	-	$0.3V_{DDIO}$	V
High Voltage on I^2C_SDA, I^2C_SCL Inputs	V_{I2C_IH}	$0.7V_{DDIO}$	-	V_{DDIO}	V
Low Voltage on I^2C_SDA Output	V_{I2C_OL}	-	-	0.4	V
Current Load when I^2C_SDA Outputs Low Voltage	I_{I2C_OL}	0	-	4.0	mA
Leakage Current on I^2C_SDA, I^2C_SCL Outputs	I_{I2C_LEAK}	-1.0	-	1.0	µA
Input Capacitance of the I^2C_SDA, I^2C_SCL Pins	C_{I2CIN}	-	-	8.0	pF

Notes

1. The OUT pin discharge MOSFET is shown in Figure 15. This MOSFET will be turned on when the power MOSFET is off.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions V_{DD} = 3.6 V, V_{BUS} = 5.0 V, V_{DDIO} = 3.0 V, -40°C ≤ T_A ≤ 85°C (see Figure 1), unless otherwise noted. Typical values noted reflect the approximate parameter means at V_{DD} = 3.6 V and T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER ON AND OFF DELAY					
VDD Power-On-Reset Timing					ms
VDD rising deglitch time	t_{D2}	7.0	8.5	10.2	
VDD falling deglitch time	t_{VDDDGT_F}	1.7	2.5	3.5	
VBUS Detection Deglitch Time (for Both Rising and Falling Edges)(4)	t_{VBUS_DET}	3.5	4.5	5.7	ms
VBUS Over-voltage Protection					µs
Protection delay(2)(4)	t_{OVPD}	-	-	2.0	
Falling-edge deglitch time(3)	t_{OVPDGT_F}	-	25	-	
VBUS Over-temperature Protection					
MOSFET turning off speed when OTP occurs(4)	t_{OTP_TO}	-	-	0.5	A/µs
Deglitch time	t_{OTP_DGT}	-	15	-	µs
OSCILLATOR					
Oscillation Frequency	f_{OSC}	85	100	112	kHz
SWITCHING DELAY					
ID Detection Delay Time after VBUS Applied (Default Value is TD = 0100)	t_D				ms
TD = 0000		-	100	-	
TD = 0001		-	200	-	
TD = 0010		-	300	-	
TD = 0011		-	400	-	
TD = 0100		-	500	-	
.....		.....	.....	.....	
TD = 1111		-	1600	-	
ID DETECTION					
ID Float Detection Deglitch Time	t_{ID_FLOAT}	-	20	-	ms
ID Shorted to Ground Detection Time (The Detection Current Source On Time)	t_{VCBL}	-	20	-	ms
ADC					
ADC Conversion Time	t_{CONV}	-	1.0	-	ms
REMOTE CONTROL					
Key Press Comparator Debounce Time	t_{RMTCON_DG}	-	20	-	ms
RESET TIMING					
Device Reset Time	t_{RSTDVC}	-	10	-	µs
VDDIO Logic Input Timing					µs
Rising edge deglitch time	$t_{VDDIODGT\_R}$	660	875	1130	
Falling edge deglitch time	$t_{VDDIODGT\_F}$	105	125	150	
VDDIO Reset Timing					µs
VDDIO reset pulse width	$t_{RSTVDDIO}$	150	-	-	

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions V_{DD} = 3.6 V, V_{BUS} = 5.0 V, V_{DDIO} = 3.0 V, -40°C ≤ T_A ≤ 85°C (see Figure 1), unless otherwise noted. Typical values noted reflect the approximate parameter means at V_{DD} = 3.6 V and T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
I^2C Reset Timing					ms
I^2C reset pulse width	t_{RSTI2C}	13.5	-	-	
I^2C_SDA/I^2C_SCL concurrent low time without causing a reset	$t_{NRSTI2C}$	-	-	8.8	
I^2C INTERFACE(4)					
SCL Clock Frequency	f_{SCL}	-	-	400	kHz
Bus Free Time between a STOP and START Condition	t_{BUF}	1.3	-	-	µs
Hold Time Repeated START Condition	$t_{HD:STA}$	0.6	-	-	µs
Low Period of SCL Clock	t_{LOW}	1.3	-	-	µs
High Period of SCL Clock	t_{HIGH}	0.6	-	-	µs
Setup Time for a Repeated START condition	$t_{SU:STA}$	0.6	-	-	µs
Data Hold Time	$t_{HD:DAT}$	0	-	-	µs
Data Setup Time	$t_{SU:DAT}$	100	-	-	ns
Rising Time of Both SDA and SCL Signals	t_R	20+0.1C_B	-	-	ns
Falling Time of Both SDA and SCL Signals	t_F	20+0.1C_B	-	-	ns
Setup Time for STOP Condition	$t_{SU:STO}$	0.6	-	-	µs
Input Deglitch Time (for Both Rising and Falling Edges)	t_{DGT}	55	-	300	ns

Notes

2. The protection delay is defined as the interval between VBUS voltage rising above the OVP rising threshold, and the OUT pin voltage dropping below the OVP rising threshold voltage for a VBUS ramp rate of >1.0 V/µs.
3. The OVP deglitch timer is only for the falling edge threshold.
4. These parameters are not tested. They are guaranteed by design.

ELECTRICAL PERFORMANCE CURVES

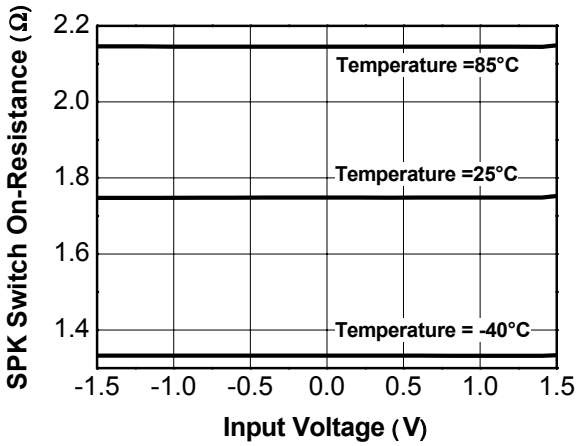


Figure 4. SPK Switch On Resistance vs Input Voltage

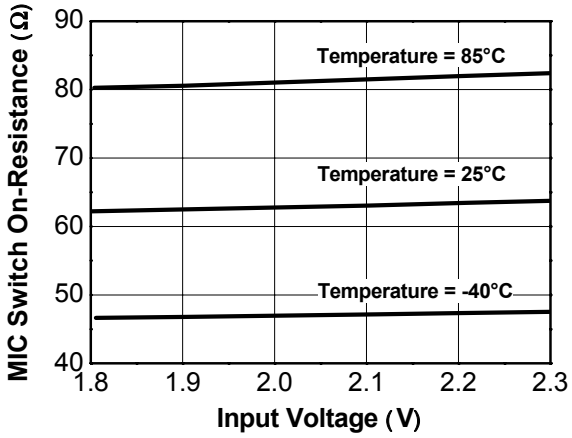


Figure 7. MIC Switch On Resistance vs Input Voltage

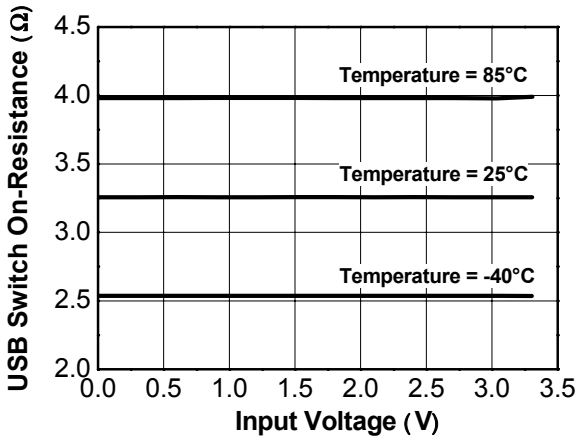


Figure 5. USB Switch On Resistance vs Input Voltage

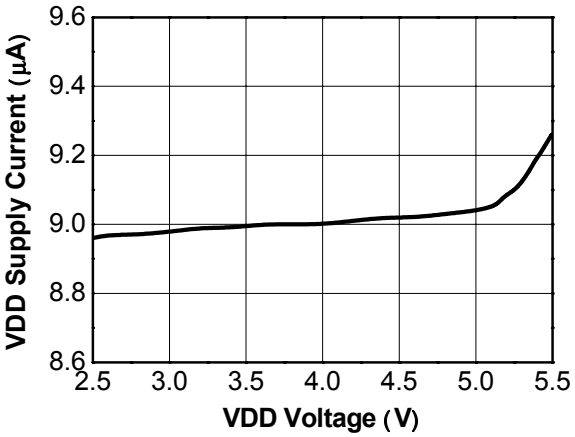


Figure 8. VDD Supply Current vs Supply Voltage in Standby Mode

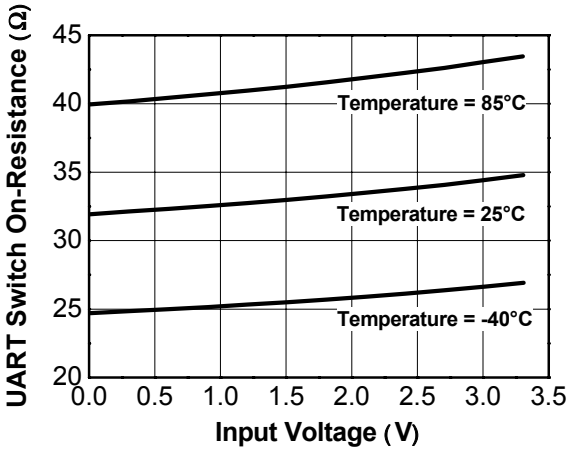


Figure 6. UART Switch On Resistance vs Input Voltage

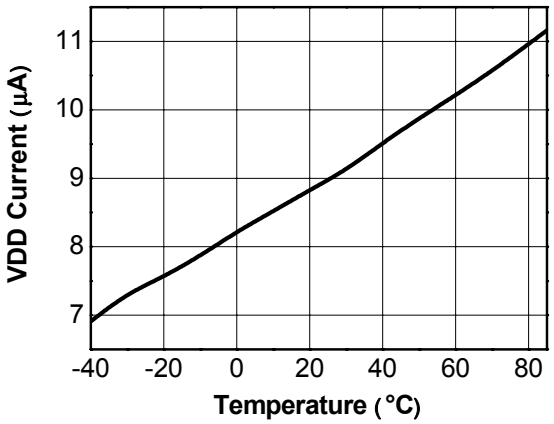


Figure 9. VDD Supply Current vs Temperature In Standby Mode

34825

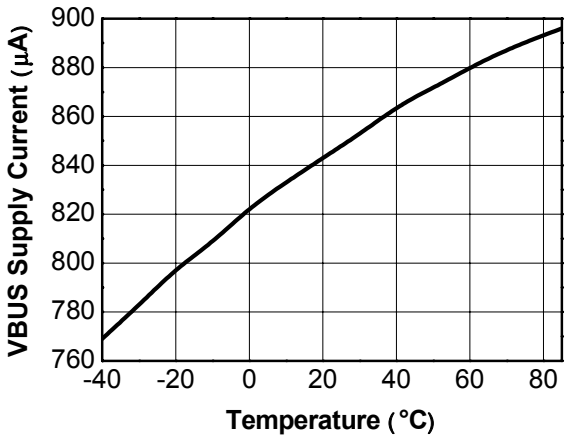


Figure 10. VBUS Supply Current vs Temperature In VBUS Power Mode

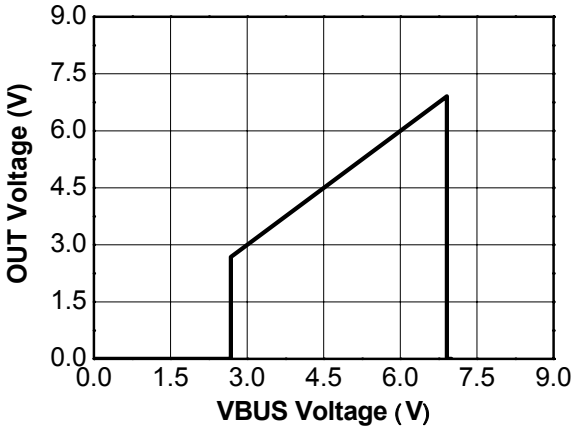


Figure 11. OUT Voltage vs VBUS Voltage

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 34825 is designed to support cell phones that adopt the micro or mini-USB connector as the sole wired interface between the cell phone and external accessories. Using the micro-USB connector for charging and USB data communication is required by the OMTP standard for the UCS. The 34825 further extends the micro-USB connector to support other accessories to eliminate all other mechanical connectors in a cell phone. The supported accessories include various audio headsets, UART connection, R/D test cables for firmware downloading, and other user defined accessories, in addition to the chargers defined in the *Battery Charging Specification, Revision 1.0,* from the USB Implementer's Forum and the *CEA-936-A USB Carkit Specification,* from the Consumer Electronics Association (CEA). The supported chargers are listed in Table 7.

The 34825 offers two mechanisms to assist the identification of the accessory. The ID detection mechanism allows the cell phone to measure the ID resistor value between the ID pin and the ground with a 5-bit ADC. The VBUS detection mechanism allows the cell phone to find out the connection status between the D+ and D- pins. Together, the exact accessory can be determined. A detection flow is initiated by a change in the VBUS pin voltage or by a change in the ID pin floating status. Detaching the accessory from the micro or mini-USB connector causes the VBUS voltage or/ and the ID resistance to change. The identification flow will be initiated to confirm if an accessory is still connected. The host can also initiate the identification flow by resetting an ACTIVE bit in the register from 1 to 0.

Upon the completion of the identification flow, an interrupt signal is sent to the host IC, so the host IC can take further actions. The 34825 contains switches that the host IC can control via an I^2C interface. Based on the accessory, the host IC can configure the switch connections in the 34825, so that the signal paths for the USB communication, or the UART communication, or audio accessories can be established between the micro or mini-USB connector pins and the system ICs. If the accessory is a power supply, the supplied voltage is switched to the Li-ion battery charging function in the cell phone via an internal power MOSFET.

The host IC controls the 34825 via the I^2C serial bus. The register map in the 34825 contains status information of the device and the control bits that the host IC can access to control the 34825.

FUNCTIONAL PIN DESCRIPTION

SPEAKER RIGHT CHANNEL (SPK_R)

Right channel of the baseband speaker output.

SPEAKER LEFT CHANNEL (SPK_L)

Left channel of the baseband speaker output.

MICROPHONE OUTPUT (MIC)

Microphone output to the baseband.

D+ OF THE USB TRANSCEIVER (D+)

D+ line of the USB transceiver.

D- OF THE USB TRANSCEIVER (D-)

D- line of the USB transceiver.

UART RECEIVER (RXD)

Receiver line of the UART.

UART TRANSMITTER (TXD)

Transmitter line of the UART.

TEST2 INDICATOR (TEST2)

Push-pull output to indicate the type of the connected test cable.

IO POWER SUPPLY (VDDIO)

Power supply input for the logic IO interface. Generally the IO power supply voltage should be the same as the IO voltage used in the cell phone system. VDDIO is also one of the hardware reset input sources. A falling edge at this pin will reset the 34825. See Reset for more information.

TEST1 INDICATOR (TEST1)

Open-drain output to indicate the attachment of a test cable.

POWER SUPPLY (VDD)

Power supply input. Bypass to ground with a 1.0 μF capacitor.

INTERRUPT OUTPUT ($\overline{\text{INT}}$)

Active low open-drain output. The $\overline{\text{INT}}$ pin sends an interrupt signal to the host IC when an interrupt event happens. The $\overline{\text{INT}}$ output returns to high voltage once all interrupt bits are read.

DATA LINE OF THE I^2C INTERFACE (I^2C_SDA)

Data line of the I^2C interface.

I^2C CLOCK (I^2C_SCL)

Clock line of the I^2C interface. The I^2C_SCL input together with the I^2C_SDA input forms one of the hardware reset input sources.

POWER OUTPUT (OUT)

Output of the power MOSFET in the 34825. This pin is connected to a charger input. Bypass to ground with a 1.0 μF capacitor.

CHARGE CURRENT SETTING ($\overline{\text{ISET}}$)

Open-drain output to set the charge current according to the power supply current capability.

VBUS POWER SUPPLY (VBUS)

USB VBUS input. Bypass this pin to ground with a less than 10 nF capacitor. When the accessory is an audio kit, this pin is the microphone input to the 34825.

D- OF THE USB CONNECTOR (DM)

D- line of the mini or micro-USB connector.

D+ OF THE USB CONNECTOR (DP)

D+ line of the mini or micro-USB connector.

ID OF THE USB CONNECTOR (ID)

ID pin of the mini or micro-USB connector.

GROUND (GND)

Ground.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

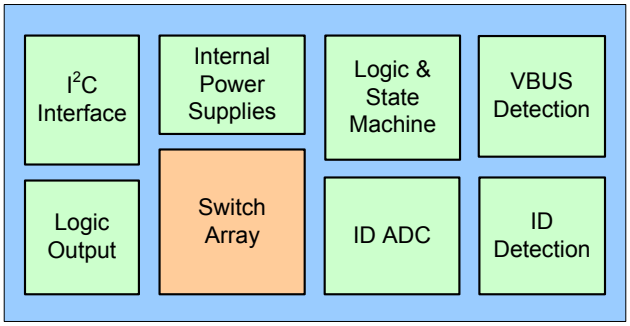


Figure 12. 34825 Functional Internal Block Diagram

INTERNAL POWER SUPPLIES

This block contains the bias power supplies to the internal circuits. The inputs to this block include VBUS, VDD and VDDIO.

LOGIC AND STATE MACHINE

This block includes the state machine for accessory detection and identification, the register map, and other logic circuits.

I^2C INTERFACE

The I^2C interface block has the circuit for the I^2C communication that a master device can use to access the registers in the 34825. The 34825 is a slave device.

LOGIC OUTPUT

The logic output includes open-drain or push-pull drivers for the four logic output signals, TEST1, TEST2, $\overline{INT}$, and $\overline{ISET}$.

SWITCH ARRAY

The switch array consists of analog switches for UART, USB, audio signal switching and one high-voltage power MOSFET for power switching.

VBUS DETECTION

This block detects whether the power supply at VBUS pin is present or removed.

ID DETECTION

This block contains a circuit to detect whether an ID resistor is connected to the ID pin or not.

ID ADC

An internal 5-bit ADC measures the resistance at the ID pin. The result is stored in the ADC Result register and sent to the Logic and State Machine block to determine what accessory is attached.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

The 34825 has five operational modes: Power Down mode, VBUS Power mode, Standby mode, Active mode, and Power Save mode. The mode transition diagram is given in Figure 13.

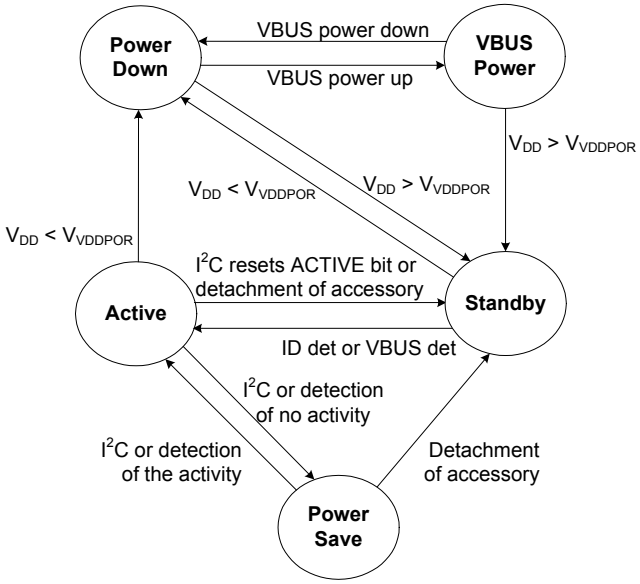


Figure 13. Mode Transition Diagram

POWER DOWN MODE

The Power Down mode is when neither the VDD pin nor the VBUS pin is powered. In this mode, the IC does not respond to any accessory attachment except for a power supply. When an external power supply is plugged into the mini or micro-USB connector, the 34825 enters the VBUS Power mode.

VBUS POWER MODE

The 34825 enters the VBUS Power mode when the VBUS pin is powered but the VDD pin is not. In the VBUS Power mode, the internal power MOSFET is turned on to power the charging function in the cell phone. The $\overline{\text{ISET}}$ pin outputs high-impedance in this mode.

STANDBY MODE

The Standby mode is when the VDD voltage is higher than the POR (Power-On-Reset) threshold and no accessory is attached. In this mode, only the ID detection circuit, the I^2C interface, and the internal registers are powered in order to minimize the quiescent current from the VDD pin. The ID detection circuit samples the status of the ID line every 50 ms.

If detecting an attachment of an accessory, the 34825 moves to the Active mode for further accessory identification.

ACTIVE MODE

The Active mode starts when an accessory is plugged into the mini or micro-USB connector while the VDD pin is powered. The 34825 identifies the accessory and interrupts the host IC for further actions. Different functions will be enabled according to the identification result, so the quiescent current in Active mode is dependent on the type of accessories.

The operational mode can be changed from Active to Standby either by an accessory detachment or by resetting the ACTIVE bit to 0 through an I^2C programming operation.

POWER SAVE MODE

The Power Save mode can be enabled only for accessories with a remote controller (refer to Table 21). The 34825 enters into the Power Save mode to minimize the operating current while such an accessory is attached, but not in operation. For example, if the cell phone is not in an audio playback mode when a headset is attached, the host IC can force the 34825 to the Power Save mode via the I^2C programming. The 34825 can also automatically enter into the Power Save mode when no activity is detected on the SPK_R or SPK_L pins in 10 seconds. The VDD current in the Power Save mode is slightly higher than the current in the Standby mode.

The 34825 can exit the Power Save mode by an I^2C programming or will exit the mode automatically when

detecting audio signal activities or an accessory detachment. If the transition is caused by an accessory detachment, the 34825 moves from the Power Save mode to the Standby mode directly. Otherwise, it moves to the Active mode, and the configuration of the IC resumes to the same configuration before entering the Power Save mode.

DEVICE MODE REGISTER

The PSAVE bit, ACTIVE bit and RST bit in the Device Mode register (refer to Table 9) hold the information of the device operational mode. The RST bit, which is of R/C (read and clear) type, indicates whether a reset has occurred. The RST bit is set when a reset occurs (refer to Reset for more information). The RST bit is cleared when read by an I^2C access. The ACTIVE bit and the PSAVE bit together indicate the device mode by the relationship shown in Table 5. When the device is in the VBUS Power mode, the registers are not powered up.

The ACTIVE bit is a R/W (read and write) bit, it can be written by an I^2C operation. When the host IC writes '0' to the ACTIVE bit, the device will be forced to the Standby mode. If an accessory is attached when the ACITVE is set to 0, the accessory identification flow shown in Figure 14 will be re-started.

The PSAVE bit is also a R/W bit. When the 34825 is configured to the Auto Power-save mode (AutoPSAVE bit is set to 1), the PSAVE bit indicates whether the 34825 is in the Power Save mode or not. When the 34825 is configured to the Manual Power-save mode (AutoPSAVE bit set to 0), the host IC can writes '1' to the PSAVE bit to force the 34825 into the Power Save mode when an Audio R/C accessory is attached. For all other accessories attachment, the 34825 does not enter the Power Save mode even the PSAVE bit is set to 1.

Table 5. The Device Modes vs. the Register Bits

PSAVE	ACTIVE	MODE
0	0	Standby
0	1	Active
1	1	Power Save
1	0	Undefined

POWER-UP

The 34825 has four possible power-up scenarios depending on which of the VDD pin and the VBUS pin is powered up first. The four scenarios correspond to the following four mode transitions.

1. **From Power Down to VBUS Power:** the VBUS pin is powered up when $V_{DD} < V_{VDDPOR}$ (VDD POR threshold)
2. **From VBUS Power to Standby:** VBUS is already powered when the VDD voltage rises above its POR threshold
3. **From Power Down to Standby:** the VDD pin is powered up when $V_{BUS} < V_{VBUSPOR}$ (VBUS POR threshold)
4. **From Standby to Active:** the VDD pin is already powered when the VBUS voltage rises above its POR threshold

SCENARIO 1: VDD = 0 V AND VBUS IS POWERED UP (POWER DOWN MODE TO VBUS POWER MODE TRANSITION)

If the VDD pin is not powered but the VBUS is powered up within a voltage range between the POR threshold and the OVP (over-voltage protection) threshold, the internal power MOSFET is softly turned on. The IC is in the VBUS Power mode.

In this VBUS Power mode, the $\overline{ISET}$ outputs high-impedance and all registers are in the reset state. The power MOSFET remains on unless it is disabled by the over-voltage protection or the over-temperature protection block.

SCENARIO 2: VBUS = HIGH AND VDD IS POWERED UP (VBUS POWER MODE TO STANDBY MODE TRANSITION)

If the VBUS pin is already powered when the VDD pin is powered up, the device moves from the VBUS Power mode to the Standby mode and then quickly moves to the identification flow of the Active mode to identify the accessory, as shown in Figure 14.

After the VDD pin is powered up, the 34825 starts up the internal supplies. The POR resets all register bits. The power MOSFET remains on during the reset process.

SCENARIO 3: VBUS = 0 V AND VDD IS POWERED UP (POWER DOWN MODE TO STANDBY MODE TRANSITION)

If no accessory is plugged into the micro or mini-USB connector when VDD is powered up, the 34825 moves from the Power Down mode to the Standby mode. The internal supplies are started up first, and then the whole chip is reset and is ready to accept accessories. Then when an accessory is attached, the 34825 enters the Active mode. The power MOSFET is off in this case since VBUS = 0 V.

SCENARIO 4: VDD = HIGH AND VBUS IS POWERED UP (STANDBY TO ACTIVE MODE TRANSITION)

This is a normal VBUS detection case as shown in Figure 14. More description can be found in Power Supply Type Identification.

ACCESSORY IDENTIFICATION

Accessories are categorized into two groups. Powered accessories are accessories that supply power to the VBUS pin while non-powered accessories do not. When the accessory is a powered one, the VBUS-detection mechanism will check the connection between the D+ and the D- pins as part of the power supply type identification (PSTI). A powered accessory may or may not have an ID resistor. A non-powered accessory must have an ID resistor for the identification purpose.

Accessories that have an ID resistor are grouped into three types, as listed in Table 21.

1. Test Accessories. Such accessories include two USB test cables that are powered accessories, and two UART test cables that are non-powered accessories. A test accessory has an ID resistor and four ID resistor values are reserved for them (see Table 21 for the ID resistor assignment). Two logic output pins, TEST1 and TEST2, are offered to indicate the attachment of such accessories (see Table 8). The USB or the UART switches in the IC will be turned on automatically when a test accessory is attached.
2. Accessories with a remote controller. Two accessories are offered to support remote control (RC) keys. The ID resistor values are 619 kΩ and 1.0 MΩ respectively, as given in Table 21. Such accessories are non-powered accessories. The 34825 monitors the ID pin continuously for key pressing when such an accessory is connected. 13 ID resistors are assigned to the remote control keys, as listed in Table 21.
3. Other accessories. The remaining ID resistor values are reserved for users to assign to their own accessories.

The identification flow chart is shown in Figure 14. In the Standby mode, the 34825 monitors both the ID pin and the VBUS pin simultaneously. If an accessory is detected, the identification state machine will find out in parallel the ID resistor value and the type of the power supply (if a powered accessory is attached). When the 34825 is in the Active mode with the ACTIVE bit = 1, the host IC can force the ACTIVE bit to 0 via the I^2C bus to initiate the identification state machine.

The details on the identification flow for the VBUS-detection mechanism and the ID detection mechanism are described as following.

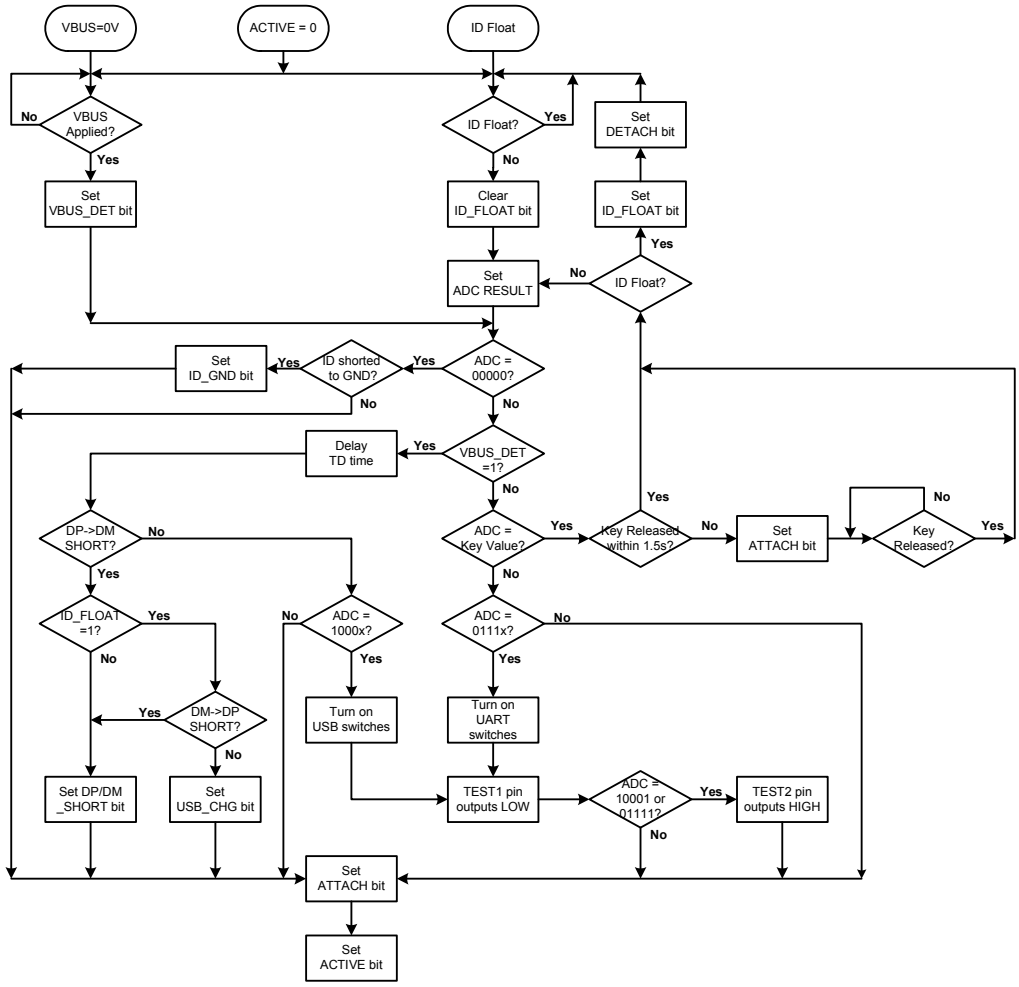


Figure 14. Detailed Accessory Identification Flow Diagram

ID DETECTION

The ID detection relies on the resistance between the ID pin and the ground (R_{ID}) inside the accessory for the accessory detection and recognition. The nominal ID resistance that the 34825 supports is listed in Table 6 as well as in Table 21. The 34825 offers a 5-bit ADC for the resistance recognition and the corresponding ADC results vs. the R_{ID} are also listed in Table 6. The resistors are required to have 1% or better accuracy for the ADC to recognize successfully.

A comparator monitors the ID pin for attachment and detachment detection. When no accessory is attached, the ID pin is floating. An ID_FLOAT bit in the Status register stays in the value of 1. When a resistor less than or equal to 1.0 MΩ is connected between the ID line and the ground, the ID_FLOAT bit changes to 0. When the resistor is removed, ID_FLOAT bit returns to 1. A falling-edge of the ID_FLOAT bit represents the attachment of the accessory and the ADC is enabled to measure the ID resistance. The ADC Result register has the identification result of the R_{ID}, as given in Table 6. A rising edge of the ID_FLOAT bit represents the detachment of the accessory.

The ADC results are broken into two groups. The values between '00001' to '01101' are assigned to 13 remote-control keys for the two accessories that support remote controllers, as listed in Table 21. The rest of the ADC results are assigned to various accessories. If the ADC result is one of the remote control key values in the identification flow, it is possible that the remote control key is stuck when the accessory is attached.

A special Stuck Key Identification flow is designed to resolve such an issue. As shown in the Figure 14, if the stuck key is recognized but is released within 1.5s, the identification flow will return to re-detect the ID line; Otherwise, the ATTACH bit will be set and the ADC Result register has the key result. After the key is released, the 34825 will detect the ID resistance value again. If the accessory is still connected, the ATTACH bit is set again and the ADC result has the ID resistor value of the accessory.

When the ADC result is 00000, the resistance between the ID pin and the ground is less than 1.90 kΩ. The ID_GND bit in the Status register indicates whether the ID pin is shorted to ground or not. If the ID pin is shorted to ground with less than 30 Ω of resistance, the ID_GND pin is set to “1”.

Table 6. ADC Output vs. Resistor Values (Unit: kΩ)

ADC Result	R_{ID} (kΩ)	ADC Result	R_{ID} (kΩ)	ADC Result	R_{ID} (kΩ)	ADC Result	R_{ID} (kΩ)
00000	(1)	01000	10.03	10000	40.2	11000	255
00001	2.00	01001	12.03	10001	49.9	11001	301
00010	2.604	01010	14.46	10010	64.9	11010	365
00011	3.208	01011	17.26	10011	80.6	11011	442
00100	4.014	01100	20.5	10100	102	11100	523
00101	4.820	01101	24.07	10101	121	11101	619
00110	6.03	01110	28.7	10110	150	11110	1000
00111	8.03	01111	34.0	10111	200	11111	(2)

Notes
1. If the ID resistance is below 1.90 kΩ (nominal value), the ADC result is set to 00000.
2. If the ID line is floating, the ADC result is set to 11111

POWER SUPPLY TYPE IDENTIFICATION

The 34825 supports various standard power supplies for charging the battery. The power supplies supported include those that are user defined, and the ones defined in the *Battery Charging Specification, Revision 1.0,* from the USB Implementer’s Forum and the *CEA-936-A USB Carkit Specification*, from the Consumer Electronics Association. The five types of power supplies specified in the afore mentioned two specification documents are listed in Table 7.

The Power Supply Type Identification (PSTI) function is offered to assist the identification of the power supply type. The PSTI state machine checks the connection status between the DP and the DM pins. The state machine starts when the VBUS pin voltage rises above the VBUS detection threshold, which is indicated with an VBUS_DET bit in the status register. The state machine will find out if the DP and DM pins are shorted, indicated with the DP/DM_SHORT bit, or the connection has the characteristics of a USB charger, indicated with the USB_CHG bit. Together with the ID detection result, the power supply type can be determined. The conditions for reaching the conclusion of the five supported power supplies are listed in Table 7.

Table 7. Power Supply Type vs. Detection Result

Item #	VBUS_DET	DP/DM_SHORT	USB_CHG	ID_FLOAT	ADC Result	Accessory Type
1	1	0	0	1	11111	Standard USB Port
2	1	0	1	1	11111	USB Charger
3	1	1	0	1	11111	Dedicated Charger
4	1	1	0	0	10111	Carkit Charger Type 1
5	1	1	0	0	11011	Carkit Charger Type 2

OPERATION AFTER IDENTIFICATION

The operation after the identification is dependent on the VDDIO voltage. The VDD voltage has to be higher than its POR threshold for the 34825 to perform the identification state machine. Once completed, the identification results are stored in the Status and the ADC Result registers and the ATTACH bit is set. If the VDDIO is not powered, the interrupt signal from the $\overline{INT}$ pin cannot be sent because the $\overline{INT}$ pin is normally pulled up to the VDDIO. The host cannot access the 34825 either via the I^2C bus. Hence, no communication will occur between the 34825 and the host IC when the VDDIO is not powered. The $\overline{INT}$ signal will send an interrupt signal if the VDDIO is powered and the ATTACH bit is not masked by the ATTACH_m bit (refer to Interrupt on page 26 for more details). If the ATTACH bit is masked while the VDDIO is powered, the interrupt signal will not be sent but the host IC can still access the register map via the I^2C bus. Once the host IC accesses the 34825 register map and determines the accessory type, it can manage the analog switches and other signals in the 34825 by programming the S/W Control 1 and S/W Control 2 registers.

The switches are open by default except if the attached accessory is one of the four test cables listed in Table 21. More descriptions on the analog switches and the operation of the 34825 are given in the following sections.

ANALOG SWITCHES

SIGNAL SWITCH ARRAY

The 34825 offers an array of analog switches for signal switching, as shown in Figure 15. Two pairs of switches (USB and UART) are for switching the UART and USB signals to the micro or mini-USB connector. Stereo audio signals can be switched from the SPK_L and the SPK_R inputs to the DP and the DM pins that are wired to the USB connector. Both the SPK_L and the SPK_R inputs are capable of passing signals of +/-1.5 V, referencing to the GND pin voltage. The SPK_L and the SPK_R pins are pulled down to ground via a 100 kΩ resistor respectively, as shown in Figure 15. A microphone switch connects the MIC pin to the VBUS pin.

All switches are controlled by bits in the S/W Control 1 and 2 registers except when the accessory attached is a test cable.

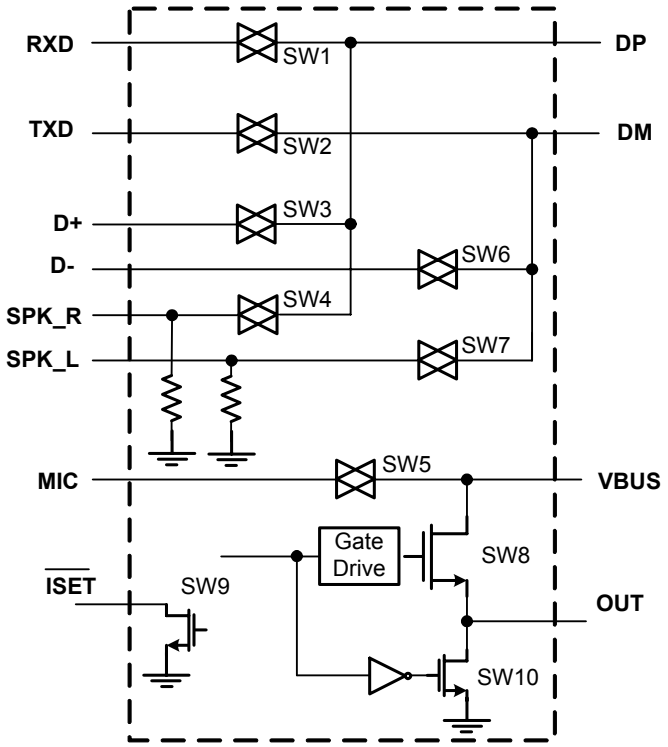


Figure 15. Analog and Digital Switches

POWER MOSFET

The SW8 in Figure 15 is a power MOSFET that controls the power flow from the VBUS input to the OUT pin. The power MOSFET serves two purposes. For the Audio accessory with microphone, the power MOSFET isolates the

VBUS pin from both the input decoupling capacitor and the input quiescent current of the charger IC connected to the OUT pin, so that the microphone signal can be connected to the VBUS pin without any interference from the OUT pin. The power MOSFET is also used as the input Over-voltage Protection (OVP) or Over-current Protection (OCP) switch for other components in the cell phone, such as the charger IC, to allow a low voltage rated charger IC to be used for cost reduction.

The power MOSFET is guaranteed to be turned on in VBUS power mode even when the VDD voltage is below V_{VDDPOR} threshold, to ensure that the cell phone battery can be charged when the battery is fully discharged.

PROTECTION

OVER-VOLTAGE PROTECTION (OVP)

The VBUS line is capable of withstanding a 28 V voltage. The 34825 protects the cell phone by turning off the internal power MOSFET when the VBUS voltage is higher than the OVP threshold. In this case, the 34825 turns off the power MOSFET within 1.0 μs after the input voltage exceeds the OVP threshold, and the OVP_EN bit in the Interrupt register is set to interrupt the host IC. When the OVP event is cleared, the OVP_OTP_DIS bit in the Interrupt register is set to inform the host IC.

OVER-CURRENT PROTECTION (OCP) AND OVER-TEMPERATURE PROTECTION (OTP)

If the current flowing through the power MOSFET exceeds the specified OCP limit, the 34825 will operate in CC (Constant Current) mode, regulating the output current at the OCP limit. If the OCP condition persists, the IC temperature will rise, eventually reaching the Over-Temperature-Protection (OTP) limit. The 34825 then turns off the power MOSFET and sets the OTP_EN interrupt bit in the Interrupt register to inform the host IC. The power MOSFET is turned on again when the IC temperature falls below the OTP falling temperature threshold, and the OVP_OTP_DIS bit is set. If the above case happens repeatedly 7 times, the power MOSFET will be permanently turned off until the accessory is detached or the IC is reset.

The power MOSFET is turned off with a limited speed under the OTP case to prevent a high overshoot voltage at the VBUS pin.

OPERATION WITH ACCESSORIES

AUDIO ACCESSORY SUPPORTING REMOTE CONTROLLER (R/C ACCESSORY)

Two ID resistors are designated for accessories with a remote controller, as listed in Table 21. A typical accessory with a remote controller is an audio headset that has a stereo speaker, a micro phone, and a remote controller, as shown in Figure 16. The five pins in the mini or micro-USB connector are assigned in Figure 16. If some components are not included in the accessory, the corresponding pins should be left floating. For example, if the microphone is not included in the stereo headset, VBUS pin should be left floating in the headset.

The timing of the key pressing is shown in Figure 17. If a key is pressed for a time less than 20 ms, the 34825 ignores this key press. If the key is still pressed after 20 ms, 34825 starts a timer to count the time during which the key is pressed. There are three kinds of key press conditions according to the pressing time: error key press, short key press, and long key press.

1. Error key press: if the key pressing time is less than T_{KP}, The 34825 ignores this key press.
2. Short key press: if the key pressing time is between T_{KP} and T_{LKP}, the KP bit is set to inform the host IC. The ADC result holds the key value. The $\overline{INT}$ outputs low impedance when the key is released and returns to a high impedance, due to the clearance of the KP bit when the interrupt register is read.
3. Long key press: if the key pressing time is longer than T_{LKP}, the long key press bit LKP in the Interrupt register is set to inform the host IC. The host IC needs to respond to the key press immediately. The ADC result holds the key value. When the key is released, the long key release bit LKR in the Interrupt register is set to interrupt the host IC again. The ADC Result register still has the key value.

When such a accessory is attached, the 34825 can either be forced into the Power Save mode or automatically enter into the Power Save mode. This is controlled by the AutoPSAVE bit in the Control register.

When AutoPSAVE = 1, if no activity is detected at the SPK_L and SPK_R pins in 10 seconds, the 34825 enters the Power Save mode automatically to minimize the quiescent current. Upon detecting the activity in audio signal switches, the 34825 returns to the Active mode. When AutoPSAVE = 0, the host IC can control the mode of 34825 manually by setting the PSAVE bit in the Device Mode register via I^2C.

In the Power Save mode, the key pressing is monitored as well.

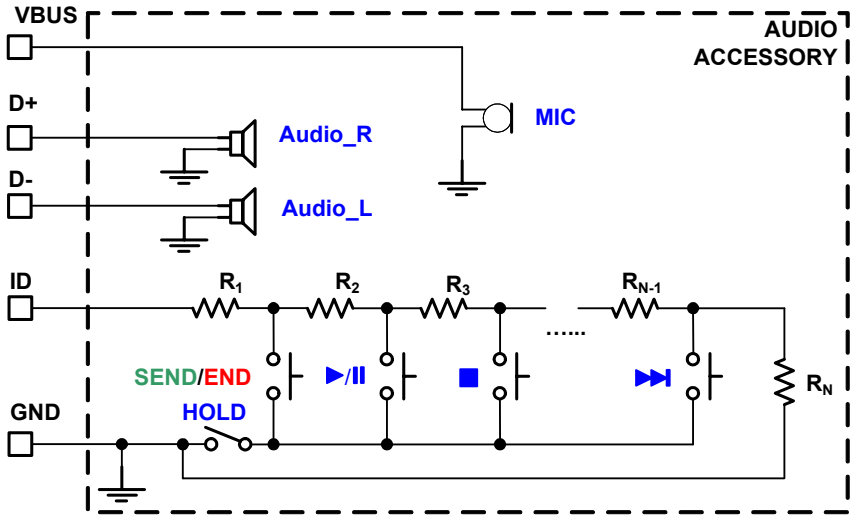


Figure 16. Audio Accessory with Remote Control and Microphone

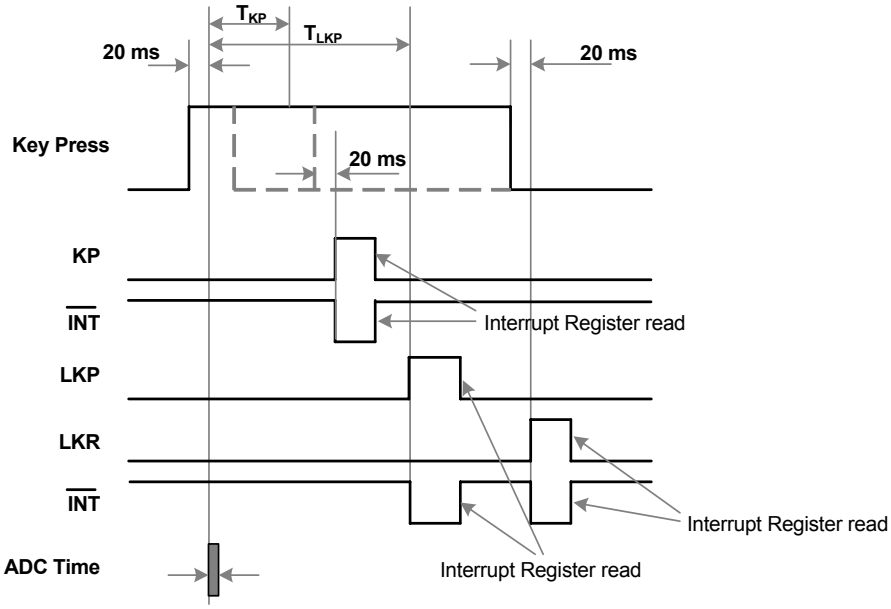


Figure 17. The Remote Control Key Pressing Timing

TEST ACCESSORY

The Test Accessories listed in Table 21 are special USB cables and UART cables for test and R/D purpose. It has an ID resistance to differentiate it from a regular USB cable or UART cable. The test accessory has four ID resistance values to distinguish the test cable type. The detection result sets the TEST1 and the TEST2 outputs and turns on or off the USB switches, UART switches, and the power MOSFET automatically, as shown in the Table 8.

The TEST1 and the TEST2 outputs are High and Low respectively by default but can be changed by the TEST1 and TEST2 bits in the S/W Control 2 register, if the accessory is *NOT* a test cable. If the accessory is a test cable, the TEST1 outputs Low always and the TEST2 is dependent on the actual test cable. The TEST1 and TEST2 output cannot be changed by the TEST1 and the TEST2 bits in the S/W Control 2 register. The corresponding analog switches, either USB or UART switches, are turned on automatically in the case of a test cable. The TEST1, TEST2, and the switch status are summarized in Table 8.

Table 8. TEST1, TEST2, and Switch Status vs. Test Cables

Accessory Type	ADC Result	TEST1 Output	TEST2 Output	Auto-ON Switches	Power MOSFET
UART test cable type 1	01110	LOW	LOW	UART Switches	OFF
UART test cable type 2	01111	LOW	HIGH	UART Switches	OFF
USB test cable type 1	10000	LOW	LOW	USB Switches	ON
USB test cable type 2	10001	LOW	HIGH	USB Switches	ON
Other accessories	others	HIGH(1)	LOW(1)	No auto-on Switches	No auto-on Switches

Notes
1. These values are default values and can be changed by the TEST1 and TEST2 bits in the S/W Control 2 register.

USB HOST (PC OR HUB)

When the attached accessory is a USB host or hub, the ID pin is floating. The power MOSFET is turned on to allow the charger to charge the battery. The $\overline{\text{ISET}}$ outputs default high impedance to limit the charging current to a lower level. The host IC can turn on the D+ and D- switches and then pull the D+ signal to high to start the USB attaching sequence.

USB CHARGER OR DEDICATED CHARGER

When the attached accessory is a USB Charger or a Dedicated Charger, the 34825 turns on the power MOSFET to allow the charger to start. The host IC can set the $\overline{\text{ISET}}$ outputs low impedance to allow a higher charge current.

5-WIRE CARKIT CHARGER (TYPE 1 OR TYPE 2)

A 5-wire carkit charger is a charger specified in the *CEA-936-A USB Carkit Specification*. The 5-wire carkit charger outputs 5V to the VBUS pin, has the D+ and D- pins shorted internally, and has an ID resistor. The ID resistor has a value of either 200kΩ or 440kΩ to distinguish the current capability of the charger. Refer to the *CEA-936-A USB Carkit Specification* for more information.

When the attached accessory is a 5-wire carkit charger, the 34825 turns on the power MOSFET to allow the Li-ion battery charging function to start. The host can set the $\overline{\text{ISET}}$ outputting high impedance or low impedance to choose the charge current.

RESERVED ACCESSORY

The users can assign the reserved ID resistor values listed in Table 21 to their user specific accessories. When a user specific accessory is attached, the identification flow will identify the ID resistance and as well as the power supply type in case of a powered accessory. The ADC Result register and the Status register contain the information of the R_{ID} value and the power supply type. The baseband can read these registers to distinguish the type of the accessory for further actions.

DETACHING DETECTION

When either the VBUS voltage drops below the VBUS power detection threshold or the ID resistor is removed, a detaching detection flow starts. Figure 18 shows the detailed detection flow. When the DETACH bit is set, the $\overline{\text{INT}}$ outputs low voltage to inform the host IC. At the end of the detaching detection flow, the ACTIVE bit is cleared and the 34825 enters the Standby mode. A new identification flow will start if either the VBUS voltage is above its POR threshold or the ID resistor is connected.

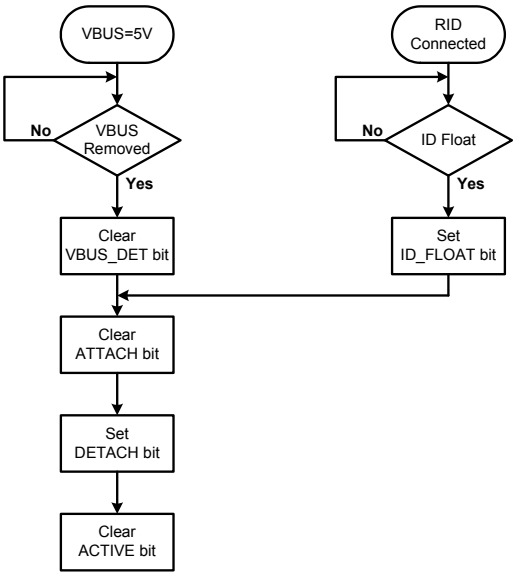


Figure 18. The Detachment Detection Flow

LOGIC CONTROL FEATURES

RESET

HARDWARE RESET

The 34825 has three sources for hardware resetting the IC. As the Figure 19 shows, the sources include the Power-On-Reset caused by the rising VDD, a hardware reset caused by the VDDIO input and a hardware reset using the I^2C bus lines. The Power-On-Reset is described earlier. The reset caused by the VDDIO input or by the I^2C bus lines belongs to system resets.

The hardware reset condition using the I^2C signals is shown in Figure 20. When both the I^2C_SCL and the I^2C_SDA have a negative pulse with time of t_{RSTI2C}, a hardware reset is generated. The result of the reset is same as a Power-On-Reset.

The operating waveforms of the hardware reset using the VDDIO pin are shown in Figure 21. The VDDIO detection has a deglitch-time $t_{VDDIODGT\_F}$. A glitch on the VDDIO with duration less than the deglitch time will be ignored. If the pulse on the VDDIO lasts longer than the deglitch time, a reset from the VDDIO is detected to generate a reset signal. To effectively reset the 34825, the reset pulse from the VDDIO needs be longer than the 150 μs minimum reset pulse width given in the Dynamic Electrical Characteristics table.

SOFTWARE RESET

In addition to the two hardware reset types, the system reset has another reset source, the software reset by writing '1' to the RESET bit in the Control register. The Reset bit will be cleared to '0' at once since it is of W/C type. The consequence of the software reset is the same as the hardware reset. All registers will be reset.

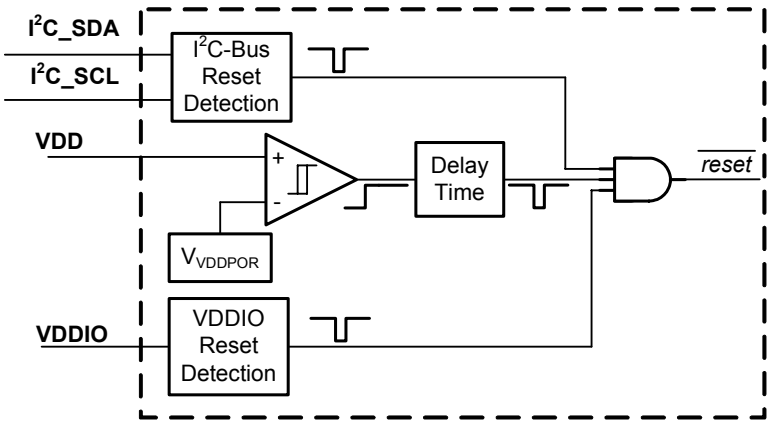


Figure 19. Sources of Reset in 34825

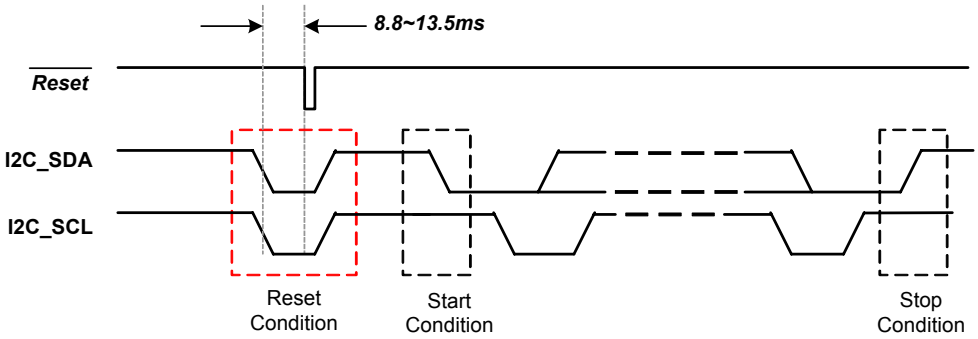


Figure 20. Hardware Reset Using the I²C Bus

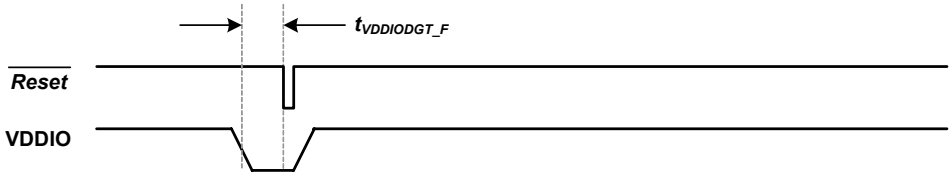


Figure 21. Hardware Reset Using the VDDIO Input

INTERRUPT

There are eight interrupt sources in the 34825 causing an interrupt at the INT pin to the host IC. They are accessory attachment, accessory detachment, short-key press, long key press, long-pressed key release, VBUS voltage OVP, the IC temperature OTP, and either the OVP or the OTP condition is removed. The 34825 detects each event and sets the corresponding bit in the Interrupt register. As long as the Interrupt register is set, the INT pin outputs low voltage. The Interrupt register is not writable. When the Interrupt register is read, the Interrupt register is cleared automatically. Once the Interrupt register is cleared, the INT pin returns to high voltage.

An interrupt mask register is provided to mask unwanted interrupt source. When the bit of the Interrupt Mask register is set to 1, the corresponding interrupt source is blocked. The INT does not output low voltage even though this interrupt bit is set in the Interrupt register.

LOGIC OUTPUT

There are three logic outputs pins:TEST1, TEST2 and ISET. They are controlled by the register bits with the same name in the Control register if the attached accessory is *NOT* a test cable. The TEST2 output is a push-pull output with the voltage pulled up to the VDDIO, and the rest of them are open-drain outputs.

The ISET generally is used to control the charge current level. A typical charger IC uses one external resistor to set

the charge current. By using $\overline{\text{ISET}}$ output, the charger IC can use two external resistors in parallel to set two charge current levels, as shown in Figure 27.

I²C SERIAL BUS INTERFACE

The I²C bus is enabled in the Standby, the Power Save, and the Active modes. The serial clock (SCL) and the serial data (SDA) lines must be connected to a positive supply using pull-up resistors. Internally the I²C bus voltage is referenced to the VDDIO input. The 34825 is a slave device. Maximum data rate is 400 kbps.

ADDRESSING AND PROTOCOL

The 7-bit address for the 34825 is 0100101, as shown in Figure 22.

0	1	0	0	1	0	1	R/W

Figure 22. I²C Slave Address

The following three figures show three I²C-bus transaction protocols. The Word Address is an 8-bit register address in the 34825.

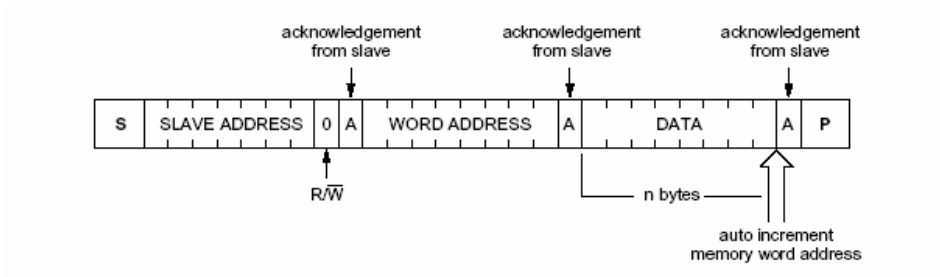


Figure 23. Master Transmits to Slave (Write Mode)

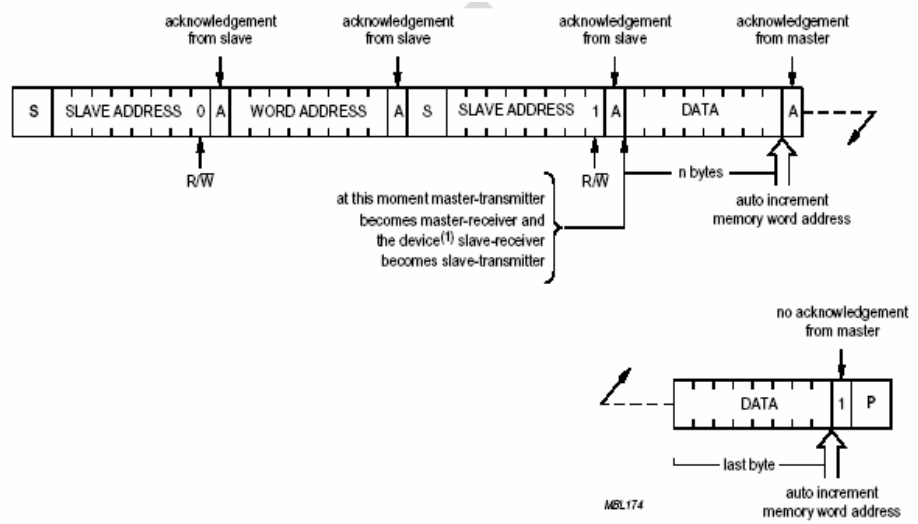


Figure 24. Master Reads After Setting Word Address (Write Word Address and then Read Data)

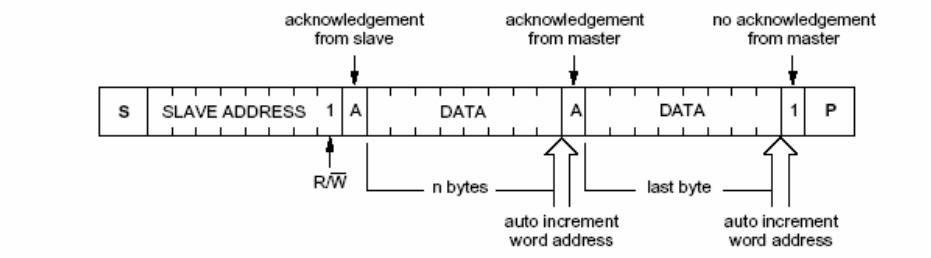


Figure 25. Master Reads Slave Immediately after First Byte (Read Mode)

REGISTER MAP

Table 9. Register Map

Addr	Register	Type	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
83H	Interrupt	R/C	00000000	OVP_OTP_DIS	OTP_EN	OVP_EN	LKR	LKP	KP	DETACH	ATTACH
85H	Interrupt Mask	R/W	00000000	OVP_OTP_DIS_m	OTP_EN_m	OVP_EN_m	LKR_m	LKP_m	KP_m	DETACH_m	ATTACH_m
87H	ADC Result	R	00011111	Reserved	Reserved	Reserved	ADC Value				
88H	Timing Set	R/W	00000000	Key Press				Long Key Press			
93H	S/W Control 1	R/W	00000001	Reserved			DP/DM Switching			VBUS Switching	
94H	S/W Control 2	R/W	00000100	Reserved	Reserved	Reserved	ISETB	TEST2	TEST1	Reserved	
A0H	Status	R	0x000xxx	Reserved	FET_STATUS	USB_CHG	DP/DM_SHORT	ID_GND	ID_FLOAT	VBUS_DET	ADC_STATUS
A1H	Control	R/W	011000x0	Reserved	Reserved	AutoPSAVE	Reserved	Reserved	RESET	Reserved	Reserved
A2H	Time Delay	R/W	10010100	Reserved	Reserved	Reserved	Reserved	TD			
A3H	Device Mode	R/W	00000001	Reserved	Reserved	Reserved	Reserved	Reserved	PSAVE	ACTIVE	RST

Table 10. Interrupt Register

Bit	Mode	Symbol	Reset	Description	Notes
0	R/C	ATTACH	0	1: accessory attached	
1	R/C	DETACH	0	1: accessory detached	
2	R/C	KP	0	1: remote controller short key is pressed	
3	R/C	LKP	0	1: remote controller long key is pressed	
4	R/C	LKR	0	1: remote controller long key is released	
5	R/C	OVP_EN	0	1: VBUS voltage higher than the OVP threshold	
6	R/C	OTP_EN	0	1: The temperature of 34825 is above the OTP threshold	
7	R/C	OVP_OTP_DIS	0	1: OVP or OTP event is removed	

Table 11. Interrupt Mask Register

Bit	Mode	Symbol	Reset	Description	Notes
0	R/W	ATTACH_m	0	1: interrupt disabled	
1	R/W	DETACH_m	0	1: interrupt disabled	
2	R/W	KP_m	0	1: interrupt disabled	
3	R/W	LKP_m	0	1: interrupt disabled	
4	R/W	LKR_m	0	1: interrupt disabled	

Table 11. Interrupt Mask Register

Bit	Mode	Symbol	Reset	Description	Notes
5	R/W	OVP_EN_m	0	1: interrupt disabled	
6	R/W	OTP_EN_m	0	1: interrupt disabled	
7	R/W	OVP_OTP_DIS_m	0	1: interrupt disabled	

Table 12. ADC Result Register

Bit	Mode	Symbol	Reset	Description	Notes
4-0	R	ADC Result	11111	ADC Result of the ID resistor	
7-5	R	Reserved	000		

Table 13. Timing Set Register

Bit	Mode	Symbol	Reset	Description	Notes
3-0	R/W	Long Key Press	0000	Long key press duration 0000: 300 ms 0001: 400 ms 0010: 500 ms	
7-4	R/W	Key Press	0000	Normal key press duration 0000: 100 ms 0001: 200 ms 0010: 300 ms	

Table 14. Timing Table

Setting Value	Key Press	Long Key Press
0000	100 ms	300 ms
0001	200 ms	400 ms
0010	300 ms	500 ms
0011	400 ms	600 ms
0100	500 ms	700 ms
0101	600 ms	800 ms
0110	700 ms	900 ms
0111	800 ms	1000 ms
1000	900 ms	1100 ms
1001	1000 ms	1200 ms
1010	-	1300 ms
1011	-	1400 ms
1100	-	1500 ms
1101	-	-
1110	-	-
1111	-	-

Table 15. S/W Control Register 1

Bit	Mode	Symbol	Reset	Description	Notes
1-0	R/W	VBUS Switching	01	VBUS line switching configuration 00: open all switches connected to the VBUS line. 01: internal power MOSFET on 10: VBUS connected to MIC 11: open all switches connected to the VBUS line.	
4-2	R/W	DP/DM Switching	000	DP/DM line switching configuration 000: open all switches 001: DP connected to D+, DM connected to D- 010: DP connected to SPK_R, DM connected to SPK_L 011: DP connected to RxD, DM connected to TXD Others: open all switches connected to the DP pin and DM pin	
7-5	R	Reserved	000		

Table 16. S/W Control Register 2

Bit	Mode	Symbol	Reset	Description	Notes
1-0	R/W	reserved	00		
2	R/W	TEST1	1	TEST1 output 0: low-impedance 1: high-impedance	
3	R/W	TEST2	0	TEST2 output 0: low voltage 1: high voltage	
4	R/W	ISETB	0	$\overline{\text{ISET}}$ output 0: high-impedance 1: low-impedance	
7-5	R/W	Reserved	000		

Table 17. Status Register

Bit	Mode	Symbol	Reset	Description	Notes
0	R	ADC_Status	x	ADC conversion status 1: ADC conversion completed 0: ADC in progress	
1	R	VBUS_DET	x	VBUS voltage is higher than the POR 0: no 1: yes	
2	R	ID_FLOAT	x	ID line is floating 0: no 1: yes	
3	R	ID_GND	0	ID pin is shorted to ground 0: no 1: yes	
4	R	DP/DM_SHORT	0	DP/DM shorted 0: no 1: yes	
5	R	USB_CHG	0	A USB charger is connected 0: no 1: yes	
6	R	FET_STATUS	x	The on/off status of the power MOSFET 0: off 1: on	
7	R	Reserved	0		

Table 18. Control Register

Bit	Mode	Symbol	Reset	Description	Notes
0	R/W	Reserved	0		
1	R/W	Reserved	x		
2	W/C	RESET	0	Soft reset. When written to 1, the IC is reset. Once the reset is complete, the RST bit is set and the RESET bit is cleared automatically. 1: to soft reset the IC	
3	R/W	Reserved	0		
4	R/W	Reserved	0		
5	R/W	AutoPSAVE	1	Automatic Power Save mode detection control 0: disable automatic Power Save mode detection. Device can enter Power Save mode via the I^2C 1: enable automatic Power Save mode detection.	
6	R/W	Reserved	1		
7	R/W	Reserved	0		

Table 19. Time Delay Register

Bit	Mode	Symbol	Reset	Description	Notes
3-0	R/W	TD	0100	Time delay to start the powered accessory identification flow after detecting the VBUS voltage 0000: 100 ms 0001: 200 ms 0010: 300 ms 0011: 400 ms 0100: 500 ms ..... 1111:1600 ms	
7-4	R/W	Reserved	1001		

Table 20. Device Mode Register

Bit	Mode	Symbol	Reset	Description	Notes
0	R/C	RST	1	This bit indicates if a chip reset has occurred. This bit will be cleared once being read. 0: no. 1: Yes.	
1	R/W	ACTIVE	0	Indicate either the device is in Active mode 0: Standby 1: Active	
2	R/W	PSAVE	0	To indicate either the device is in Power Save mode 0: no 1: yes	
7-3		Reserved	00000		

TYPICAL APPLICATIONS

APPLICATION INFORMATION

ID RESISTANCE VALUE ASSIGNMENT

The ID resistors used with the 34825 are standard 1% resistors. Table 21 lists the complete 32 ID resistor assignment. The ones with the Assigned Functions filled are the ones that are already used with special functions. The ones reserved can be assigned to other functions.

Table 21. ID Resistance Assignment (Unit: kΩ)

Item#	ADC Result	ID Resistance	Assignment
0	00000	<1.9	Reserved
1	00001	2.0	S0
2	00010	2.604	S1
3	00011	3.208	S2
4	00100	4.014	S3
5	00101	4.820	S4
6	00110	6.03	S5
7	00111	8.03	S6
8	01000	10.03	S7
9	01001	12.03	S8
10	01010	14.46	S9
11	01011	17.26	S10
12	01100	20.5	S11
13	01101	24.07	S12
14	01110	28.7	UART Test Cable 1
15	01111	34.0	UART Test Cable 2
16	10000	40.2	USB Test Cable 1
17	10001	49.9	USB Test Cable 2
18	10010	64.9	Reserved
19	10011	80.6	Reserved
20	10100	102	Reserved
21	10101	121	Reserved
22	10110	150	Reserved
23	10111	200	Carkit Charger Type 1
24	11000	255	Reserved
25	11001	301	Reserved
26	11010	365	Reserved
27	11011	442	Carkit Charger Type 2
28	11100	523	Reserved
29	11101	619	R/C Accessory 1
30	11110	1000	R/C Accessory 2
31	11111	-	ID float

The remote control architecture is illustrated in Figure 26. The recommended resistors for the remote control resistor network are given in Table 22.

Table 22. Remote Control Resistor Values (Unit: kΩ)

Resistor	Standard Value	ID Resistance
R1	2.0	2.0
R2	0.604	2.604
R3	0.604	3.208
R4	0.806	4.014
R5	0.806	4.82
R6	1.21	6.03
R7	2.0	8.03
R8	2.0	10.03
R9	2.0	12.03
R10	2.43	14.46
R11	2.8	17.26
R12	3.24	20.5
R13	3.57	24.07
R14	590/976	614/1000

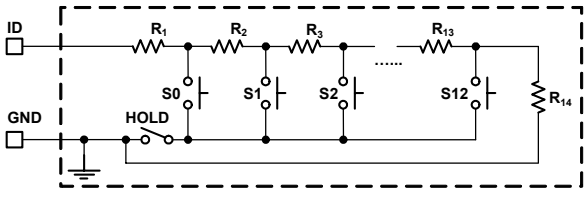


Figure 26. Remote Control Architecture

DECOUPLING CAPACITOR

Decoupling capacitors are required at all power supply input and output pins. For the VDD pin, a X5R capacitor of 1.0 μF is recommended. For VBUS pin, because it also acts as the microphone input, the decoupling capacitance at VBUS pin must be carefully considered. Assuming the voice band is 3.4 kHz and the pull-up resistance for the microphone is 2kΩ, the decoupling capacitance at the VBUS pin should

be less than 22 nF. A 4.7 nF X5R capacitor is recommended for the typical application. The OUT pin requires a 1.0 μF decoupling capacitor; a 0.01 μF capacitance is enough for the VDDIO pin.

TYPICAL APPLICATIONS

INTERFACE CIRCUIT IN A CELL PHONE

When the 34825 is used in a cell phone. The typical circuit is shown in the Figure 27. The I²C bus need two pull-up resistors. Typically they are 4.7 kΩ. When the audio outputs of the cell phone baseband or application processor are direct drive signals, the audio signals can be connected to the corresponding pins of 34825 directly. Otherwise these signals need DC-blocking capacitors to remove the DC level.

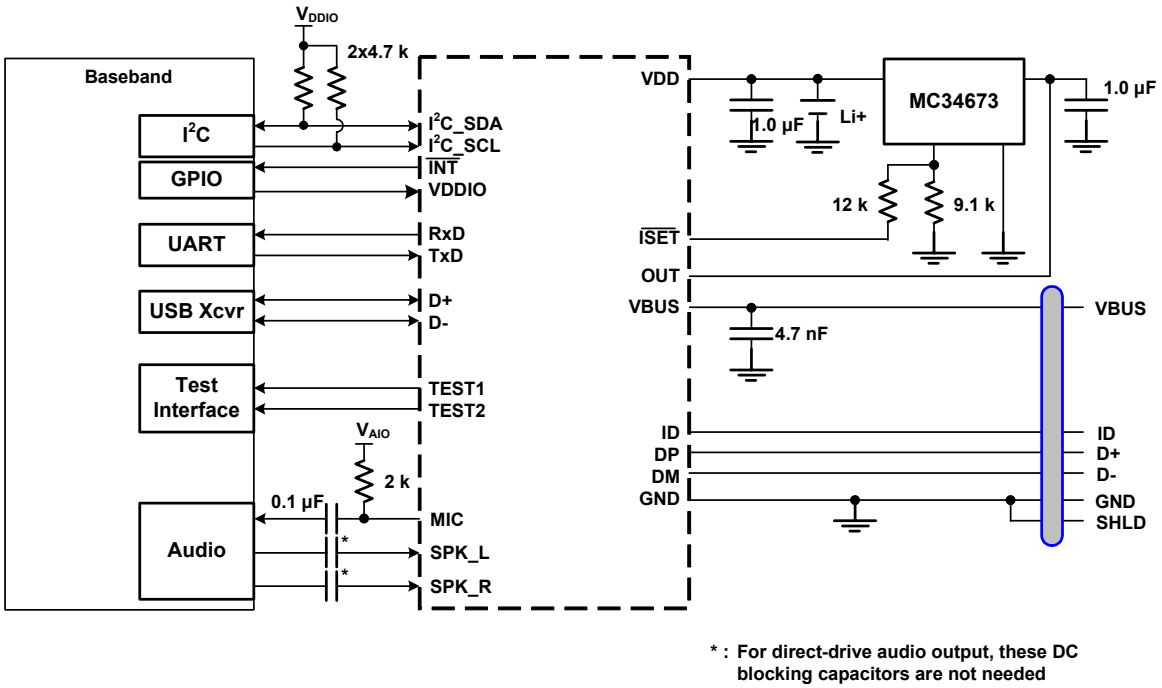
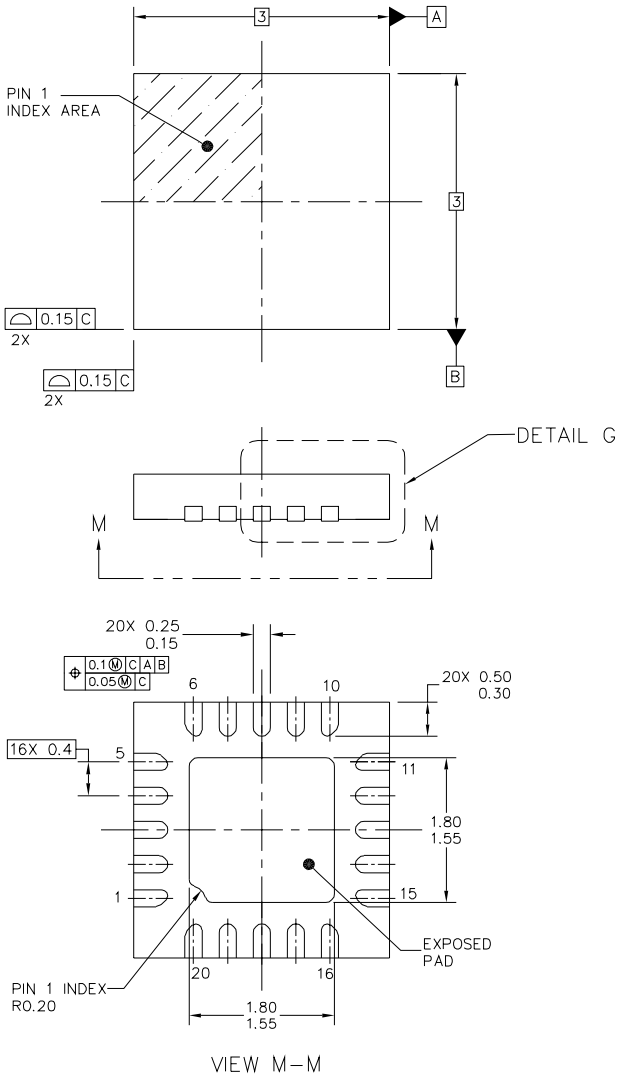


Figure 27. Interface Circuit in a Cell Phone System

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.

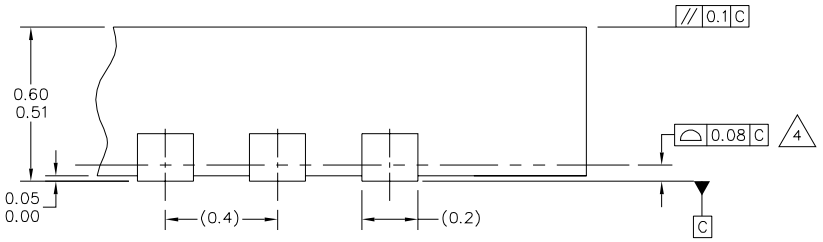


VIEW M–M

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NO LEAD PACKAGE (QFN) 20 TERMINAL, 0.4 PITCH (3 X 3 X 0.6)	DOCUMENT NO: 98ASA00037D	REV: O
	CASE NUMBER: 2064–01	16 DEC 2008
	STANDARD: NON JEDEC	

EP SUFFIX
20 LD. QFN
98ASA00037D
REVISION O

34825



DETAIL G

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NO LEAD PACKAGE (QFN) 20 TERMINAL, 0.4 PITCH (3 X 3 X 0.6)	DOCUMENT NO: 98ASA00037D	REV: O
	CASE NUMBER: 2064-01	16 DEC 2008
	STANDARD: NON JEDEC	

EP SUFFIX
20 LD. QFN
98ASA00037D
REVISION O

34825

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THIS IS NON JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND ALL OTHER BOTTOM SURFACE METALLIZATION.
5. MIN. METAL GAP SHOULD BE 0.2MM.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NO LEAD PACKAGE (QFN) 20 TERMINAL, 0.4 PITCH (3 X 3 X 0.6)	DOCUMENT NO: 98ASA00037D	REV: O
	CASE NUMBER: 2064–01	16 DEC 2008
	STANDARD: NON JEDEC	

EP SUFFIX
20 LD. QFN
98ASA00037D
REVISION O

34825

REVISION HISTORY

	DATE	DESCRIPTION OF CHANGES
1.0	8/2009	• Initial Release

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MC34825
Rev 1.0
8/2009