BUK6208-40C

N-channel TrenchMOS intermediate level FET

Rev. 01 — 9 April 2010 **Objective data sheet**

1. Product profile

1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Suitable for intermediate level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

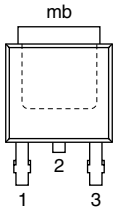
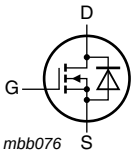
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C	[1]	-	-	50	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 1		-	-	128	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	6.6	8	mΩ
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 50 A; $V_{sup} \leq 40$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	-	210	mJ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; see Figure 6		-	-	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT428 (DPAK)	
2	D	Drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6208-40C	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
V_{GS}	gate-source voltage	Pulsed	[1]	-20	-	20	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V	[2]	-	-	50	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V	[2]	-	-	50	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; $t_p \leq 10$ µs; pulsed		-	-	349	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 1		-	-	128	W
T_{stg}	storage temperature			-55	-	175	°C
T_j	junction temperature			-55	-	175	°C
V_{GS}	gate-source voltage	DC		-16	-	16	V
Source-drain diode							
I_S	source current	$T_{mb} = 25$ °C	[2]	-	-	50	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C		-	-	349	A
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 50$ A; $V_{sup} \leq 40$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped		-	-	210	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[3][4][5]	-	-	-	J

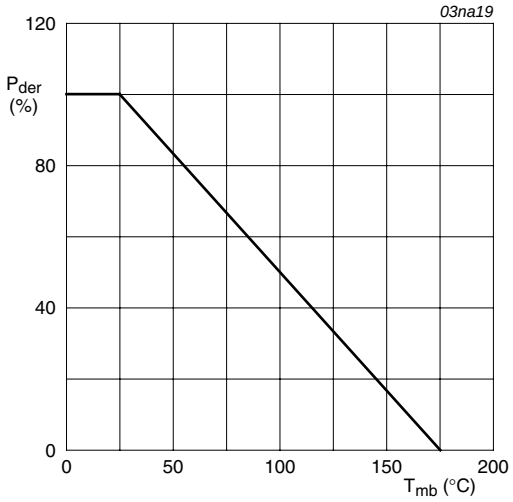
[1] Accumulated pulse duration not to exceed 5mins.

[2] Continuous current is limited by package.

[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[4] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[5] Refer to application note AN10273 for further information.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 2	-	-	1.17	K/W

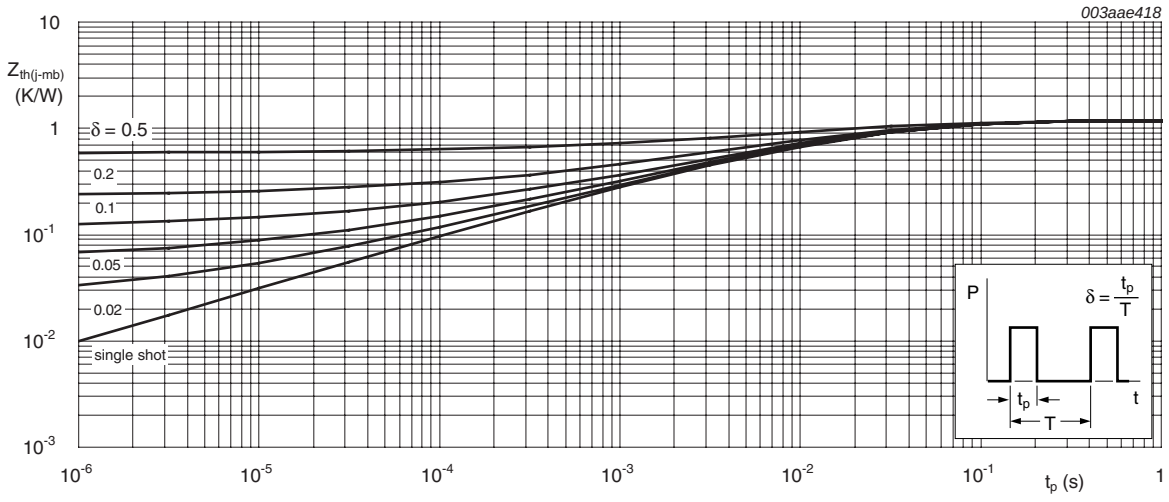
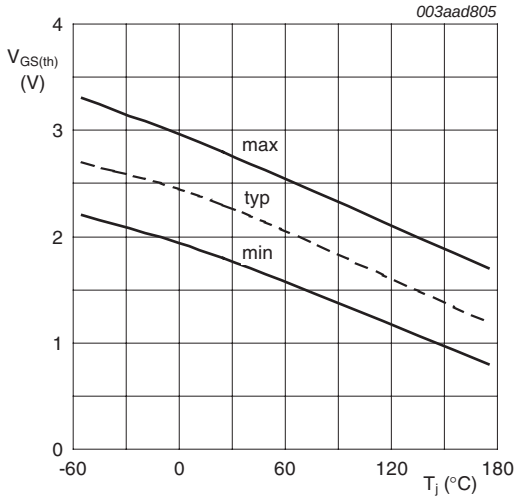


Fig 2. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

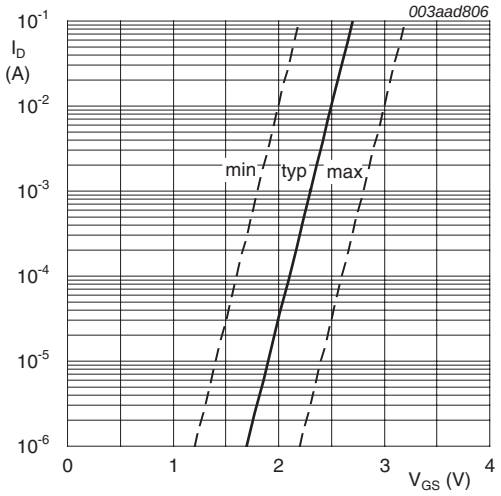
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 3; see Figure 4	1.8	2.3	2.8	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 3	-	-	3.3	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 3	0.8	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 20 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -20 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C	-	6.6	8	mΩ
		V_{GS} = 5 V; I_D = 15 A; T_j = 25 °C	-	-	[tbd]	mΩ
		V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 °C	-	-	[tbd]	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 5	-	-	16.8	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; see Figure 6	-	-	-	nC
		I_D = 25 A; V_{DS} = 32 V; V_{GS} = 5 V; see Figure 6	-	-	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; see Figure 6	-	-	-	nC
Q_{GD}	gate-drain charge		-	-	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C	-	3000	[tbd]	pF
C_{oss}	output capacitance		-	450	[tbd]	pF
C_{rss}	reverse transfer capacitance		-	330	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω	-	-	-	ns
t_r	rise time		-	-	-	ns
$t_{d(off)}$	turn-off delay time		-	-	-	ns
t_f	fall time		-	-	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to centre of die ; T_j = 25 °C	-	3.5	-	nH
L_S	internal source inductance	from source lead to source bond pad ; T_j = 25 °C	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V	-	-	-	ns
Q_r	recovered charge		-	-	-	nC



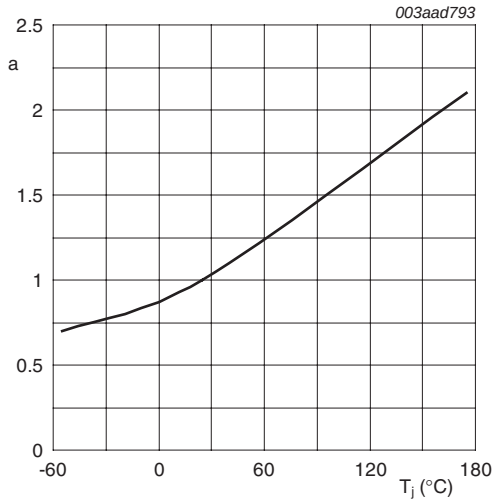
$$I_D = 1mA; V_{DS} = V_{GS}$$

Fig 3. Gate-source threshold voltage as a function of junction temperature



$$T_j = 25\,°C; V_{DS} = 5V$$

Fig 4. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

Fig 5. Normalized drain-source on-state resistance factor as a function of junction temperature

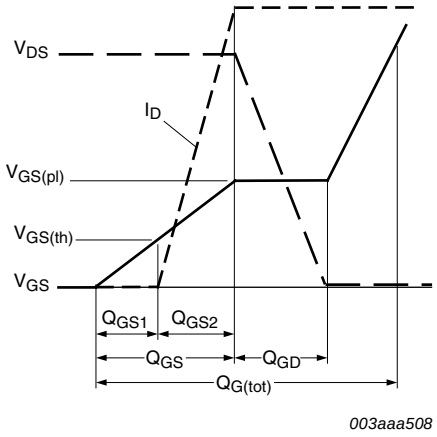
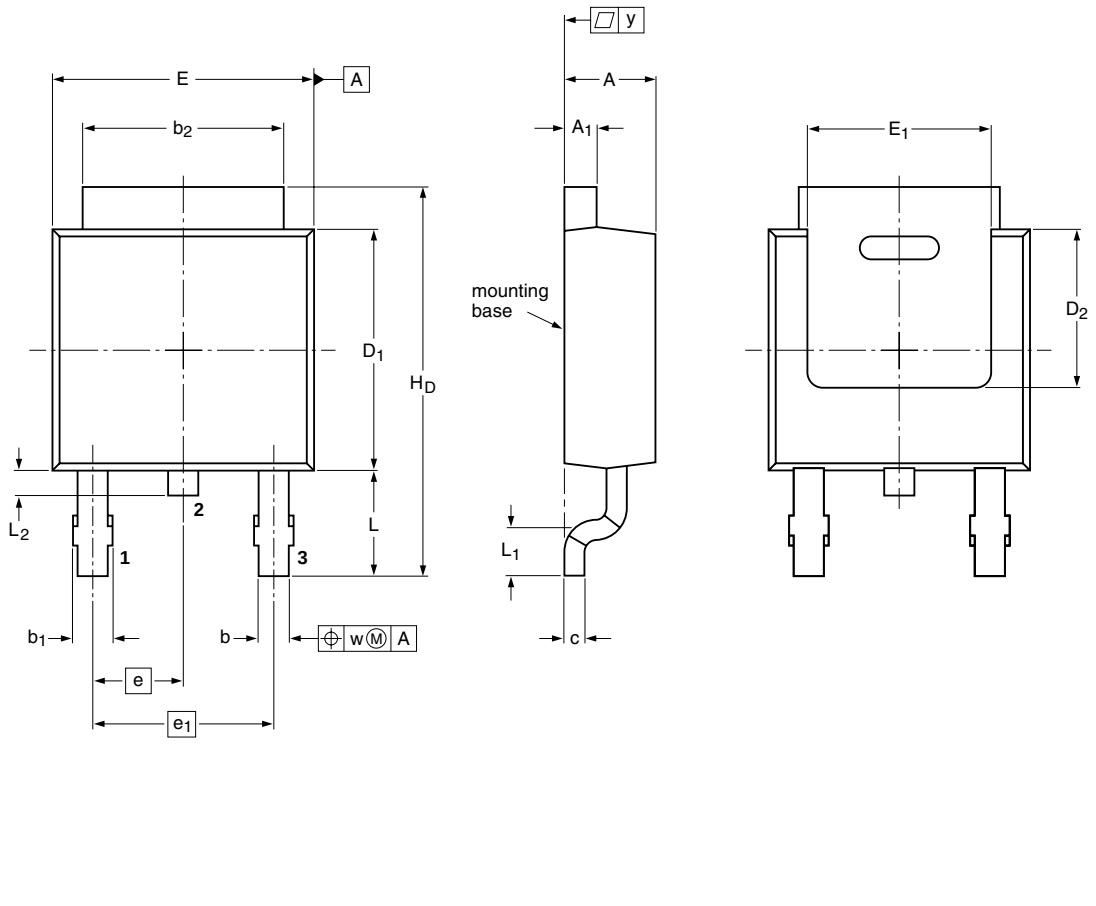


Fig 6. Gate charge waveform definitions

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig 7. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK6208-40C_1	20100409	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

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