A1 PROs

Ai2410

Signal Processor for Single-Chip CCD B/W Camera

Description

The A*i*2410 is a signal processor for CCD B/W camera application. It combines CCD analog signal processor, timing logic controller and vertical into one single chip.

Function

- Timing Logic Controller
- CDS (Correlated Double Sampling)
- AGC (Automatic Gain Control)
- Gamma Corrections
- Video Driver
- Vertical Driver

Features

- 5 steps sample and hold
- Wide dynamic range -4 to 32dB of AGC
- Built-in Opamp for AGC control loop
- 3 Mode dark-clip control
- 2 Mode white-clip control
- 75 ohm video driver and SAG compensation
- Auto Iris and electronic shutter mode
- Supports EIA/ CCIR of 510H/760H system CCD image sensors
  760H: 28.63636MHz (EIA) and 28.375MHz (CCIR)
  510H: 19.0699MHz (EIA), 18.9375MHz (CCIR)
- Built-in sync signal generation function
- Support external sync function

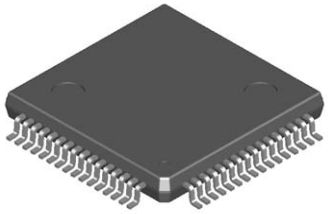
Application

CCD monochrome camera

Structure

BiCMOS silicon monolithic IC

64 pin LQFP (7x7)

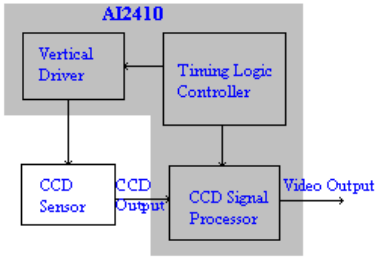


Absolute Maximum Ratings (Ta = 25 ^{o}C)

Parameter	Rating	Unit
Supply voltage Vcc, V_{DD}	7	V
Supply voltage V_{EE}	Reference voltage	V
Supply voltage V_{HH}, V_{ME}	V_{EE} - 0.3 to V_{HH} + 0.3	V
Storage Temperature T_{STG}	$-65 \sim +150$	^{o}C
Operating Temperature T_{OPR}	$-20 \sim +75$	^{o}C
Allowable Power Dissipation P_D	500	mW

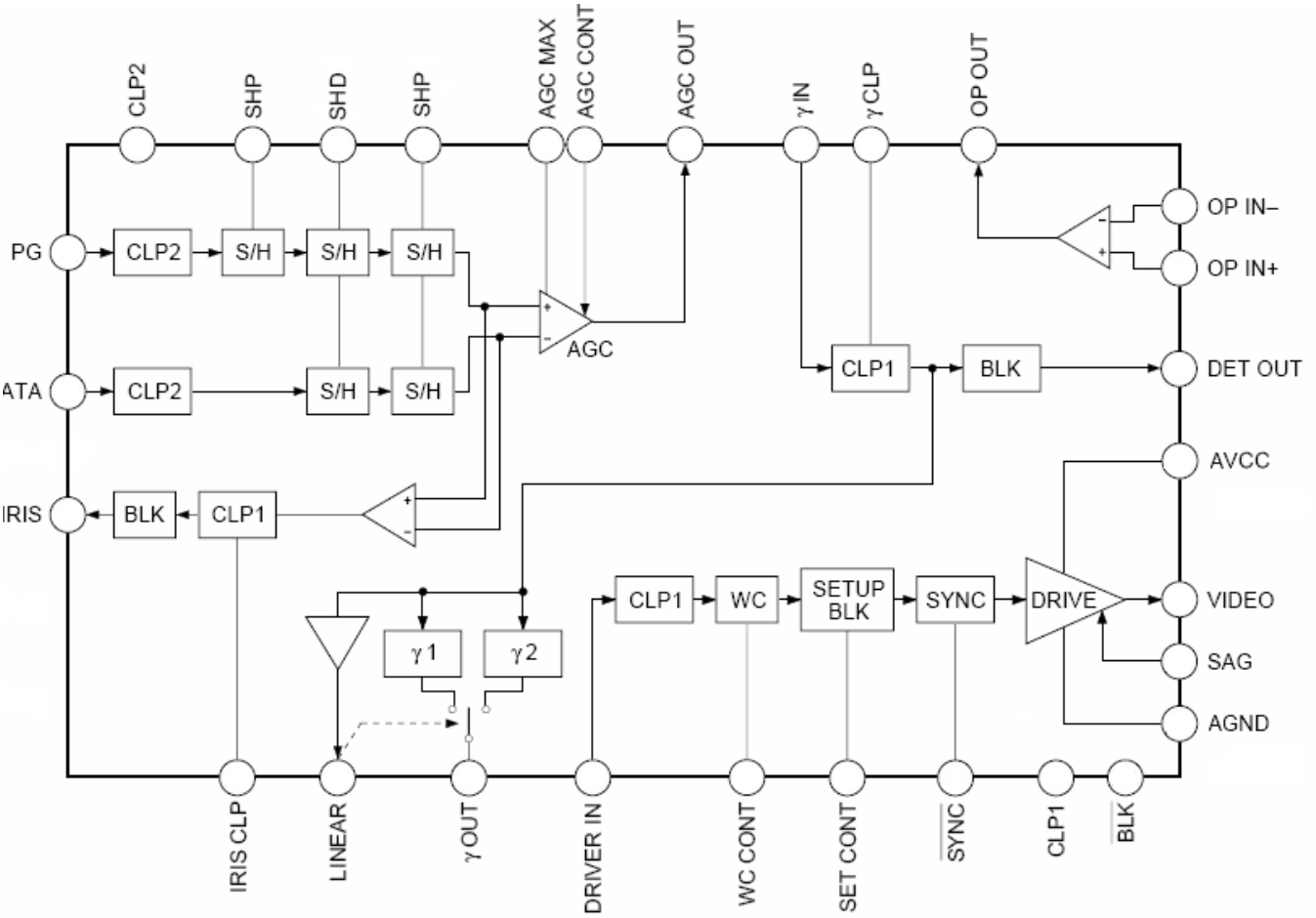
Operating Conditions

Parameter	Rating	Unit
Supply Voltage Vcc, V_{DD}	4.75 ~ 5.25	V
Supply voltage V_{HH}	V_{EE} + 25	V
Supply voltage V_{ME}	V_{EE} + 10	V

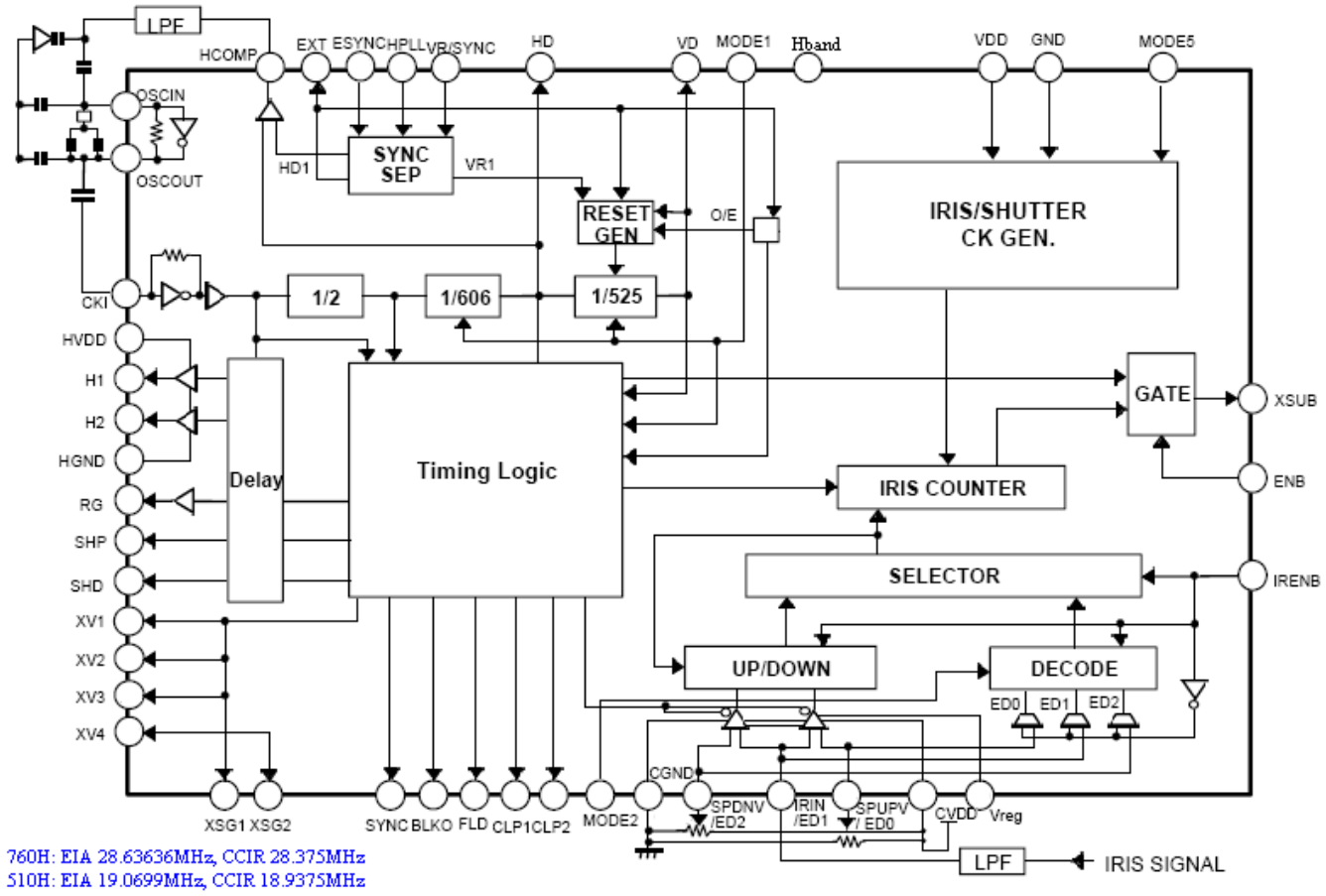


Block Diagram

CCD Signal Processor

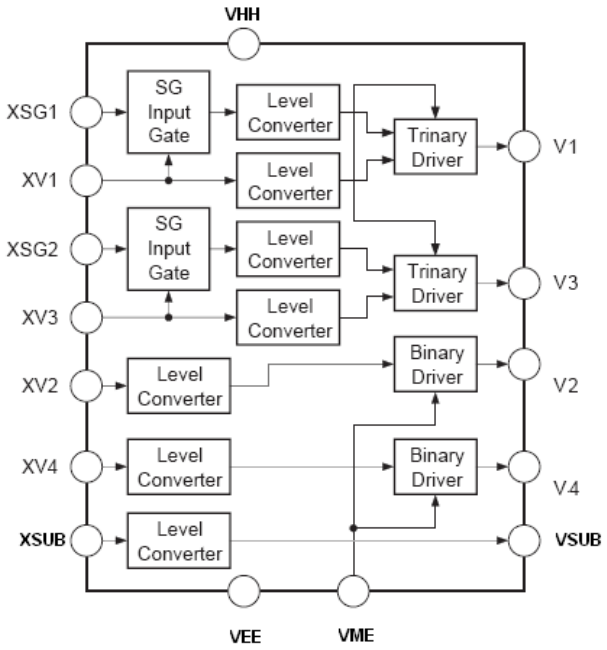


Timing Logic Controller

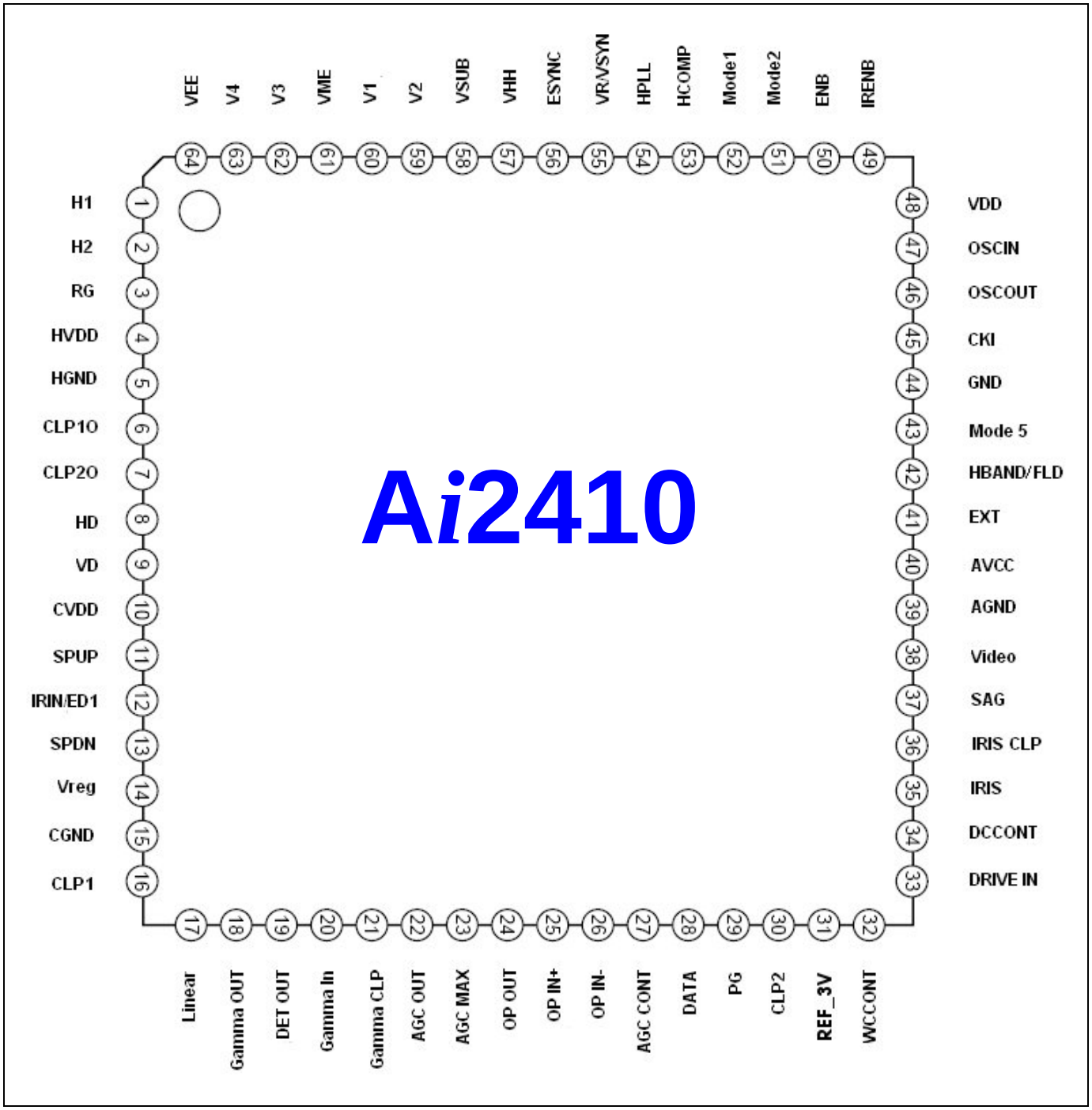


760H: EIA 28.63636MHz, CCIR 28.375MHz
510H: EIA 19.0699MHz, CCIR 18.9375MHz

Vertical Driver



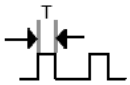
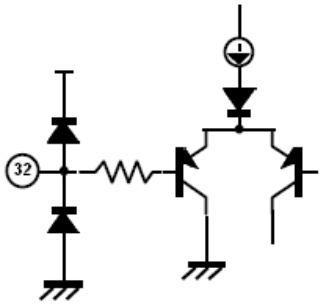
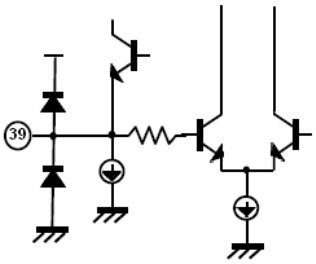
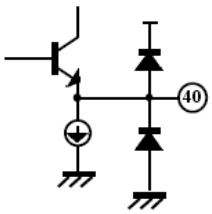
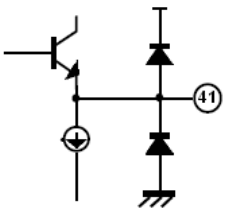
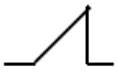
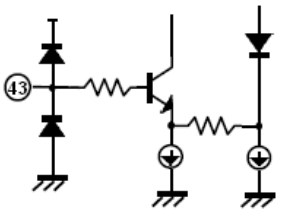
PIN Configuration

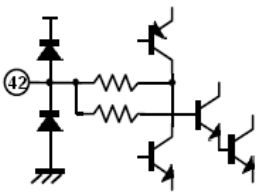
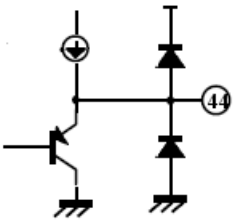
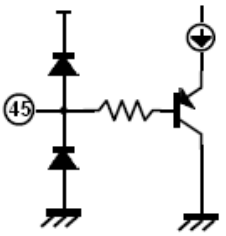
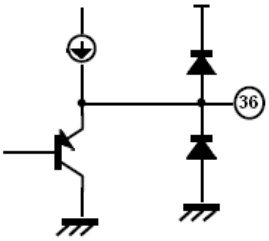
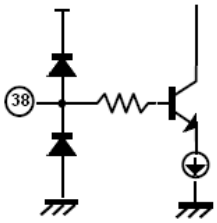
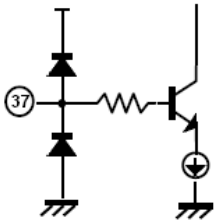


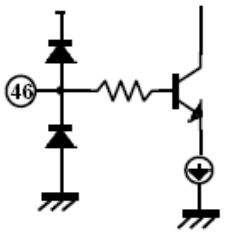
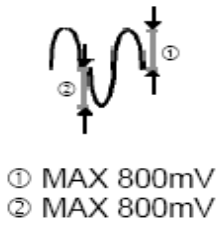
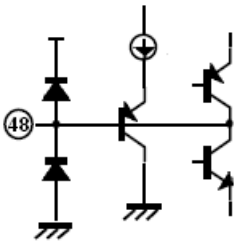
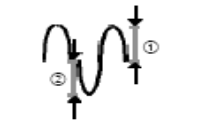
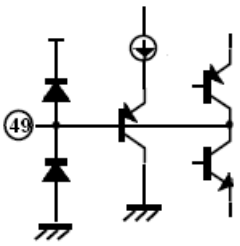
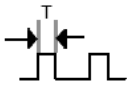
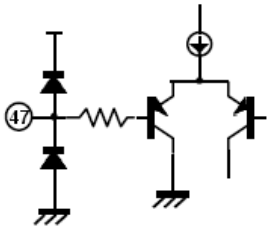
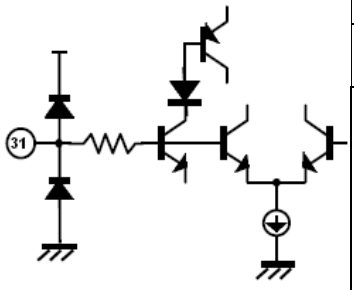
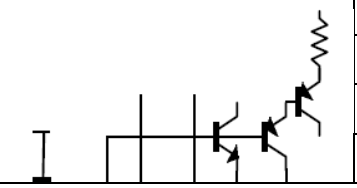
Pin Description

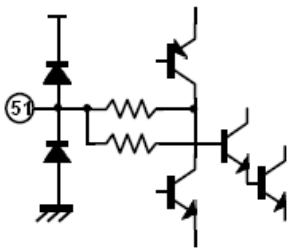
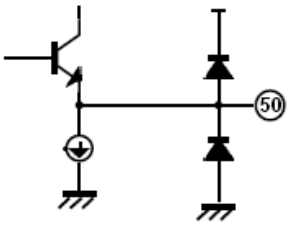
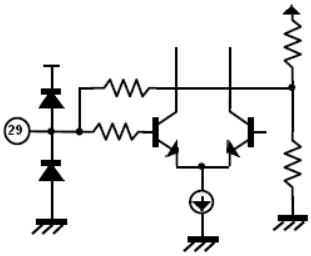
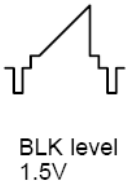
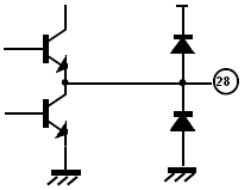
Timing Logic Controller			
No.	**Symbol**	**I/O**	**Description**
3	RG	O	Reset gate pulse output
6	CLP1O	O	Pulse output for clamp
7	CLP2O	O	Pulse output for clamp
8	HD	O	Horizontal drive output
9	VD	O	Vertical drive output
10	CVDD		Digital power supply
11	SPUP	I	Shutter speed up reference voltage/ shutter speed setting; strobe input in serial mode
12	IRIN/ED1	I	Iris signal input/shutter speed setting; clock input in serial mode
13	SPDN	I	Shutter speed down reference voltage/ shutter speed setting; data input in serial mode
14	Vreg	I	Bias current supply for comparator
15	CGND		Digital ground
41	EXT	O	External sync/internal sync identification signal High: external sync; Low: internal sync
42	HBAND	I	Selection pin for normal (510H) / high band (760H) support
43	Mode5	I	Low: Normal mode; High: Test mode (with pull-down resistance)
44	GND		Digital ground
45	CKI	I	Clock Input
46	OSCOUT	O	Oscillation (crystal oscillator) inverter output
47	OSCIN	I	Oscillation (crystal oscillator) inverter input
48	VDD		Power supply
49	IRENB	I	Low: Electronic Shutter mode; High: Auto iris mode (with pull-up resistance)
50	ENB	I	XSUB pulse ON/OFF control (with pull-up resistance) Low: XSUB pulse output stop; High: XSUB pulse output
51	Mode2	I	Electronic shutter speed input switchover (with pull-up resistance) Low: serial input; High: parallel input
52	Mode1	I	Low: EIA; High: CCIR (with pull-down resistance)
53	HCOMP	O	Comparator output (H phase comparator)
54	HPLL	I	Horizontal drive signal input (with pull-up resistance)
55	VR/VSYN	I	Vertical drive signal input/composite sync input (with pull-up resistance)
56	ESYNC	I	Low: SYNC sync or internal sync; High: VD/HD sync (with pull-down resistance)

CCD Signal Processor

No	Symbol	I/O	Specification	Equivalent Circuit	Description
16	CLP1	I	 HI : 4.5V and above LO : 0.5V and below T : 2us		Clamping input pin (active high)
17	Linear	O	 DC 1.8V Vcc		Linear signal output pin :in 8 output signal turn to γ 2 output
18	γ OUT	O	 DC 2V		Gamma compensation signal output pin γ_1 output when Pin 39 at open γ_2 output when Pin 39 at 5V
19	DET OUT	O	 MAX 1500mV TYP 500mV DC 2V		Output pin of AGC detection signal
20	γ IN	I	 Input DC permissible range *DC2 to 3V		Input pin of the gamma compensation circuit

21	γ CLP				Capacitor connecting pin for gamma input clamp
22	AGC OUT	O	 Vpp MAX 1300mV Vpp TYP 500mV DC 2.55V		Output pin of signal passed through AGC
23	AGC MAX	I	DC		Maximum gain setting pin of AGC amplifier
24	OP OUT	O			Output pin of operational amplifier
25	OP IN+	I			Non-inverted input pin of the operational amplifier (AGC detection signal input pin)
26	OP IN-	I			Inverted input pin of the operational amplifier

27	AGC CONT	I	DC		Gain control pin of AGC amplifier
28	DATA	I	 ① MAX 800mV ② MAX 800mV		CCD signal input pin
29	PG	I	 ① MAX 800mV ② MAX 800mV		CCD signal input pin
30	CLP2	I	 HI : 4.5V and above LO : 0.5V and below T : 2us		Clamping input pin (active high)
32	WCCONT	I	Input Voltage GND 2-3.5V		White clip level adjusting pin Preset mode Control mode
34	DCCONT	I	Input Voltage GND 2 – 3.5V Vcc		Dark clip level adjusting pin Preset mode 1 Control mode Preset mode 2

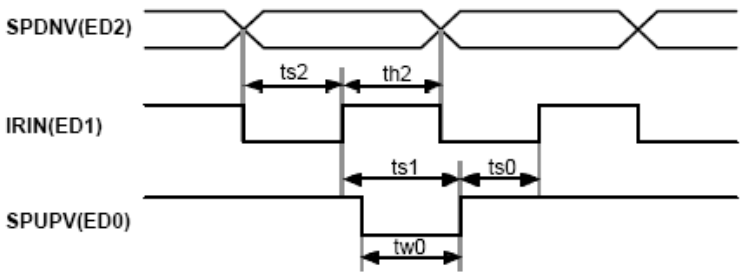
35	IRIS CLP				Capacitor connecting pin for IRIS output clamp
36	IRIS	O			Output pin of the IRIS control signal
37	SAG	I			Input pin of SAG compensation signal. AC couple from output Pin28 Video through external capacitor
38	Video	O			VIDEO signal output pin
39	AGND		Analog ground of CCD signal processor		
40	AVCC		Analog supply of CCD signal processor		
42	HBand/FLD	O	Digital Output 0-5V		Field identification signal output (High: odd field; Low: even field)
31	REF_3V	-	3V reference voltage		Normally leave it open or supply 3V externally.

Vertical Driver

No	Symbol	I/O	Description
1	H1	O	H1 clock output for CCD horizontal register drive
2	H2	O	H2 clock output for CCD horizontal register drive
4	HVDD		Power supply for H1 and H2
5	HGND		GND for H1 and H2
57	VHH		Power supply (+15V)
58	VSUB	O	Output control (VSUB)
59	V2	O	Output control ($V_{\phi 2}$)
60	V1	O	Output control ($V_{\phi 1}$)
61	VME		Power supply (0V)
62	V3	O	Output control ($V_{\phi 3}$)
63	V4	O	Output control ($V_{\phi 4}$)
64	VEE		Power supply (-8.5V)

Electrical Characteristics (V_{cc} =5V, T_a =25^oC)

Timing Logic Controller						
DC Characteristic						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Supply Voltage	V_{DD}		4.75	5.0	5.25	V
Input Voltage	V_{IH} V_{IL}		0.7 V_{DD}		0.3V_{DD}	V V
Output voltage 1: All output pins except those below)	V_{OH1} V_{OL1}	I_{OH} =-2mA I_{OL} =4mA	V_{DD} -0.8		 0.4	V V
Output voltage 2: Pin 6 (RG) and Pin 8 (HCOMP)	V_{OH2} V_{OL2}	I_{OH} =-8mA I_{OL} =8mA	V_{DD} -0.8		 0.4	V V
Output voltage 3: Pin 62 (H2) and Pin 63 (H1)	V_{OH3} V_{OL3}	I_{OH} =-12mA I_{OL} =12mA	V_{DD} -0.8		 0.4	V V
Output voltage 4: Pin 3 (OSCOUT)	V_{OH4} V_{OL4}	I_{OH} =-1mA I_{OL} =1mA	V_{DD} /2		 0.4	V V
Feedback resistance	R_{FB}	V_{IN} =GND or V_{DD}	250k	1M	2.5M	Ω
Pull-up current	I_{PU}	V_{IL} =0V	-80			μA
Pull-down current	I_{PD}	V_{IH} =V_{DD}	40			μA
Current consumption	I_{DD}	V_{DD} =5V Normal operating state		28		mA
AC Characteristic						



SYMBOL	Condition	Min.	Max.
ts2	SPDNV (ED2) setup time for IRIN (ED1) rise	20ns	-
th2	SPDNV (ED2) hold time for IRIN (ED1) rise	20ns	-

ts1	IRIN (ED1) setup time for SPUPV (ED0) rise	20ns	-
tw0	SPUPV (ED0) pulse width	20ns	50 μs
ts0	SPUPV (ED0) setup time for IRIN (ED1) rise	20ns	-

CCD Signal Processor

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
AGC Gain	AGC dynamic range	-4		32	dB
	AGC MAX = 4V, AGC CONT = 1.5V and				
	DATA IN = 100mV		18	20	dB
	AGC CONT = 5V and DATA IN = 500mV		-4	-1	dB
	AGC CONT = 1.5V and DATA IN = 30mV	30	32		dB
	AGC CONT = 3.55V and DATA IN = 320mV	8	10	12	dB
AGC OUT	DC output level of AGC OUT	2.25	2.55	2.85	V
γ_1	γ IN=500mV	530	630	730	mV
γ_2	γ IN=500mV	580	680	780	mV
Linear Gain	Gain between γ IN and Linear	1.5	2.6	3.5	dB
	γ IN =500mV				
DET OUT	DC output level of DET OUT	1.8	2.0	2.2	V
IRIS	DC output level of IRIS	1.1	1.3	1.5	V
	Gain between DATA Input and IRIS:				
	DATA input = 300mV	8	10	12	dB
Video Driver	Gain between DRIVE IN and VIDEO:				
	DRIVE IN = 700mV	5.7	6.0	6.3	dB
SYNC Level		270	293	316	mV
Dark Clip	Preset mode 1	-15	0	15	mV
	Preset mode 2	0	20	40	mV
	DC CONT = 2V		3	5	mV
	DC CONT = 3.3V	80	130		mV
White Clip	DRIVER IN = 1500mV				
	WC CONT = GND	780	820	860	mV
	WC CONT = 2.2V		300	600	mV
	WC CONT = 3.3V	1000	1300		mV
Opamp	DC output level of OP OUT				
	OP IN+ = 2.5V and OP IN- = 4V		0.8	1.2	V
	OP IN+ = 4V and OP IN- = 2.5V	4.5	4.8		V

Vertical Driver

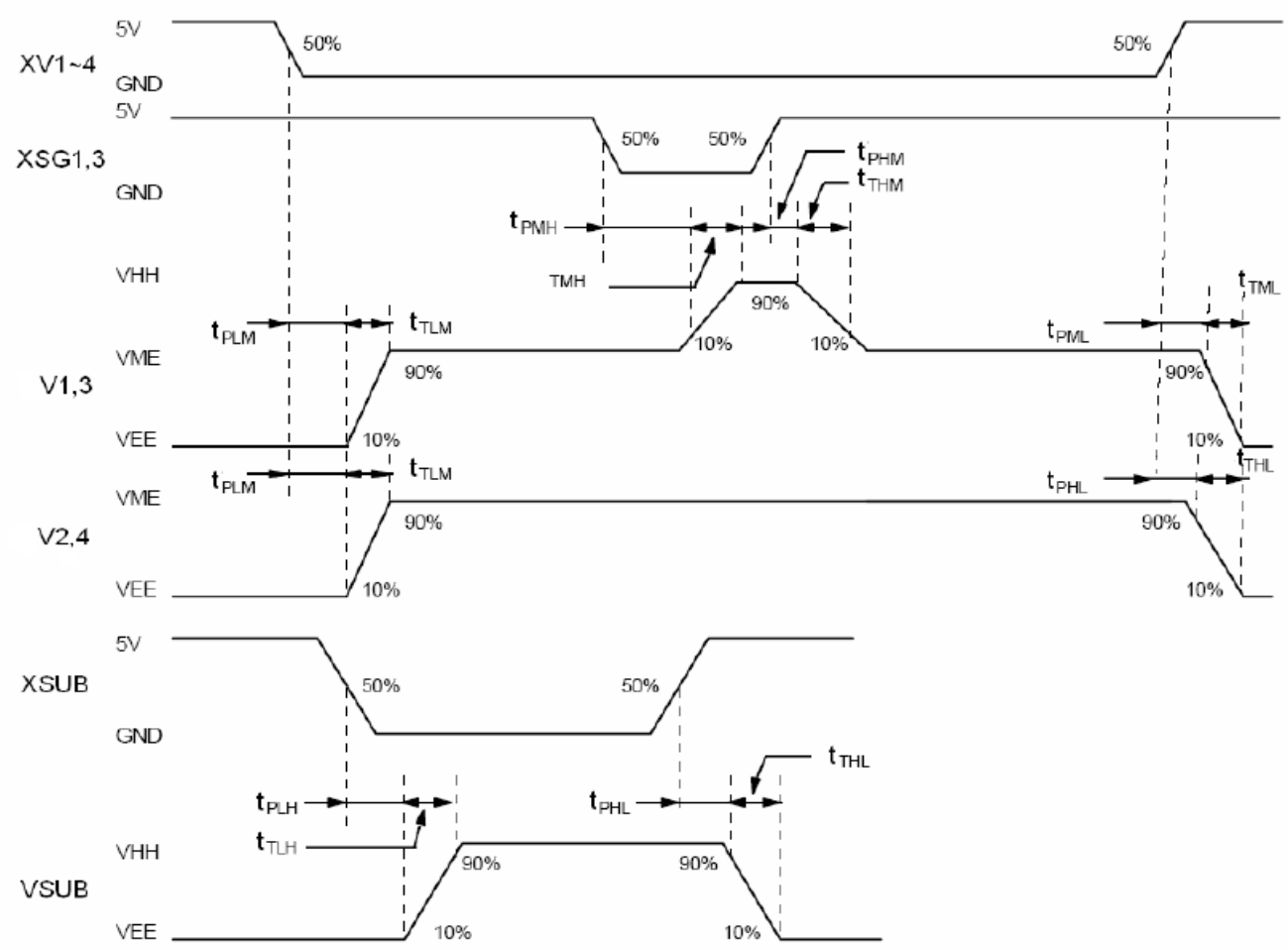
DC Characteristic

Description	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{P1}		14.5	15	15.5	V
	V_{SS}		-9.5	-8.5	-7.5	V
Operation Current	I_{P1}	Shutter speed: 1/100000s		2.0	3.5	mA
	I_{P0}	Shutter speed: 1/100000s		4.5	5.0	mA
	I_{SS}	Shutter speed: 1/100000s	-8.5	-6.5		mA
Output Current	I_{OL}	V1-4 = -8V	25	37		mA
	I_{OM1}	V1-4 = -0.5V		-15	-10	mA
	I_{OM2}	V1,3= 0.5V	9	13.5		mA
	I_{OH}	V1,3 = 14.5V		-18	-12	mA
	I_{OSL}	VSUB = -8.5V	12	18		mA
	I_{OSH}	VSUB = 14.5V		-10.5	-7	mA

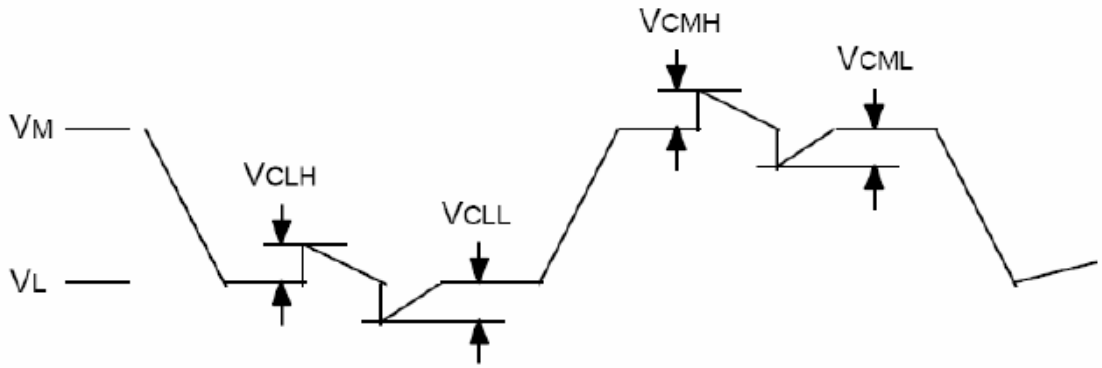
AC Characteristic (V_{P1} = 15V, V_{P0} =GND, V_{SS} =-8.5V and T_a =25 ^oC

Description	Symbol	Condition	Min.	Typ.	Max.	Unit
Delay Time	T_{PLM}	No Load	10	40	70	ns
	T_{PMH}	No Load	10	30	70	ns
	T_{PLH}	No Load	10	40	100	ns
	T_{PML}	No Load	10	100	200	ns
	T_{PHM}	No Load	10	100	180	ns
	T_{PHL}	No Load	10	60	100	ns
Rising Time	T_{PLM}	$V_{SS} \rightarrow V_{P0}$	400	700	930	ns
	T_{PMH}	$V_{P0} \rightarrow V_{P1}$	400	650	930	ns
	T_{PLH}	$V_{SS} \rightarrow V_{P1}$	10	50	100	ns
	T_{PML}	$V_{P0} \rightarrow V_{SS}$	200	300	500	ns
	T_{PHM}	$V_{P1} \rightarrow V_{P0}$	400	600	820	ns
	T_{PHL}	$V_{P1} \rightarrow V_{P0}$	10	50	100	ns
Output Noise	V_{CLH} ,V_{CLL} V_{CMH} ,V_{CML}				0.5	V

Timing Diagram



Noise Coupling Diagram



External Synchronization

1. External/Internal Sync Selection

External or internal synchronization is selected automatically by a combination of 3 pins (VR/SYNC, HPLL and ESYNC) to which the sync signal is input externally. The table below shows the input pattern combinations.

Input pattern	**VR/SYNC pin: SYNC signal** **HPLL pin : Open** **ESYNC pin : Open**	**VR/SYNC pin: VD signal** **HPLL pin : HD signal** **ESYNC pin : V_{DD}**	**VR/SYNC pin: SYNC signal** **HPLL pin : Open** **ESYNC pin : Open**
EXT pin Output	High	High	Low
Sync state	External sync	External sync	Internal sync

Note) Operation is possible even if the VD cycle of the VD input in the VD/HD sync mode is longer than normal.

The EXT pin is the external/internal sync identification signal output pin. This output signal can be used as the signal to select LC oscillation for expanding the lock range for external synchronization or the oscillator for improving the oscillation accuracy for internal synchronization.

2. Reset Operation

SYNC synchronization

The VR1 signal component is extracted from the SYNC signal supplied externally and, for EIA,V reset is performed so that the VD pulse falls at the count of 259H (262.5-3.5H) from the fall of the VR1 pulse. For CCIR, it is reset in such a way that the VD pulse falls at the count of 309H(312.5-3.5H).For these reasons, it is a prerequisite that the SYNC signal input comply with the EIA or CCIR standard.

VD/HD synchronization

V reset is performed so that the VD pulse 1H later after detecting the fall of the VD(VDR) pulse supplied externally. Therefore, this enables V reset operation regardless of the field line number. The phase difference between the VDRpulse and HD pulse which is locked horizontally at PLL circuit identifies whether the field is odd or even. (VDR must have a pulse width of 2H or more.)

Electronic Shutter/Auto IRIS

By setting the ENB(Pin 7) high, the XSUB pulse is output for a specific period to activate the electronic shutter and auto iris.

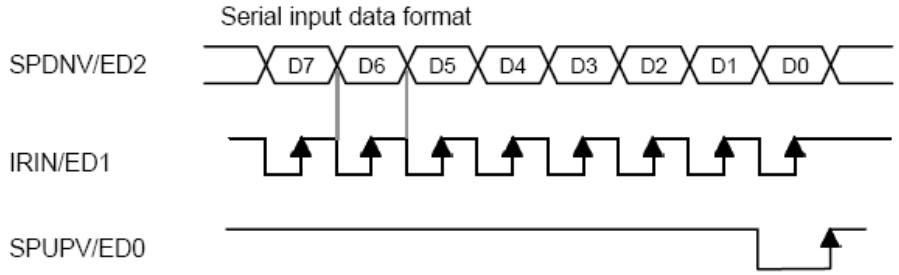
1. Auto Iris (IRENB=high, MODE2=any level)

No	Symbol	Function
25	IRIN/ED1	Iris signal input
23	SPDN/ED2	Shutter speed down reference voltage
24	SPUP/ED0	Shutter speed up reference voltage

2. Parallel input electronic shutter (IRENB=low, MODE2=high)

No	Symbol	Function							
23	SPDN/ED2	H	H	H	H	L	L	L	L
25	IRIN/ED1	H	H	L	L	H	H	L	L
24	SPUP/ED0	H	L	H	L	H	L	H	L
Shutter speed		EIA: 1/100 CCIR: 1/120	1/250	1/500	1/1000	1/2000	1/5000	1/10000	1/100000

3. Serial input electronic shutter (IRENB=low, MODE2=high)



The ED2 data is latched in the register at the ED1 rise, and retrieved internally at the ED0 rise.

Typical shutter speed

EIA		CCIR	
Load value	Shutter speed	Load value	Shutter speed
00h	1/100000	00h	1/80000
4Eh	1/10000	4Ah	1/10000
6Ah	1/5000	65h	1/5000
87h	1/2000	82h	1/2000
9Ch	1/1000	97h	1/1000
ACh	1/500	A7h	1/500
CAh	1/250	C5h	1/250
EDh	1/100	E1h	1/120

Mode Control

No.	Symbol	I/O	Low	High	Remarks
7	ENB	I	XSUB stop	XSUB output	
20	IRENB	I	Electronic shutter	Auto iris	Valid only when ENB is high
16	MODE2	I	Serial input	Parallel input	Valid only when ENB is high and IRENB is low
25	IRIN/ED1	I	Auto iris control signal input pin (IRENB = high)		Valid only when ENB is high
23	SPDN/ED2	I	Shutter speed setting pin (IRENB = low)		
24	SPUP/ED0	I			
15	MODE1	I	EIA	CCIR	
11	HPLL	I	Internal sync: HPLL (open) VR/SYNC (open) SYNC sync: HPLL (open)		
10	VR/SYNC	I	VR/SYNC (SYNC input) VD/HD sync: HPLL (HD input) VR/SYNC (VD input)		
9	ESYNC	I	SYNC sync Internal sync	VD/HD sync	
12	EXT	O	Internal sync	External sync	Switchover between internal and external sync is automatically identified by input state at Pin 9, 10 and 11

Mode Tables

1. Internal sync mode

	Interlace	
	Field readout	**Frame readout**
XSUB pulse OFF[1]	O	O
Electronic shutter ON	O	O
Auto iris ON	O	O

1 EIA for 1/60 s accumulation; CCIR for 1/50 s accumulation O: Can be used

2. SYNC sync (external sync) mode

	Interlace	
	Field readout	**Frame readout**
XSUB pulse OFF[1]	O	O
Electronic shutter ON	O	O
Auto iris ON	O	O

1 EIA for 1/60 s accumulation; CCIR for 1/50 s accumulation O: Can be used

3. VD/HC sync (external sync) mode

	VD input with normal cycle		VD input with longer cycle than normal interlace	
	Interlace			
	Field readout	Frame readout	Field readout	Frame readout
XSUB pulse OFF[1]	O	O	O	X
Serial input electronic shutter ON	O	O	X	X
Parallel input electronic shutter ON	O	O	X	X
Auto iris ON	O	O	X	X

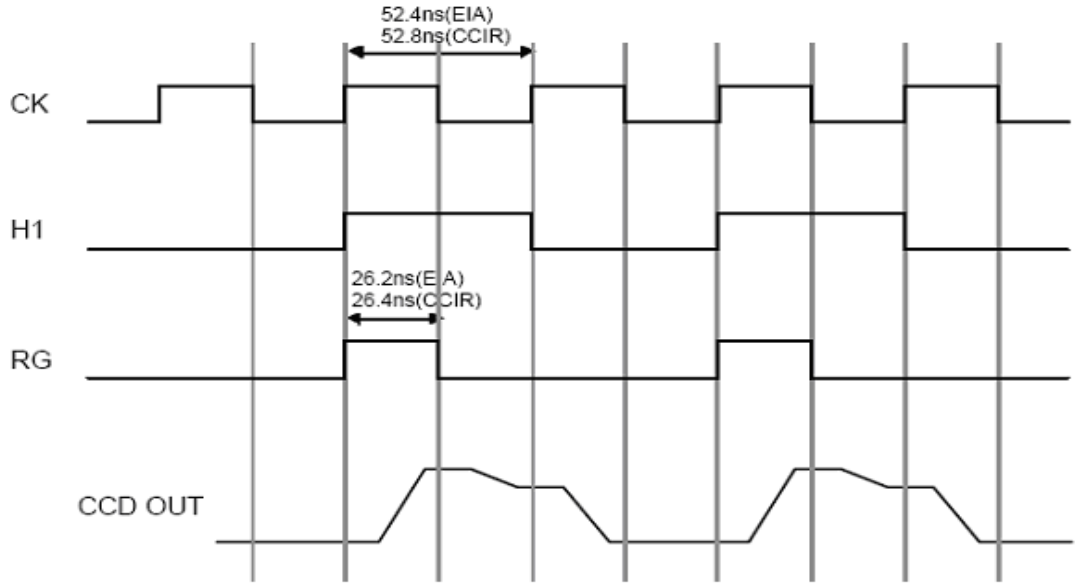
1 EIA for 1/60 s accumulation; CCIR for 1/50 s accumulation O: Can be used

X: Cannot be used

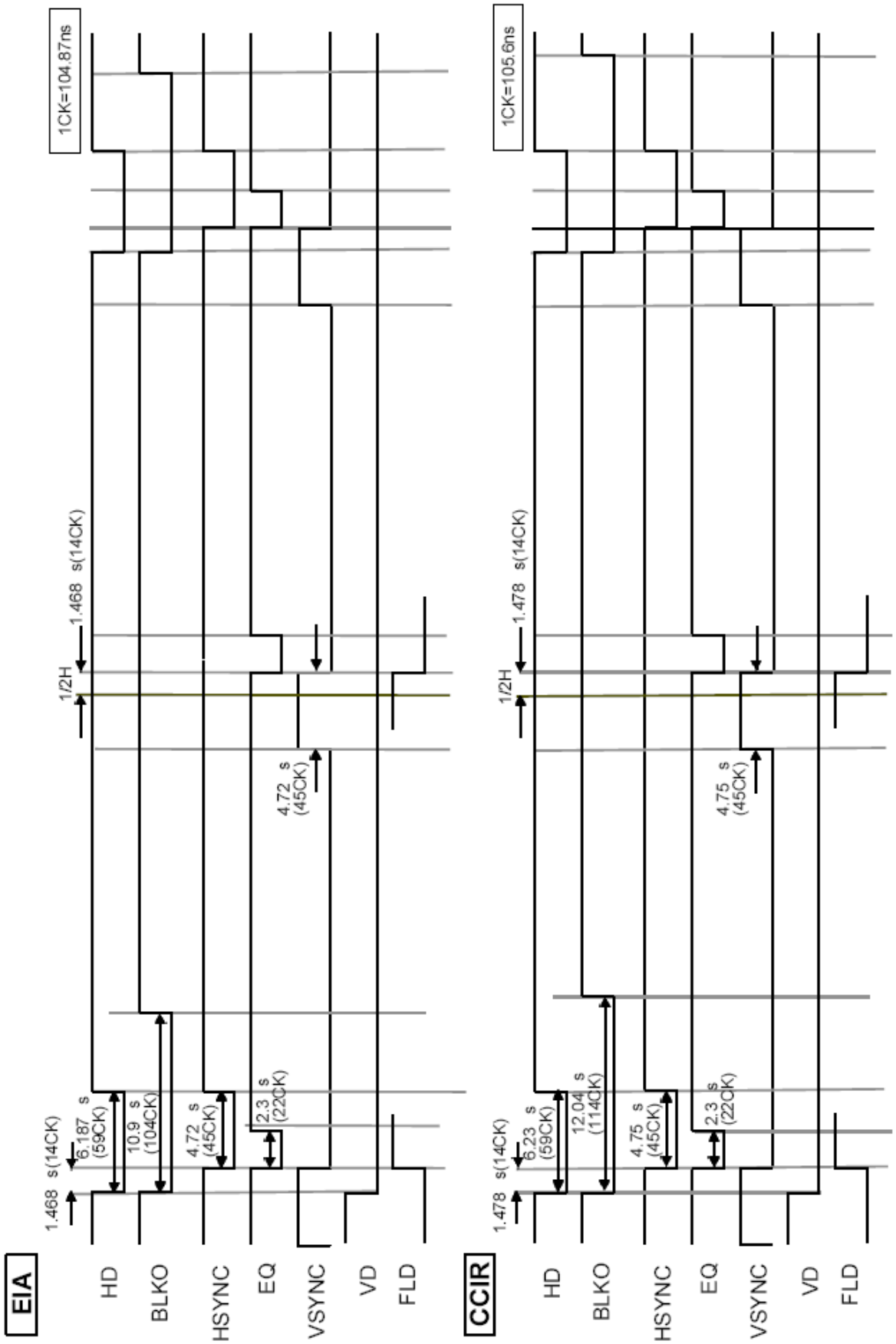
Note Only in the VD/HD sync mode, the external synchronization is possible during which VD pulses with longer cycle than normal are input to the VR/SYNC pin

Timing Diagram 1: CCD Readout

EIA/CCIR

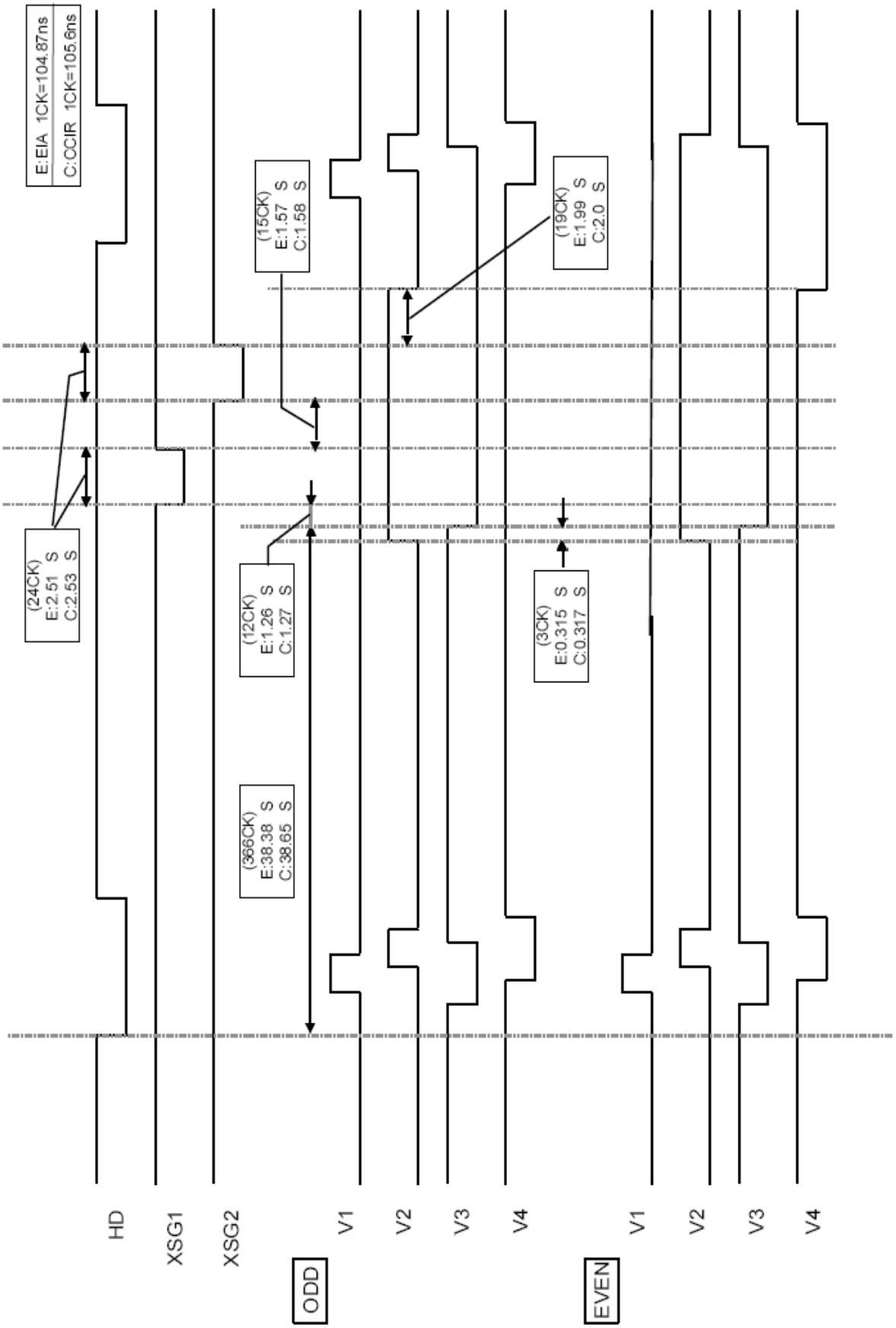


Timing Diagram 2: Horizontal Effective Period



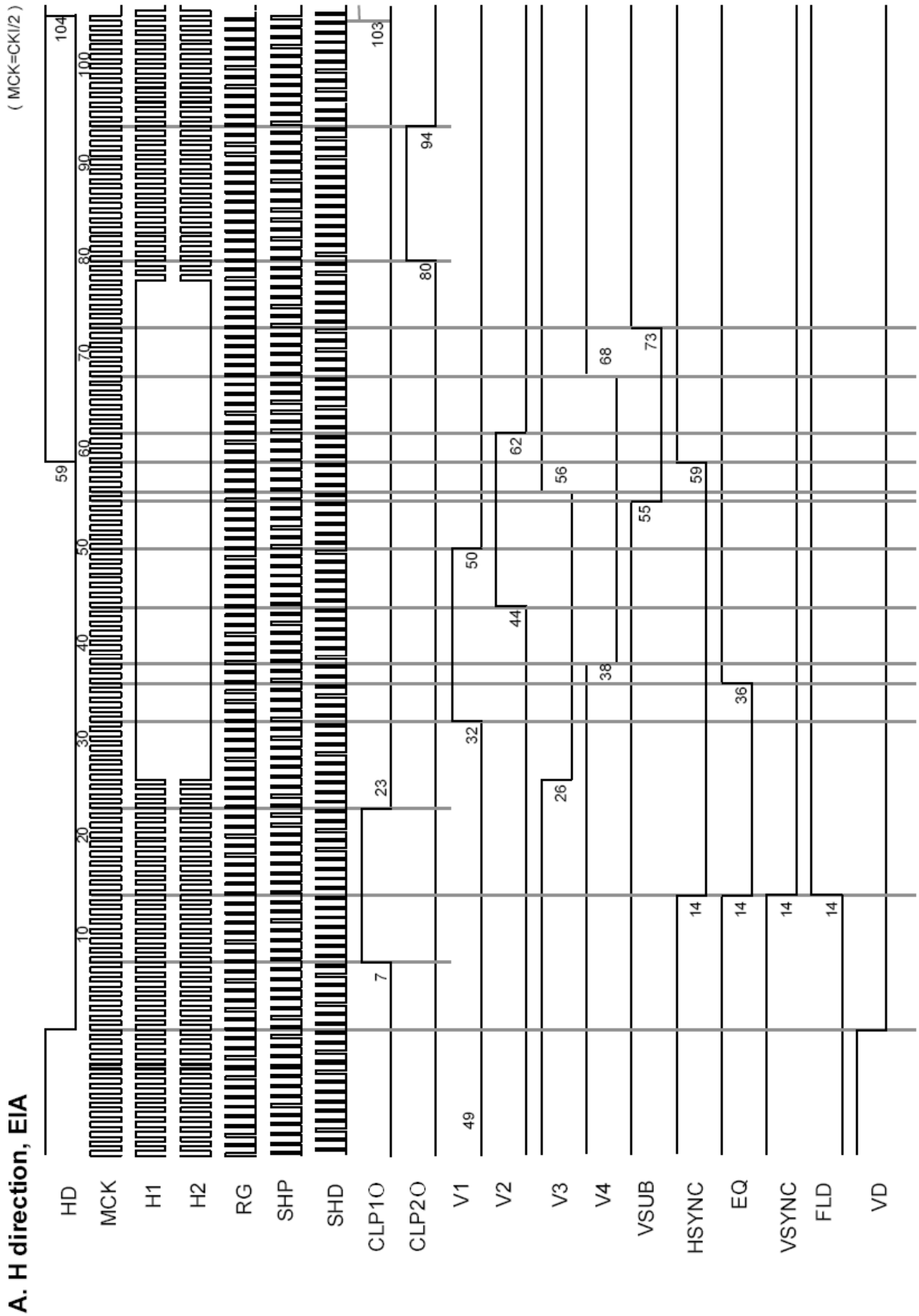
Timing Diagram 3: Charge Readout Timing

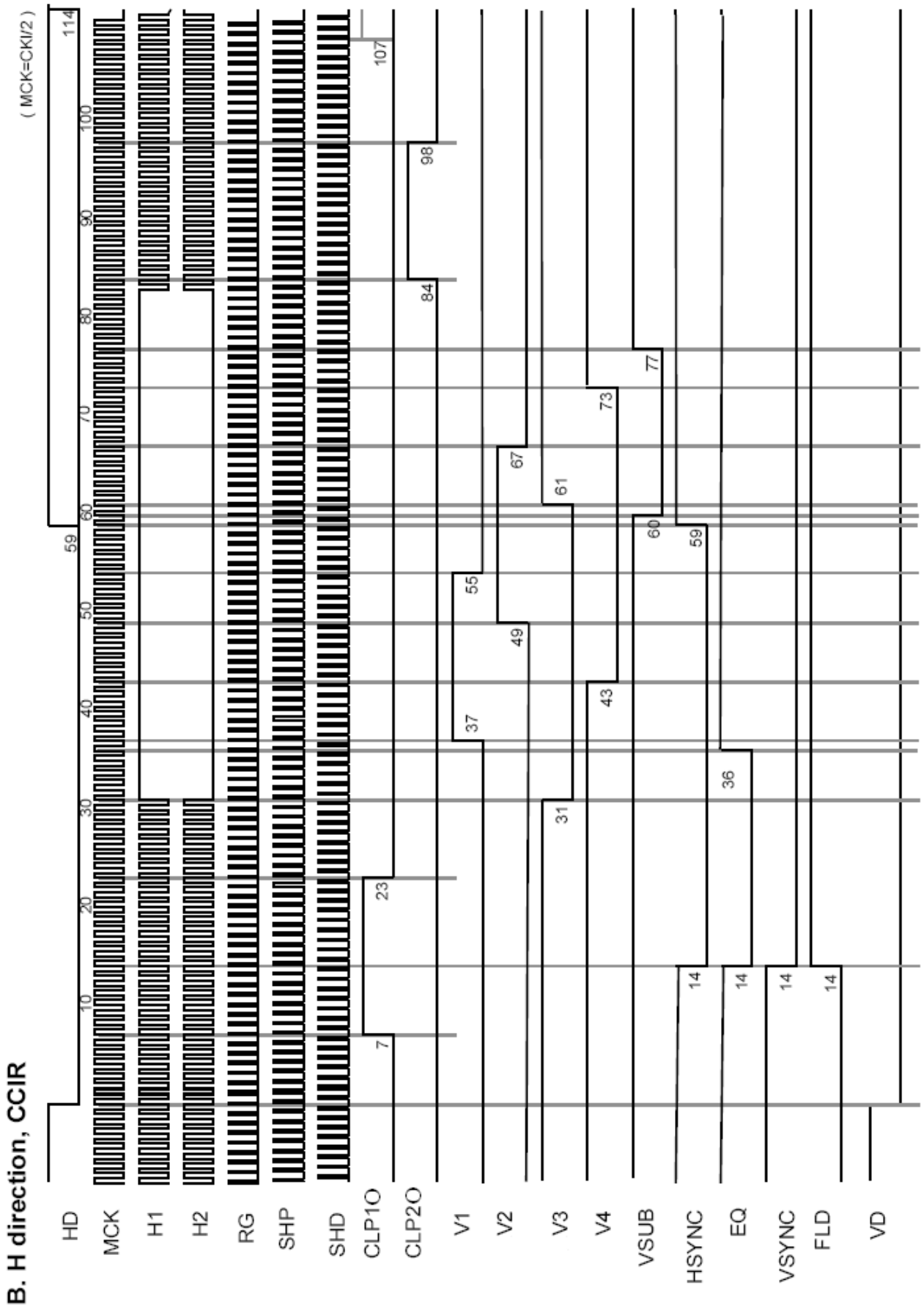
Field accumulation



Timing Diagram 4

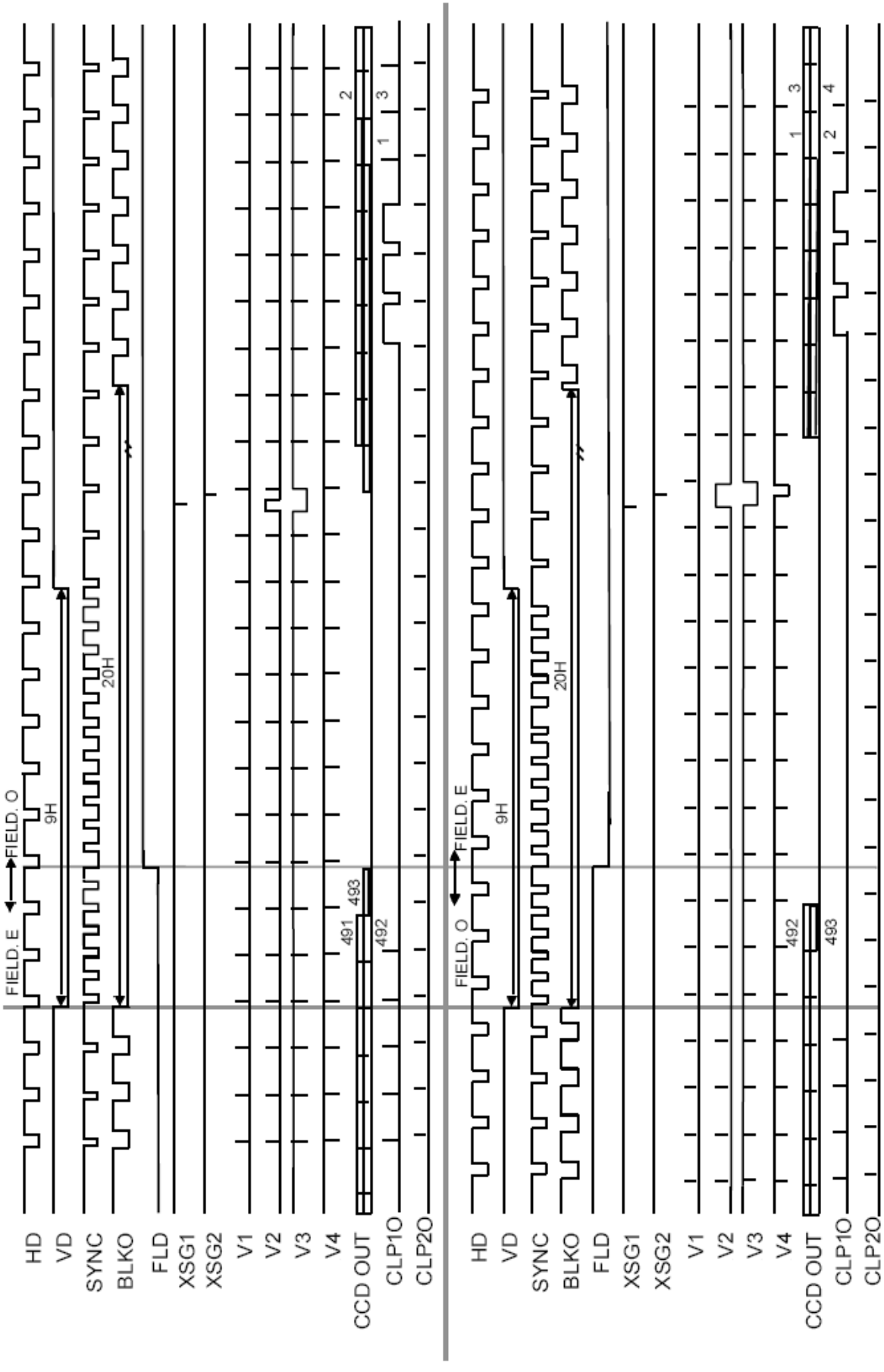
A. H direction, EIA



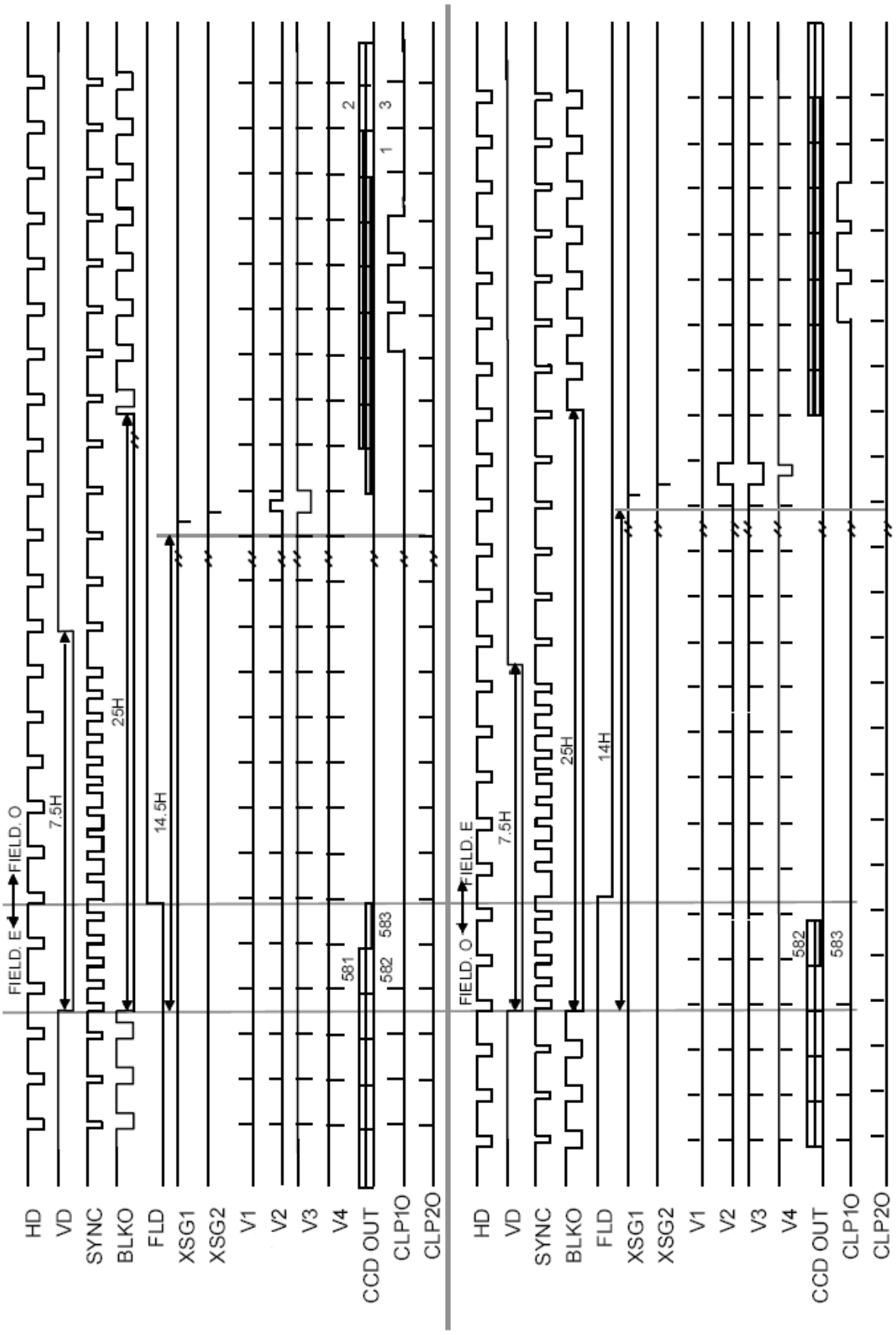

B. H direction, CCIR
(MCK=CKI/2)
HD
MCK
H1
H2
RG
SHP
SHD
CLP1O
CLP2O
V1
V2
V3
V4
VSUB
HSYNC
EQ
VSYNC
FLD
VD
114
59
7
23
107
98
84
55
37
67
49
61
31
73
43
77
60
59
14
36
14
14
14

Timing Diagram 5: Vertical Synchronization

A. V direction, EIA

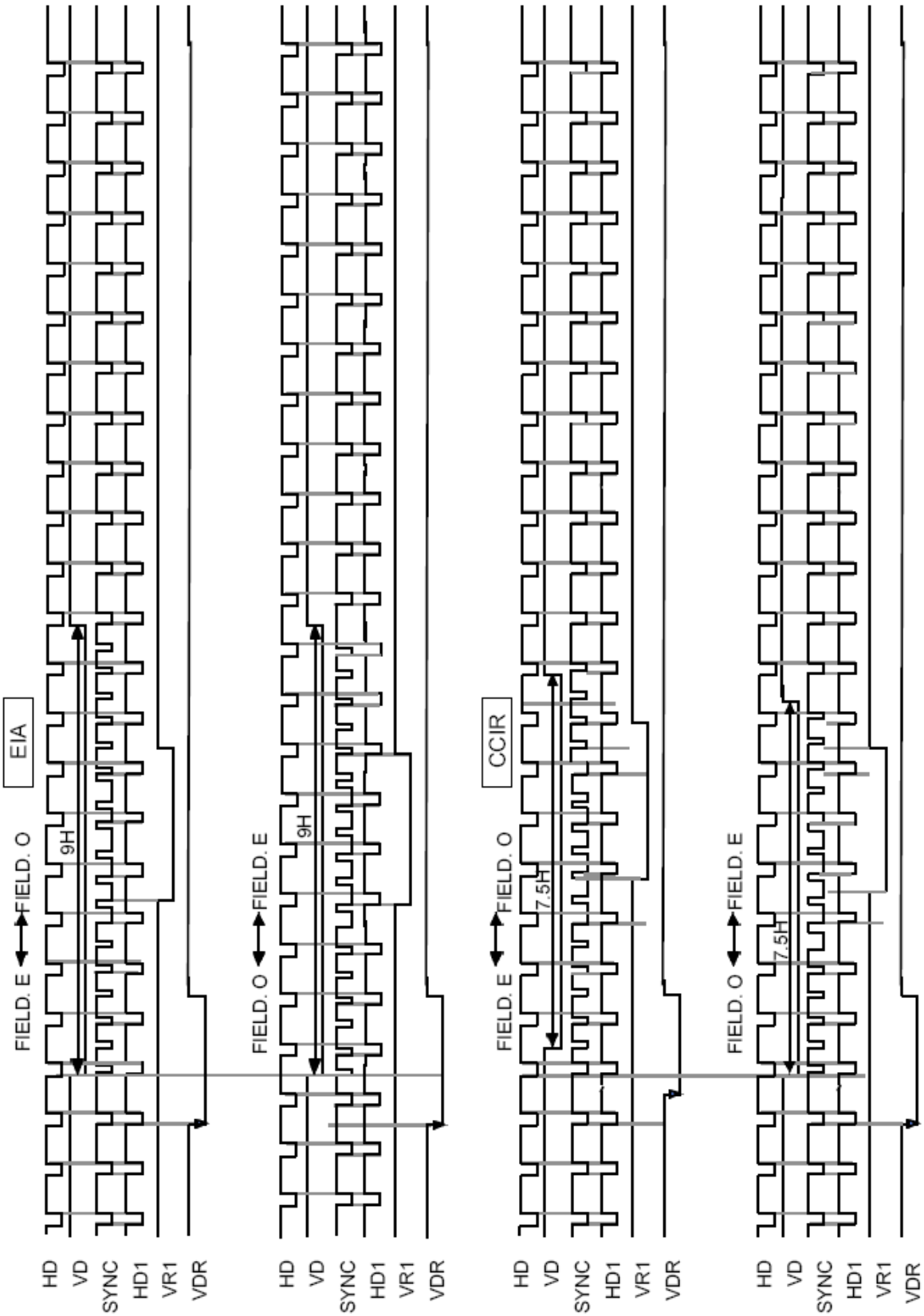


B. V direction, CCIR



Timing Diagram 6: External Synchronization Reset Operation

External Synchronization reset Operation



REVISION HISTORY

Revision	Description	Date
V1.0	Preliminary Release	9 May 2008