

# 4V Drive Pch+Pch MOS FET

## SP8J5

**●Structure**

Silicon P-channel MOS FET

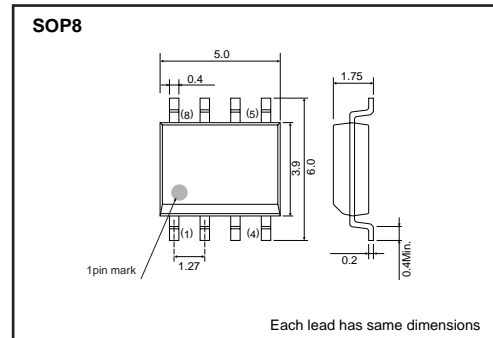
**●Features**

- 1) Low On-resistance. (25mΩ at 4.5V)
- 2) High Power Package. (PD=2.0W)
- 3) High speed switching.
- 4) Low voltage drive. (4V)

**●Applications**

Power switching, DC-DC converter

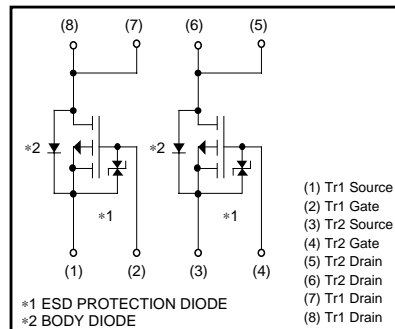
**●External dimensions (Unit : mm)**



**●Packaging specifications**

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SP8J5		○

**●Inner circuit**



**●Absolute maximum ratings (Ta=25°C)**

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V <sub>DSS</sub>	-30	V	
Gate-source voltage	V <sub>GSS</sub>	±20	V	
Drain current	Continuous	I <sub>D</sub>	±7.0	A
	Pulsed	I <sub>DP</sub> *1	±28	A
Source current (Body diode)	Continuous	I <sub>S</sub>	-1.6	A
	Pulsed	I <sub>SP</sub> *1	-28	A
Total power dissipation	P <sub>D</sub> *2	2.0	W	
Channel temperature	T <sub>ch</sub>	150	°C	
Range of Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

\*1 Pw≤10μs, Duty cycle≤1%  
 \*2 Mounted on a ceramic board

**●Thermal resistance**

Parameter	Symbol	Limits	Unit
Channel to ambient	R <sub>th(ch-a)</sub> *	62.5	°C / W

\* Mounted on a ceramic board.

## Transistors

## ●Electrical characteristics (Ta=25°C)

&lt;It is the same characteristics for Tr1 and Tr2.&gt;

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	±10	μA	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	–30	–	–	V	I <sub>D</sub> = –1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	–1	μA	V <sub>DS</sub> = –30V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS(th)</sub>	–1.0	–	–2.5	V	V <sub>DS</sub> = –10V, I <sub>D</sub> = –1mA
Static drain-source on-state resistance	R <sub>DS(on)</sub> *	–	20	28	mΩ	I <sub>D</sub> = –7A, V <sub>GS</sub> = –10V
		–	25	35	mΩ	I <sub>D</sub> = –3.5A, V <sub>GS</sub> = –4.5V
		–	30	42	mΩ	I <sub>D</sub> = –3.5A, V <sub>GS</sub> = –4.0V
Forward transfer admittance	Y <sub>fs</sub>   *	6.0	–	–	S	V <sub>DS</sub> = –10V, I <sub>D</sub> = –3.5A
Input capacitance	C <sub>iss</sub>	–	2600	–	pF	V <sub>DS</sub> = –10V
Output capacitance	C <sub>oss</sub>	–	450	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	350	–	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	–	20	–	ns	I <sub>D</sub> = –3.5A
Rise time	t <sub>r</sub> *	–	50	–	ns	V <sub>DD</sub> ≐ –15V
Turn-off delay time	t <sub>d(off)</sub> *	–	110	–	ns	V <sub>GS</sub> = –10V
Fall time	t <sub>f</sub> *	–	70	–	ns	R <sub>L</sub> =4.3Ω
Total gate charge	Q <sub>g</sub> *	–	25	–	nC	R <sub>G</sub> =10Ω
Gate-source charge	Q <sub>gs</sub> *	–	5.5	–	nC	V <sub>DD</sub> ≐ –15V
Gate-drain charge	Q <sub>gd</sub> *	–	10	–	nC	V <sub>GS</sub> = –5V
						I <sub>D</sub> = –7A

\*Pulsed

## ●Body diode characteristics (Source-drain) (Ta=25°C)

&lt;It is the same characteristics for Tr1 and Tr2.&gt;

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub>	–	–	–1.2	V	I <sub>S</sub> = –1.6A, V <sub>GS</sub> =0V

Transistors

●Electrical characteristic curves

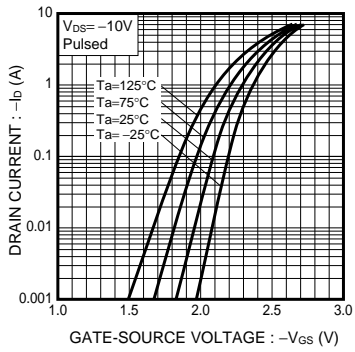


Fig.1 Typical Transfer Characteristics

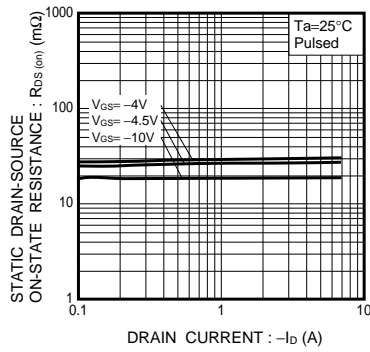


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

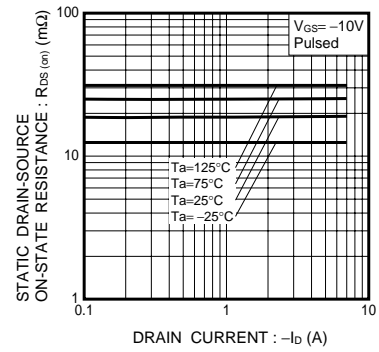


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

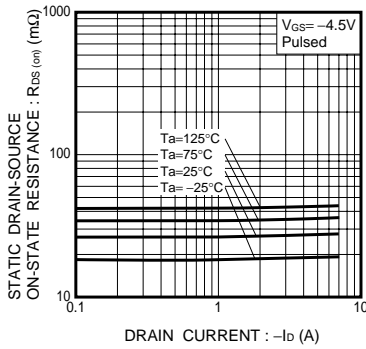


Fig.4 Static Drain-Source On-State vs. Drain Current

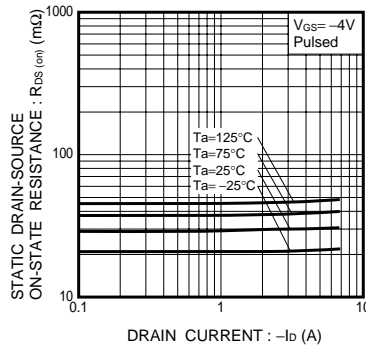


Fig.5 Static Drain-Source On-State vs. Drain Current

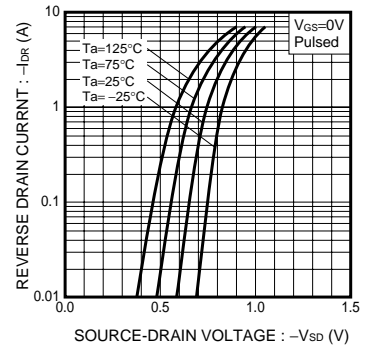


Fig.6 Reverse Drain Current Source-Drain Current

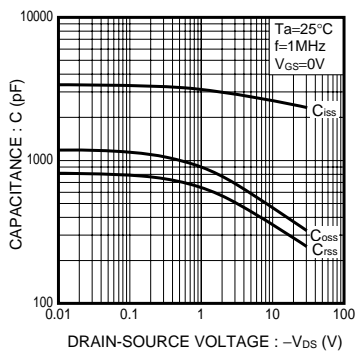


Fig.7 Typical Capacitance vs. Drain-Source Voltage

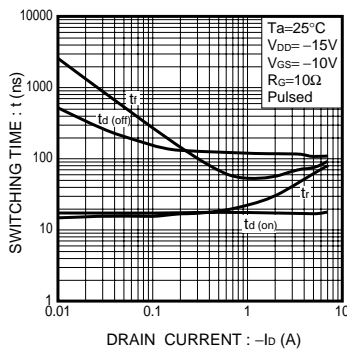


Fig.8 Switching Characteristics

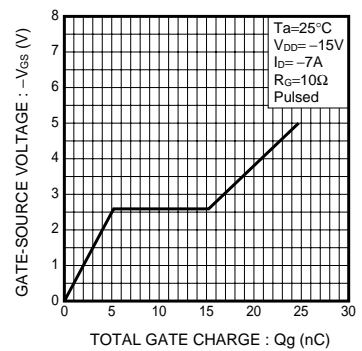


Fig.9 Dynamic Input Characteristics

Transistors

●Measurement circuits

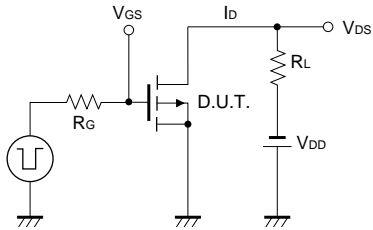


Fig.10 Switching Time Test Circuit

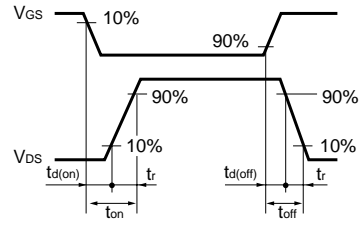


Fig.11 Switching Time Waveforms

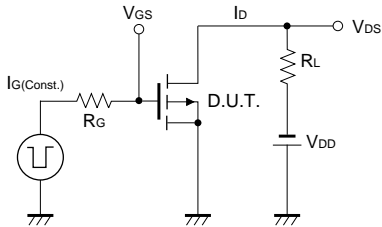


Fig.12 Gate Charge Test Circuit

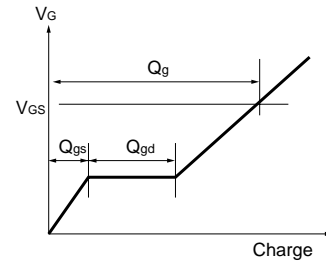


Fig.13 Gate Charge Waveform

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