

AOD4142
N-Channel SDMOS™ POWER Transistor
General Description

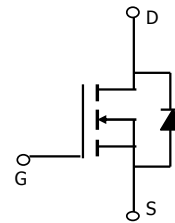
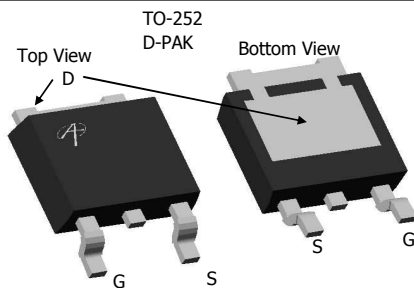
The AOD4142 is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

- RoHS Compliant
- Halogen Free*

Features

$V_{DS} (V) = 25V$
 $I_D = 50A$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 5.3m\Omega$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 9.8m\Omega$ ($V_{GS} = 4.5V$)

100% UIS Tested!
100% R_g Tested!


Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	50	A
$T_C=25^\circ C$		43	
Pulsed Drain Current ^C	I_{DM}	120	
Continuous Drain Current ^A	I_{DSM}	17	
$T_A=25^\circ C$		13	
Avalanche Current ^C	I_{AR}	50	
Repetitive avalanche energy $L=50\mu H$ ^C	E_{AR}	63	mJ
Power Dissipation ^B	P_D	50	W
		$T_C=25^\circ C$	
Power Dissipation ^A	P_{DSM}	2.5	W
		$T_A=25^\circ C$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	15	20	$^\circ C/W$
$t \leq 10s$		41	50	
Maximum Junction-to-Ambient ^A	$R_{\theta JC}$	2.1	3	$^\circ C/W$
Steady-State		2.1	3	

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	25			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			10 50	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.2	2	2.5	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	120			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=30\text{A}$		4.4	5.3	$\text{m}\Omega$
		$T_J=125^\circ\text{C}$		6.6	7.9	
		$V_{GS}=4.5\text{V}$, $I_D=20\text{A}$		7.8	9.8	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=30\text{A}$		65		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current ^G				50	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=12.5\text{V}$, $f=1\text{MHz}$	1440	1800	2160	pF
C_{oss}	Output Capacitance		310	445	580	pF
C_{riss}	Reverse Transfer Capacitance		170	285	400	pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	0.8	1.6	2.4	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=12.5\text{V}$, $I_D=30\text{A}$	25	31	37	nC
$Q_g(4.5\text{V})$	Total Gate Charge		12	15	18	nC
Q_{gs}	Gate Source Charge		4	4.8	6	nC
Q_{gd}	Gate Drain Charge		5.3	8.9	13	nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=12.5\text{V}$, $R_L=0.42\Omega$, $R_{GEN}=3\Omega$		8		ns
t_r	Turn-On Rise Time			10.4		ns
$t_{D(off)}$	Turn-Off DelayTime			29		ns
t_f	Turn-Off Fall Time			9		ns
t_{rr}	Body Diode Reverse Recovery Time		$I_F=30\text{A}$, $di/dt=500\text{A}/\mu\text{s}$	9.6	12	14
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=30\text{A}$, $di/dt=500\text{A}/\mu\text{s}$	17	21	25	nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ\text{C}$.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev1 : Oct 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

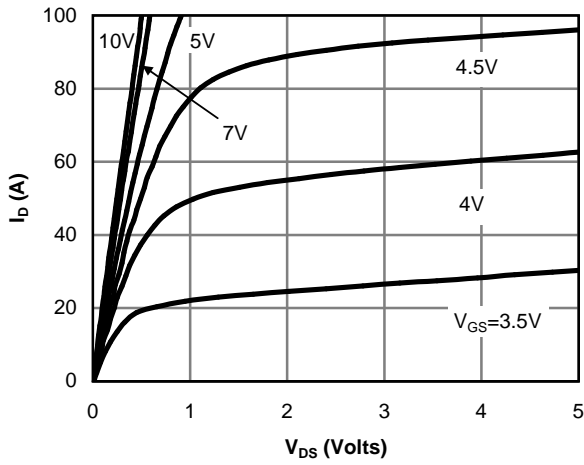


Fig 1: On-Region Characteristics

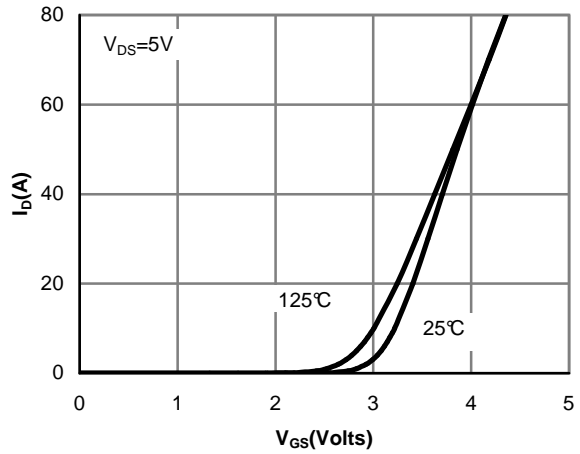


Figure 2: Transfer Characteristics

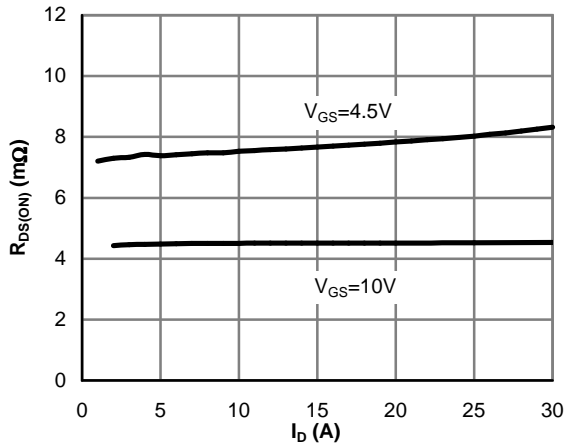


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

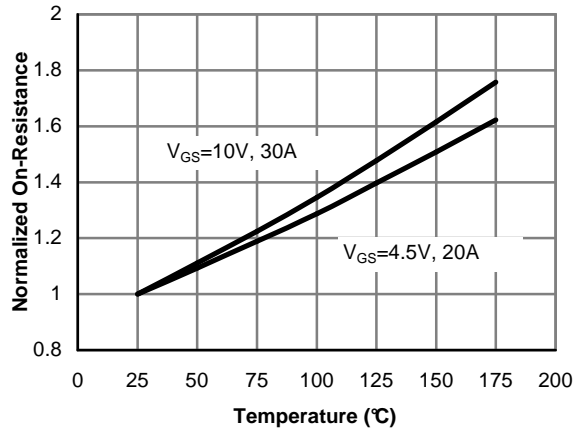


Figure 4: On-Resistance vs. Junction Temperature

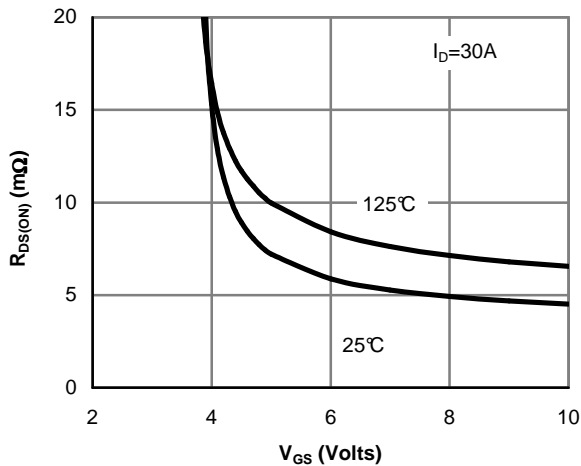


Figure 5: On-Resistance vs. Gate-Source Voltage

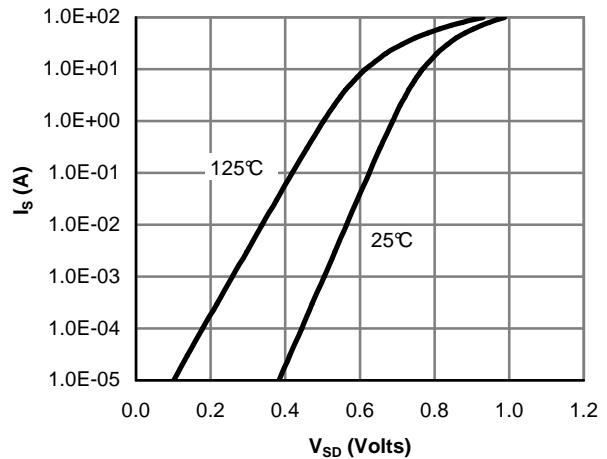


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

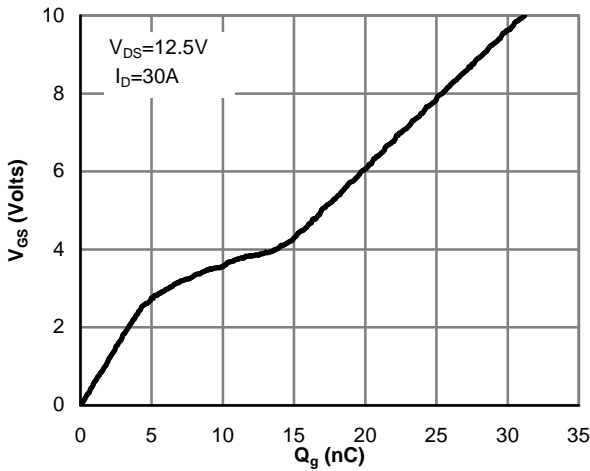


Figure 7: Gate-Charge Characteristics

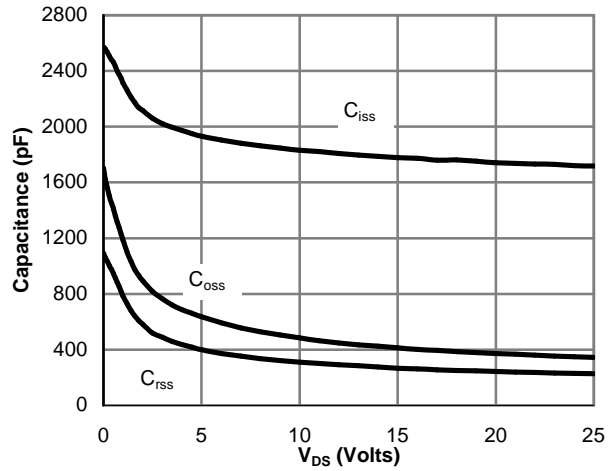


Figure 8: Capacitance Characteristics

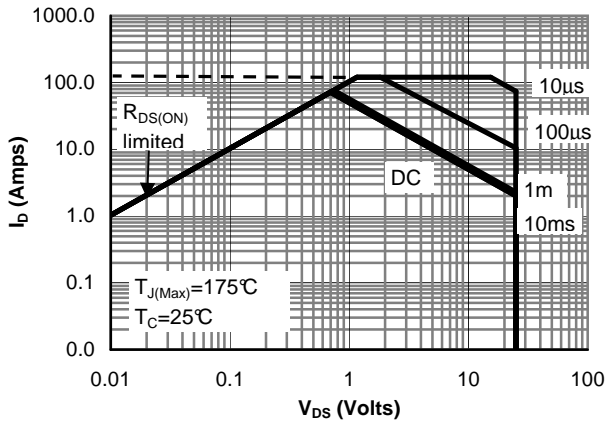


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

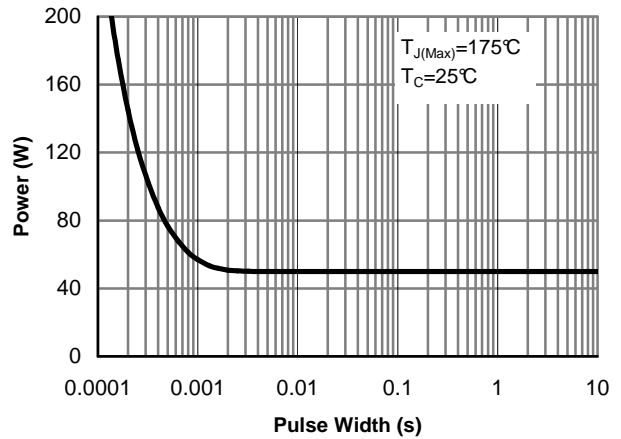


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

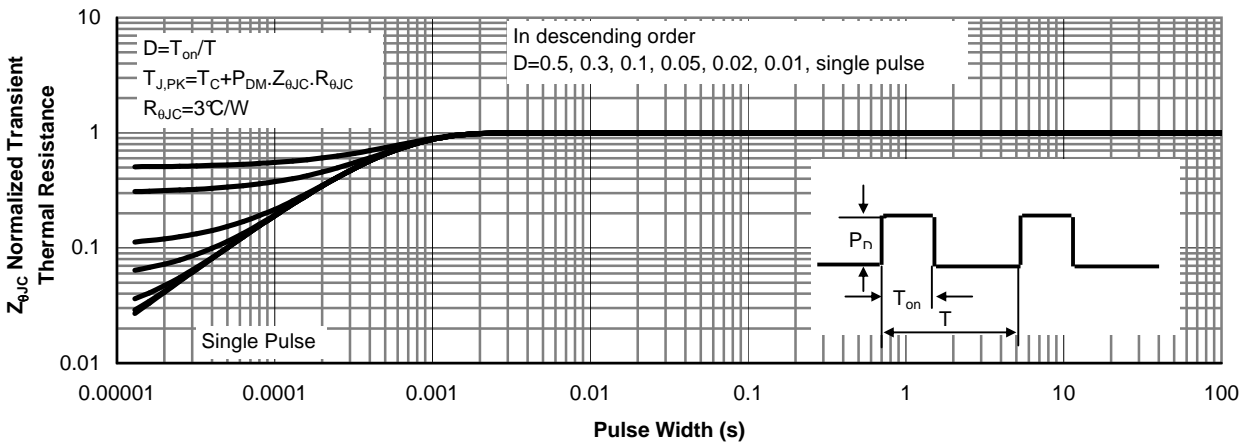


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

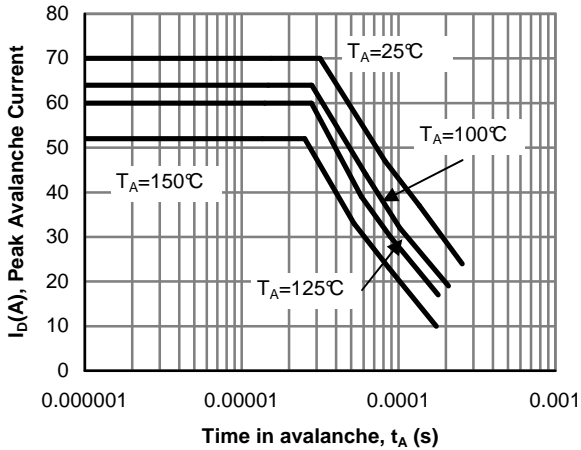


Figure 12: Single Pulse Avalanche capability

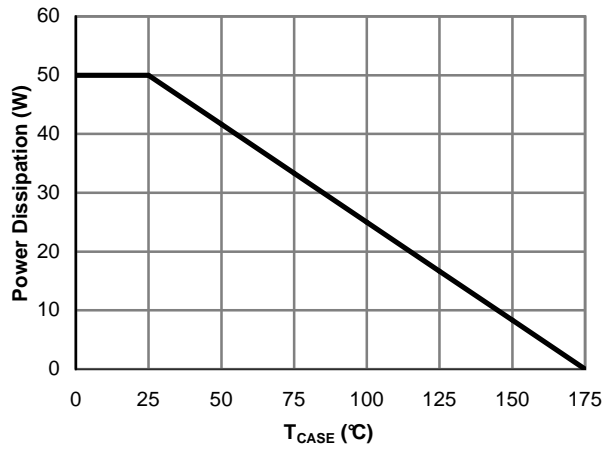


Figure 13: Power De-rating (Note F)

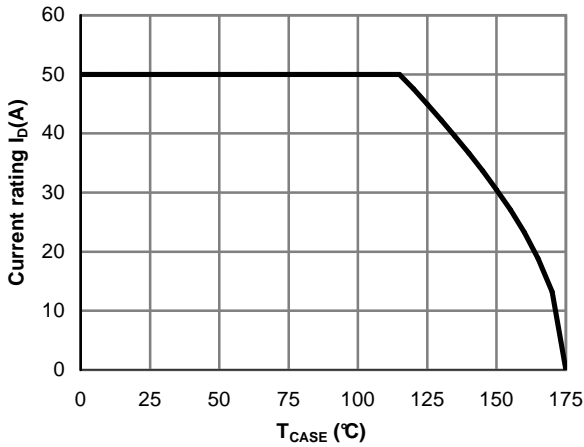


Figure 14: Current De-rating (Note F)

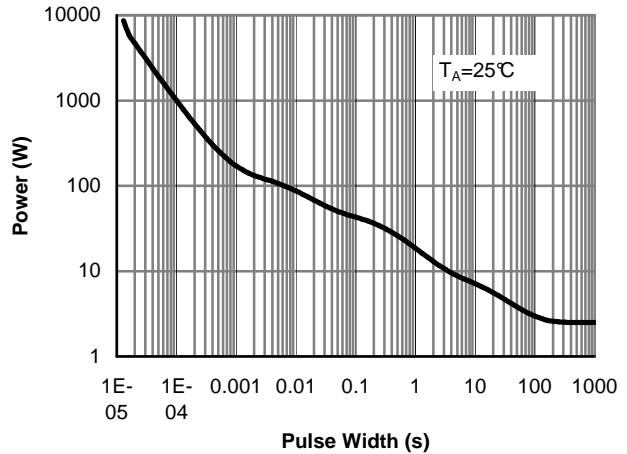


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

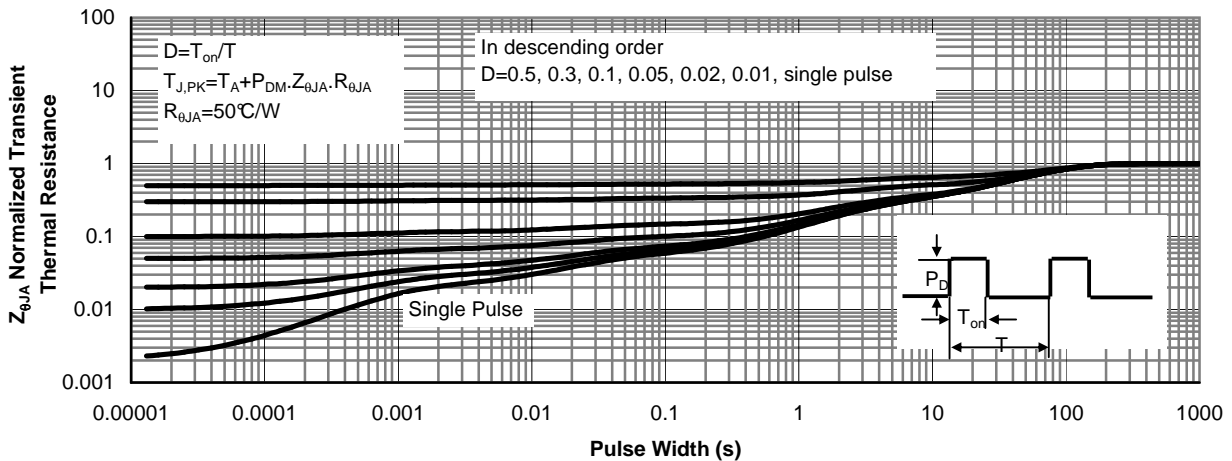


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

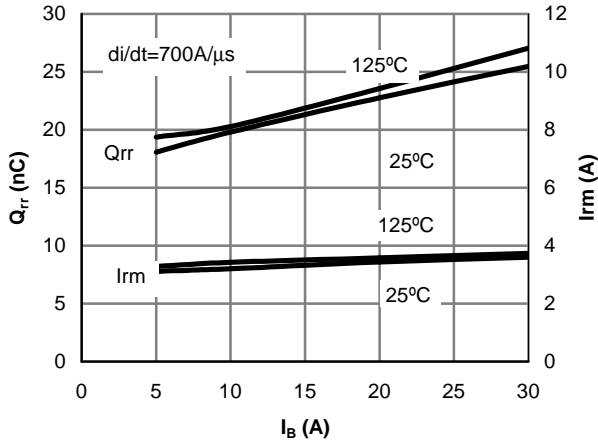


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

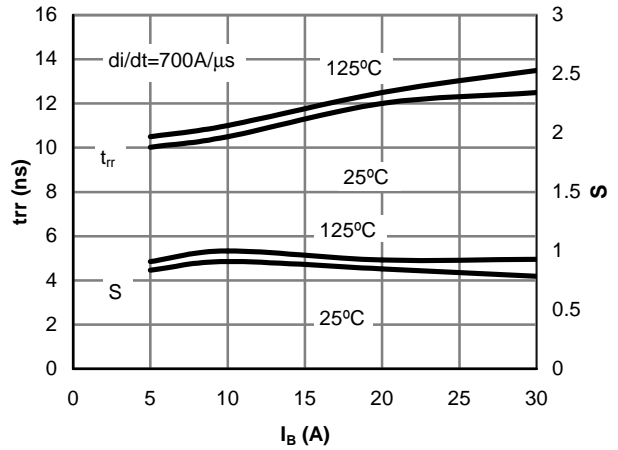


Figure 18: Diode Reverse Recovery Time and Soft Coefficient vs. Conduction Current

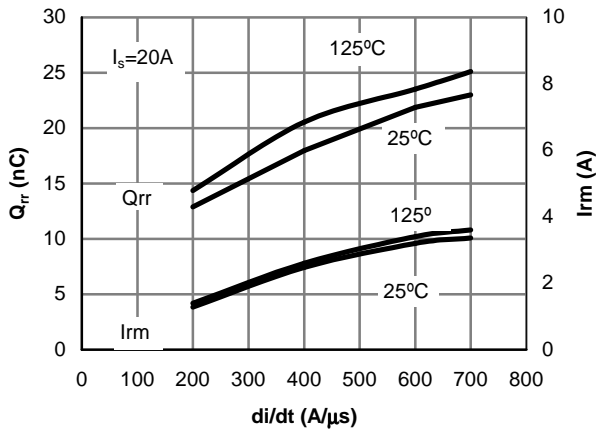


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt

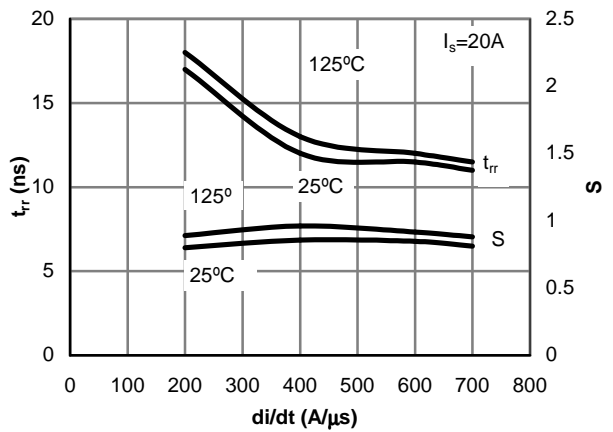
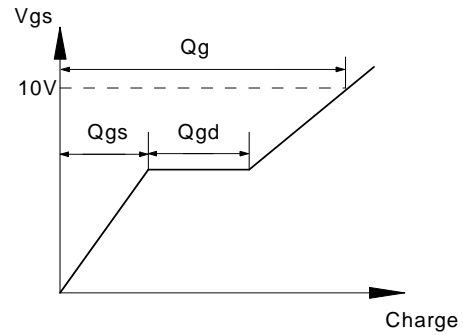
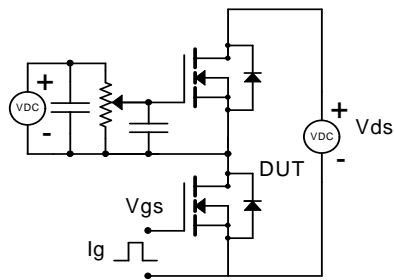
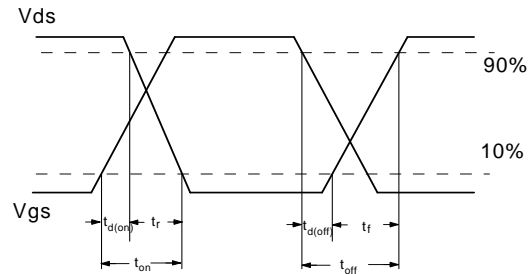
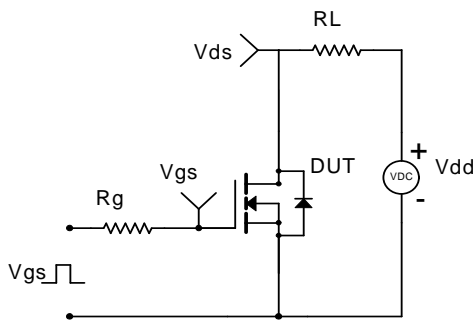


Figure 20: Diode Reverse Recovery Time and Soft Coefficient vs. di/dt

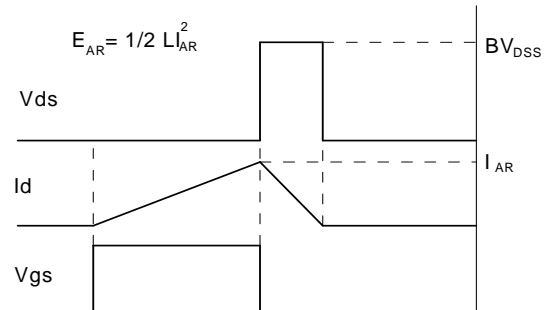
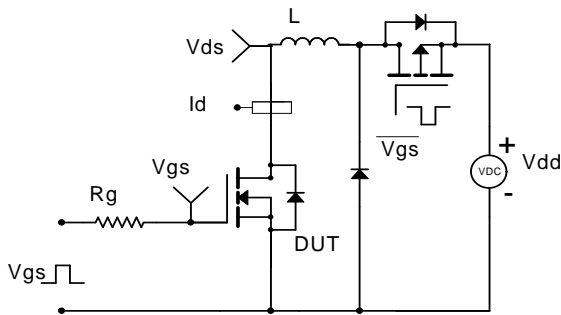
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

