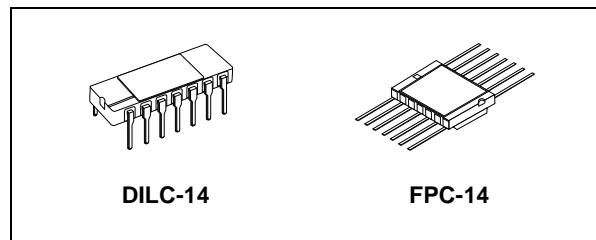




M54HC164

RAD-HARD 8 BIT SIPO SHIFT REGISTER

- HIGH SPEED:
 $f_{MAX} = 62\text{MHz}$ (TYP.) at $V_{CC} = 6\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 164
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9306-041



ORDER CODES

PACKAGE	FM	EM
DILC	M54HC164D	M54HC164D1
FPC	M54HC164K	M54HC164K1

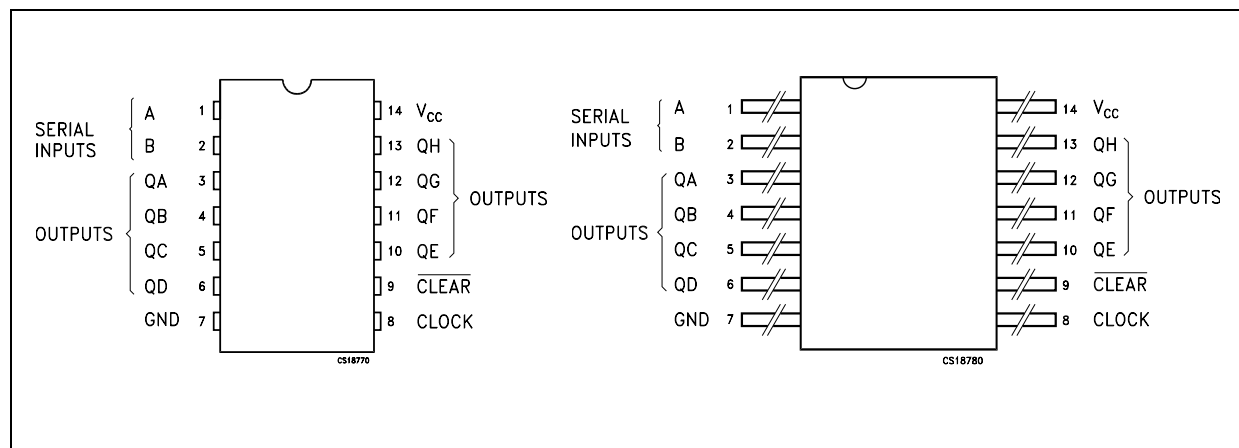
DESCRIPTION

The M54HC164 is an high speed CMOS 8 BIT SIPO SHIFT REGISTER fabricated with silicon gate C²MOS technology.

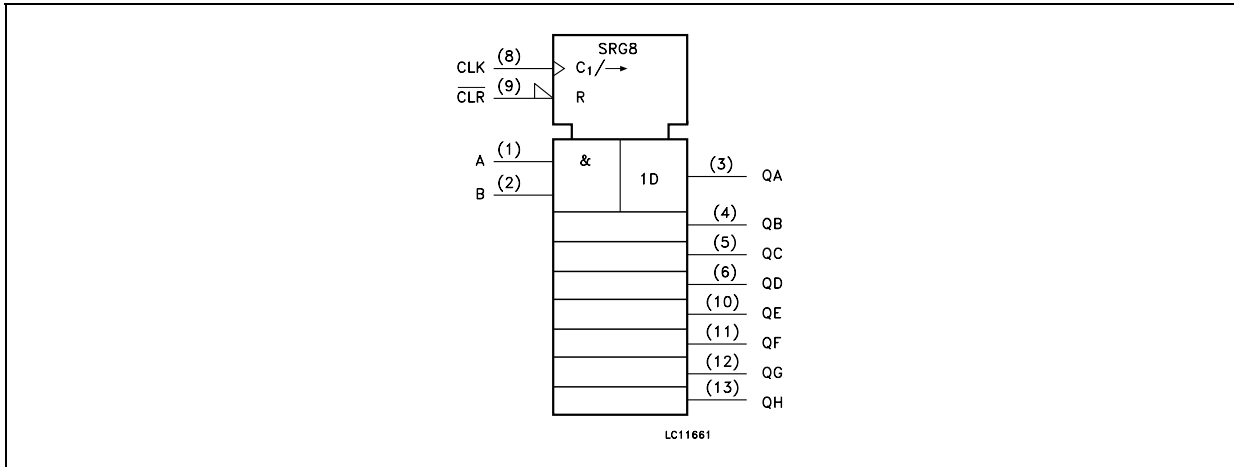
The M54HC164 is an 8 bit shift register with serial data entry and an output from each of the eight

stages. Data is entered serially through one of two inputs (A or B), either of these inputs can be used as an active high enable for data entry through the other input. An unused input must be high, or both inputs connected together. Each low-to-high transition on the clock inputs shifts data one place to the right and enters into QA the logic NAND of the two data inputs (A x B), the data that existed before the rising clock edge. A low level on the clear input overrides all other inputs and clears the register asynchronously, forcing all Q outputs low. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

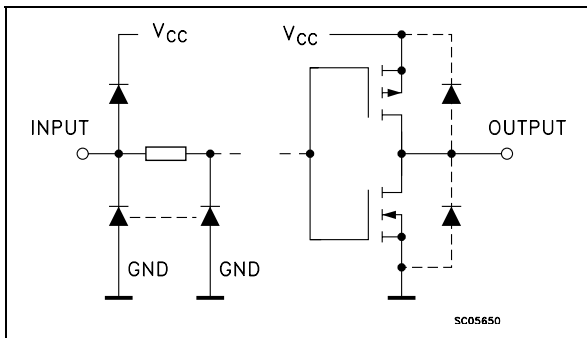
PIN CONNECTION



IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

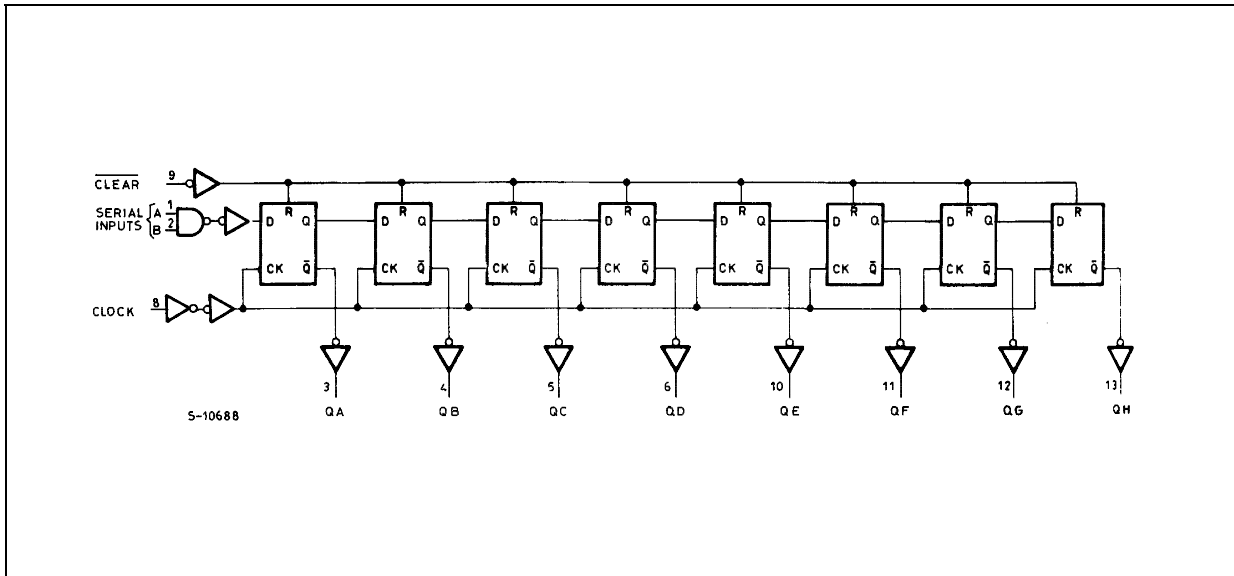
PIN N°	SYMBOL	NAME AND FUNCTION
1, 2	A, B	Data Inputs
3, 4, 5, 6, 10, 11, 12, 13	QA to QH	Outputs
8	CLOCK	Clock Input (LOW to HIGH, Edge Triggered)
9	CLEAR	Master Reset Input
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	SERIAL IN		QA	QB	QH
		A	B				
L	X	X	X	L	L	L
H		X	X	NO CHANGE			
H		L	X	L	QAn	QGn
H		X	L	L	QAn	QGn
H		H	H	H	QAn	QGn

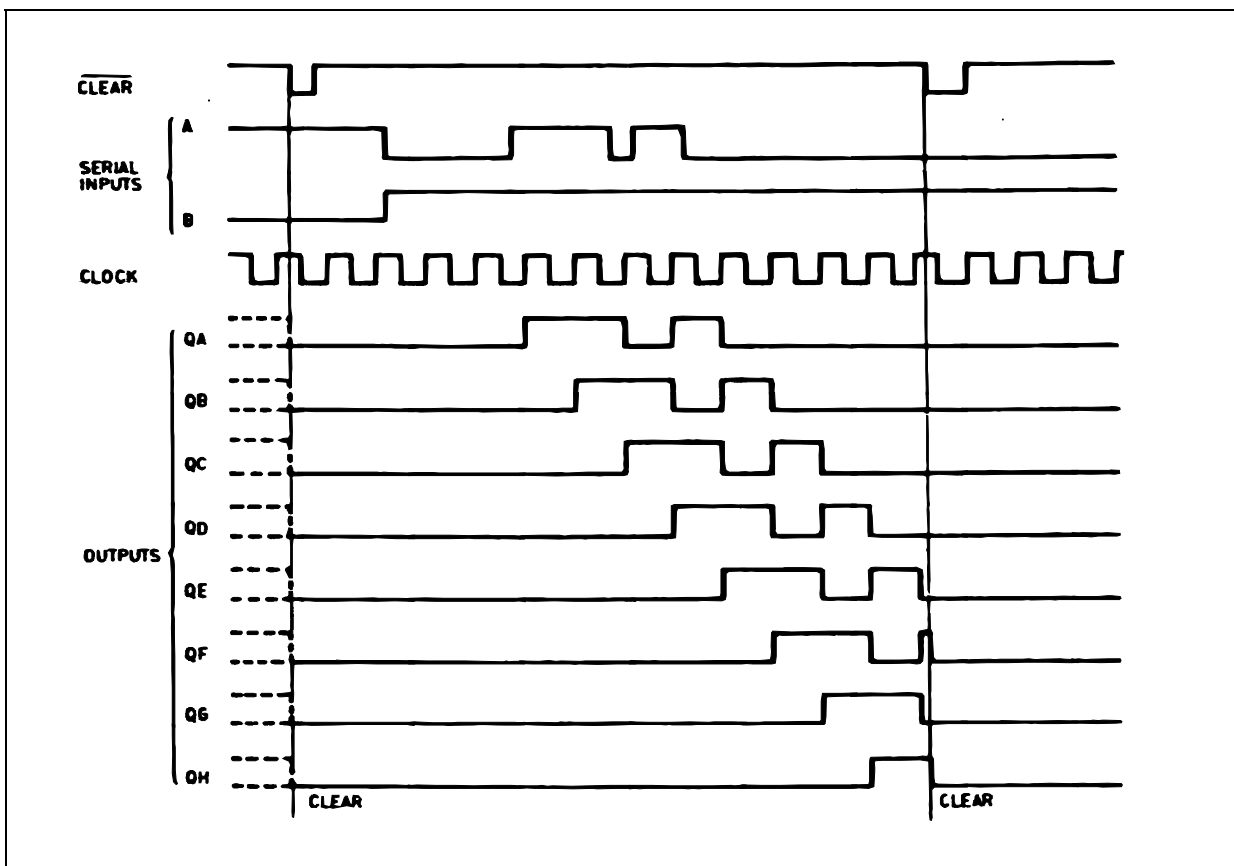
X : Don't Care
 QAn - QGn : The level of QA - QG, respectively, before the most-recent transition of the clock

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit	
V_{CC}	Supply Voltage	2 to 6	V	
V_I	Input Voltage	0 to V_{CC}	V	
V_O	Output Voltage	0 to V_{CC}	V	
T_{op}	Operating Temperature	-55 to 125	°C	
t_r, t_f	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V _{OH}	High Level Output Voltage	2.0	I _O =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I _O =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I _O =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60		
V _{OL}	Low Level Output Voltage	2.0	I _O =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O =20 μA		0.0	0.1		0.1		0.1	
		6.0	I _O =20 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND			4		40		80	μA

M54HC164

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

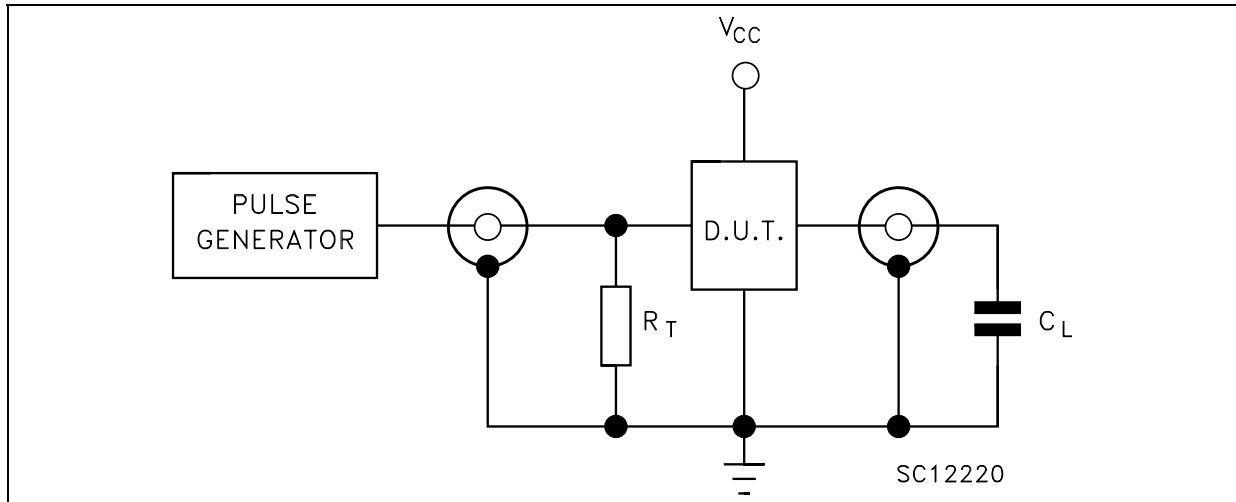
Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q)	2.0			57	160		200		240	ns
		4.5			19	32		40		48	
		6.0			16	27		34		41	
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Q)	2.0			60	175		220		265	ns
		4.5			20	35		44		53	
		6.0			17	30		37		45	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	18		5.0		4.2		MHz
		4.5		31	53		25		21		
		6.0		37	62		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0			40	75		95		110	ns
		4.5			10	15		19		22	
		6.0			9	13		16		19	
t_s	Set-up Time (A, B - CK)	2.0		50			65		75		ns
		4.5		10			13		15		
		6.0		9			11		13		
t_h	Hold Time (A, B - CK)	2.0		5			5		5		ns
		4.5		5			5		5		
		6.0		5			5		5		
t_{REM}	Minimum Removal Time	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			99						pF

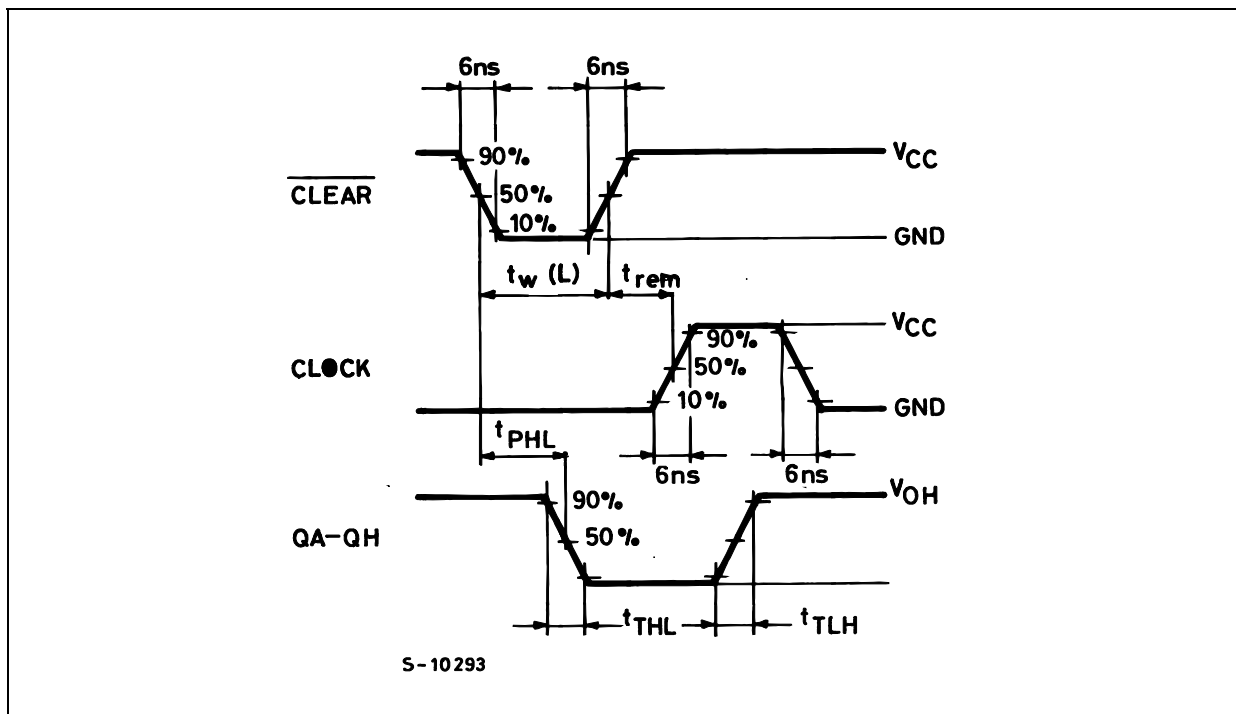
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

TEST CIRCUIT

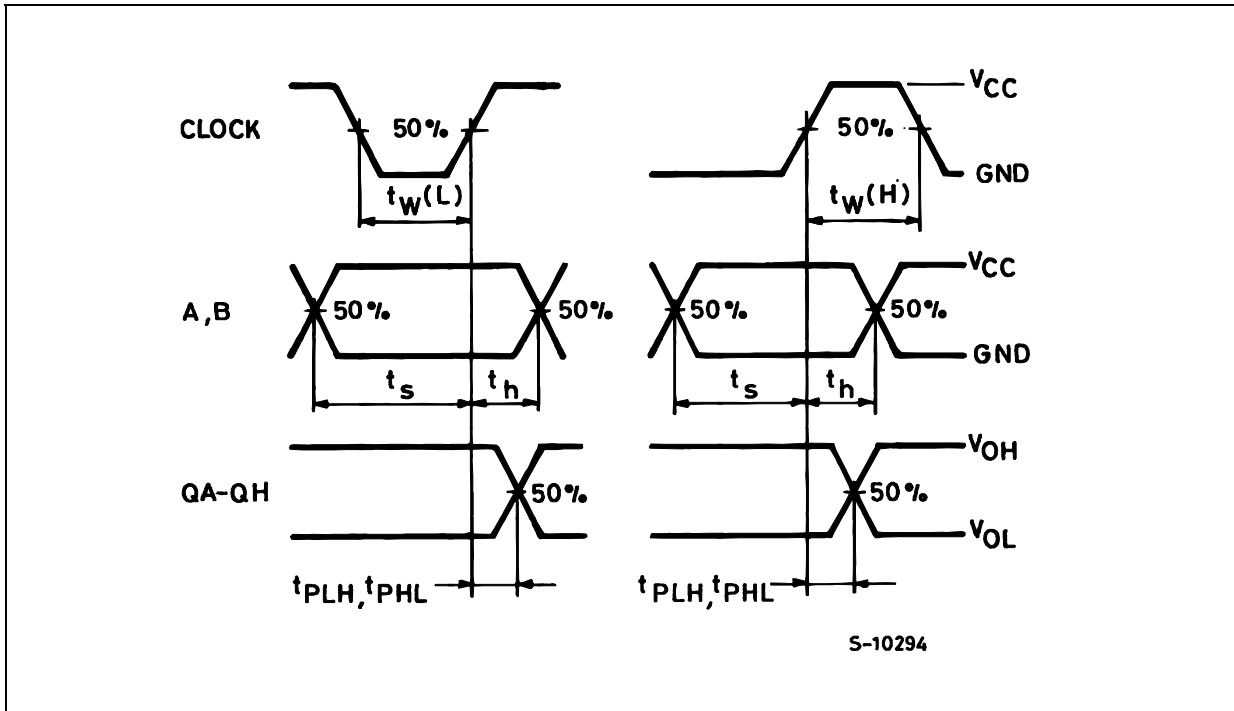


$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: MINIMUM PULSE WIDTH (CLEAR), MINIMUM REMOVAL TIME (CLEAR TO CLOCK)
 ($f=1\text{MHz}$; 50% duty cycle)

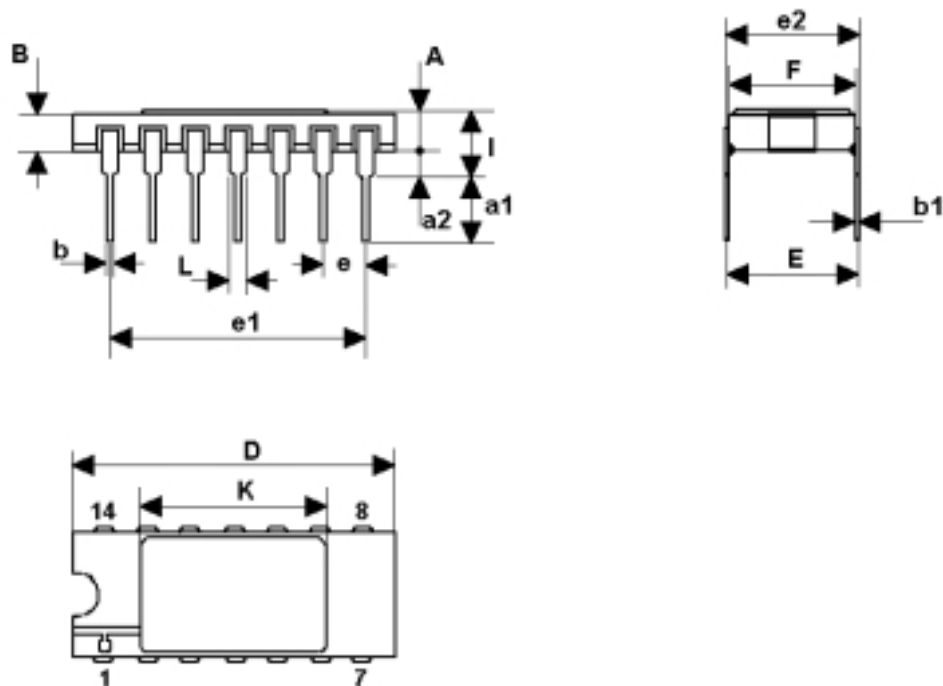


WAVEFORM 2: PROPAGATION DELAY TIMES, MINIMUM PULSE WIDTH (CLOCK), SETUP AND HOLD TIME (A, B TO CLOCK) (f=1MHz; 50% duty cycle)



DILC-14 MECHANICAL DATA

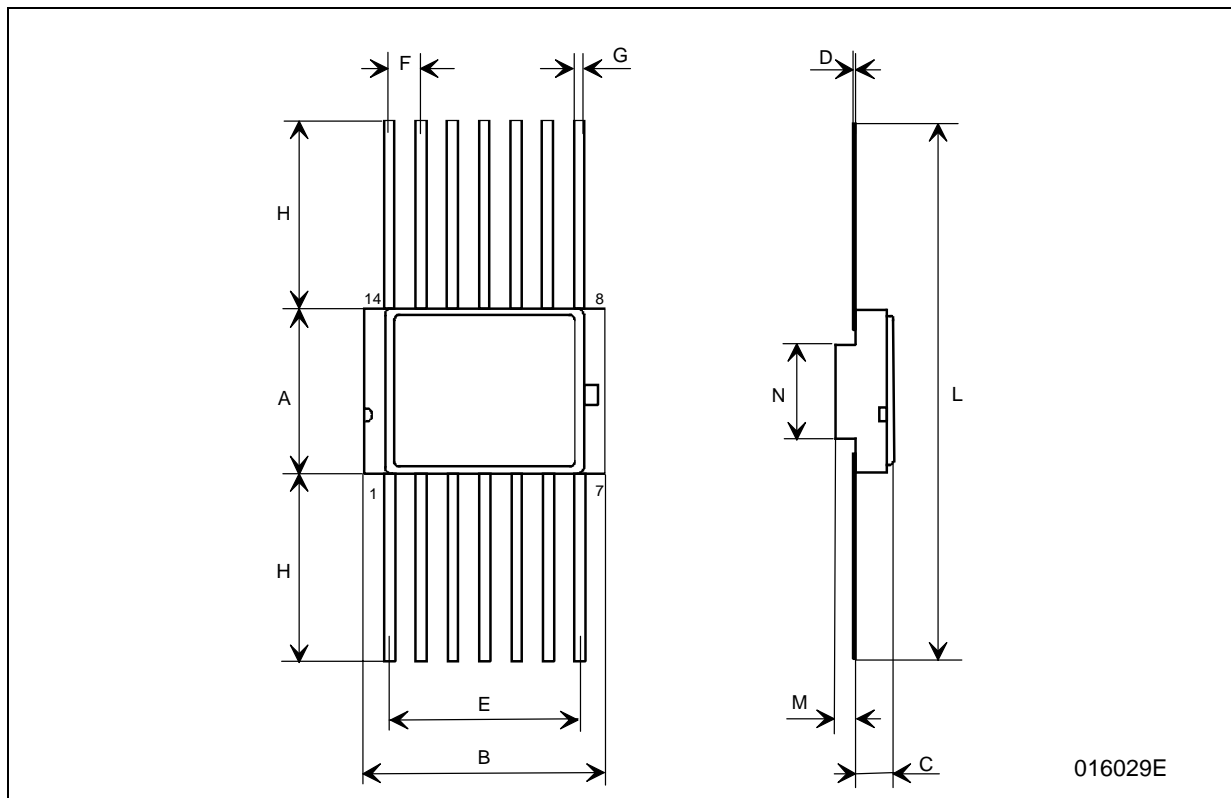
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		22.54	0.083		0.100
a1	3.00		3.70	0.118		0.146
a2	0.63	0.88	1.14	0.025	0.035	0.045
B	1.82	2.03	2.39	0.072	0.080	0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	18.79	19.00	19.20	0.740	0.748	0.756
e	7.36	7.62	7.87	0.290	0.300	0.310
e1		2.54			0.100	
e2	15.11	15.24	15.37	0.595	0.600	0.605
e3	7.62	7.87	8.12	0.300	0.310	0.320
F	7.11		7.75	0.280		0.305
I			3.70			0.146
K	10.90		12.1	0.429		0.476
L	1.14	1.27	1.5	0.045	0.050	0.059



0016173H

FPC-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	6.75	6.91	7.06	0.266	0.272	0.278
B	9.76	9.95	10.14	0.384	0.392	0.399
C	1.49		1.95	0.059		0.077
D	0.10	0.127	0.15	0.004	0.005	0.006
E	7.50	7.62	7.75	0.295	0.300	0.305
F		1.27			0.050	
G	0.38	0.43	0.48	0.015	0.017	0.019
H		6.0			0.236	
L	18.75		22.0	0.738		0.866
M		0.38			0.015	
N		4.31			0.170	



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