PH9030L

N-channel TrenchMOS logic level FET

Rev. 01 — 29 July 2008 Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC convertors
- Notebook computers
- Portable equipment
- Switched-mode power supplies

1.4 Quick reference data

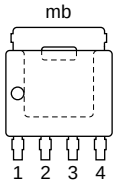
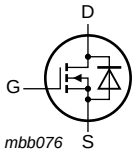
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	-	30	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1; see Figure 3	-	-	63	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	-	62.5	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 10 A; V_{DS} = 12 V; see Figure 10; see Figure 11	-	3.2	-	nC
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 8; see Figure 9	-	7	9	mΩ

NXP founded by Philips

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1,2,3	S	source	 **SOT669 (LFPAK)**	
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PH9030L	LFPAK	Plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

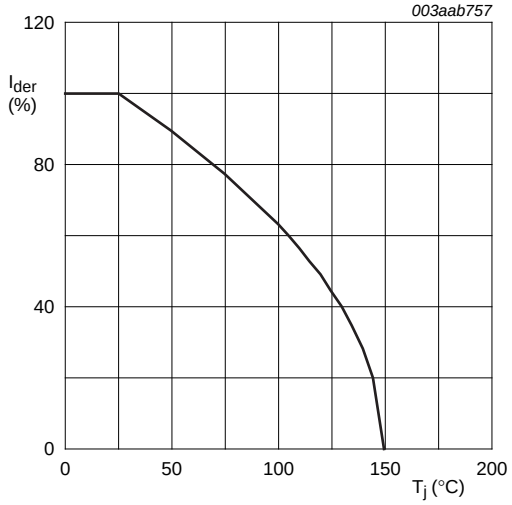
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

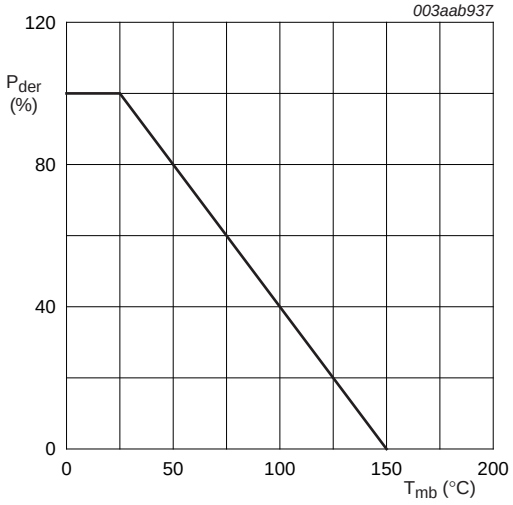
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	30	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	V_{GS} = 10 V; T_j = 100 °C; see Figure 1	-	39	A
		V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1; see Figure 3	-	63	A
I_{DM}	peak drain current	t_p ≤ 10 µs; pulsed; T_{mb} = 25 °C; see Figure 3	-	214	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	62.5	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	52	A
I_{SM}	peak source current	t_p ≤ 10 µs; pulsed; T_{mb} = 25 °C	-	208	A
Avalanche Ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 33 A; V_{sup} ≤ 30 V; unclamped; t_p = 0.08 ms; R_{GS} = 50 Ω	-	53	mJ

© NXP B.V. 2008. All rights reserved.



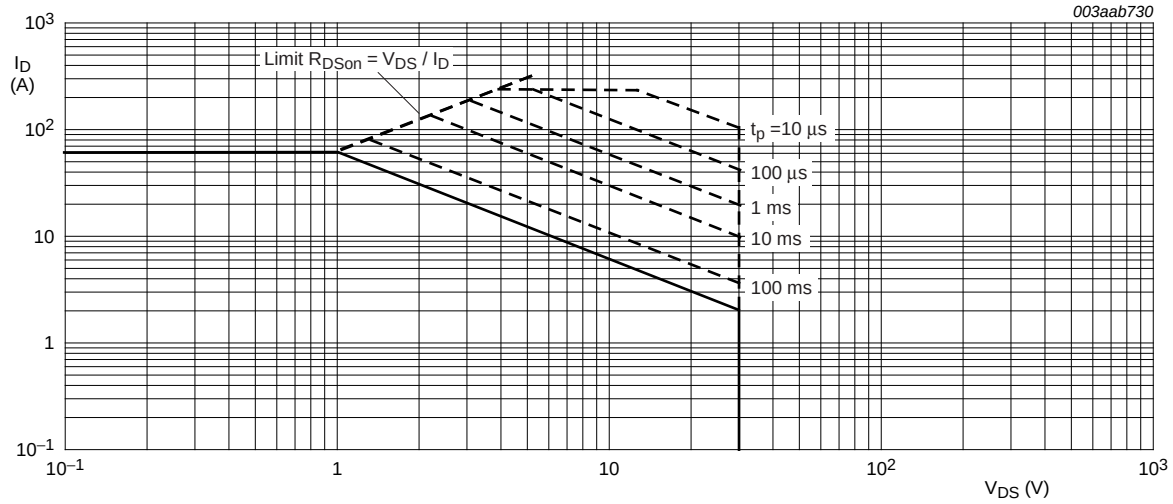
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$T_{mb} = 25\,°C; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

© NXP B.V. 2008. All rights reserved.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	2	K/W

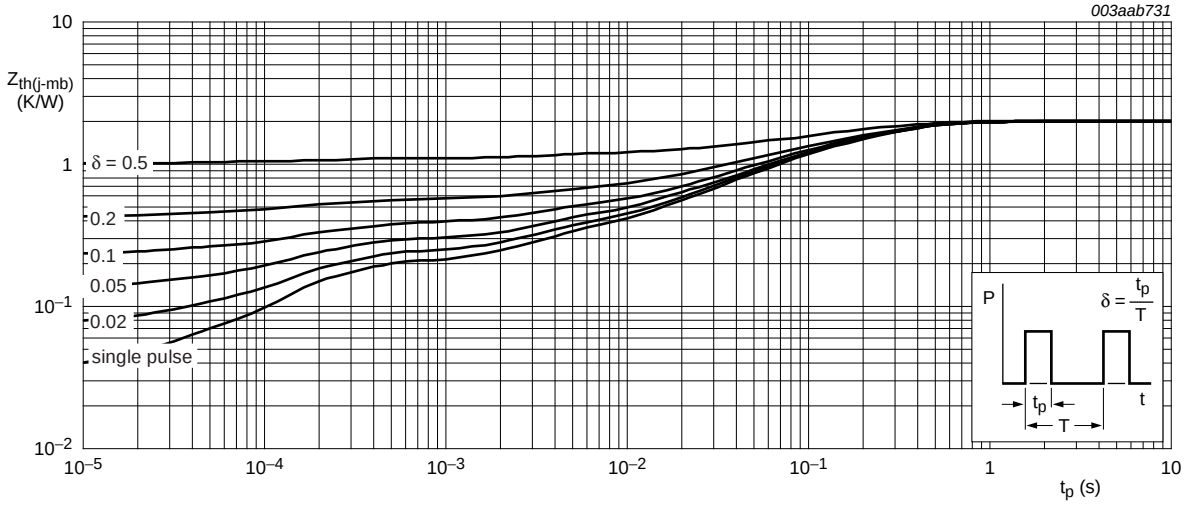


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

© NXP B.V. 2008. All rights reserved.

6. Characteristics

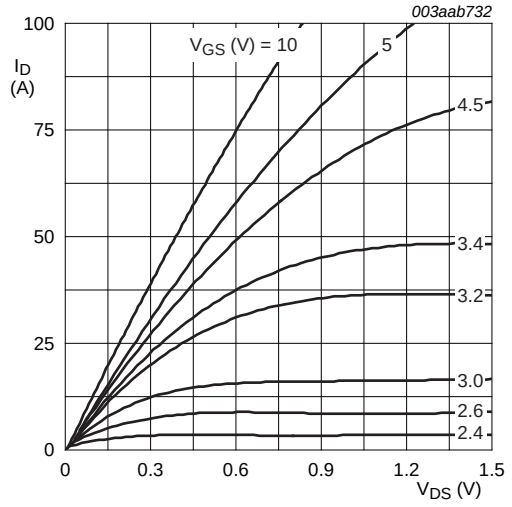
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 6; see Figure 7	1.3	1.7	2	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 7; see Figure 6	-	-	2.6	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 7; see Figure 6	0.8	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C; see Figure 8; see Figure 9	-	11.9	15.8	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; see Figure 8; see Figure 9	-	10	12.5	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 8; see Figure 9	-	7	9	mΩ
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C	-	-	100	µA
R_G	internal gate resistance (AC)	f = 1 MHz	-	0.56	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 12 V; V_{GS} = 4.5 V; see Figure 10; see Figure 11	-	13.3	-	nC
Q_{GS}	gate-source charge		-	4.8	-	nC
Q_{GD}	gate-drain charge		-	3.2	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 10 A; V_{DS} = 12 V; see Figure 10; see Figure 11	-	2.72	-	V
C_{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 12	-	1565	-	pF
		V_{DS} = 0 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C	-	1839	-	pF
C_{oss}	output capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 12	-	355	-	pF
C_{rss}	reverse transfer capacitance		-	186	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.5 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5.6 Ω	-	20	-	ns
t_r	rise time		-	41	-	ns
$t_{d(off)}$	turn-off delay time		-	15	-	ns

© NXP B.V. 2008. All rights reserved.

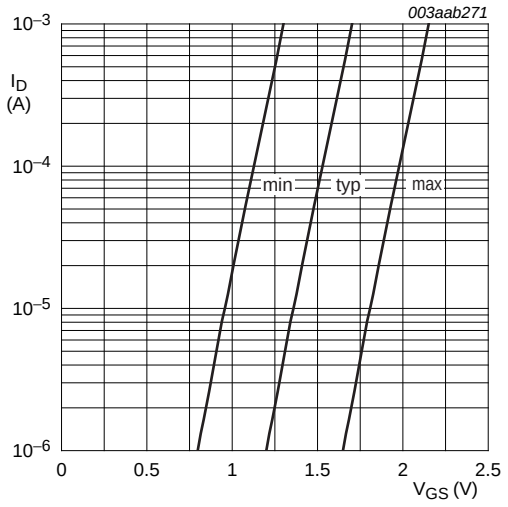
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	fall time	V_{DS} = 12 V; R_L = 0.5 Ω; R_L = 0.5 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 5.6 Ω	-	25	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 14	-	0.89	1.16	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/s; V_{GS} = 0 V; V_{DS} = 30 V	-	43	-	ns
Q_r	recovered charge		-	15	-	nC



$T_j = 25\,°C$

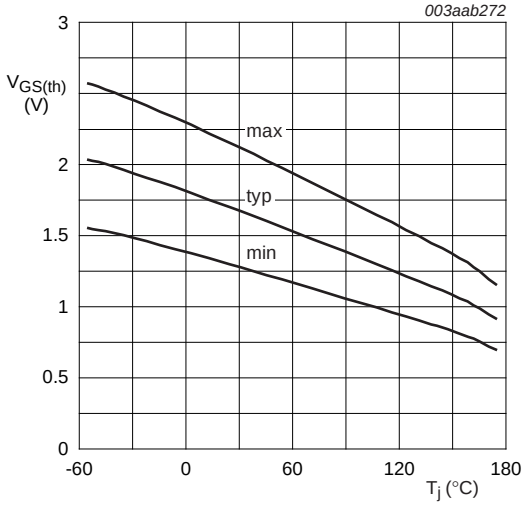
Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



$T_j = 25\,°C; V_{DS} = 5\,V$

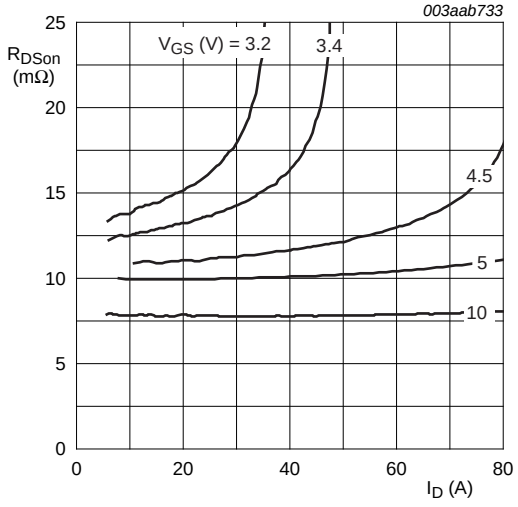
Fig 6. Sub-threshold drain current as a function of gate-source voltage

© NXP B.V. 2008. All rights reserved.



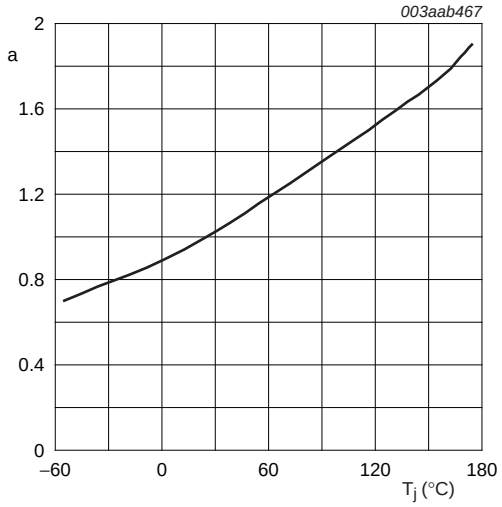
$I_D = 1\,mA; V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



$T_j = 25\,°C$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature

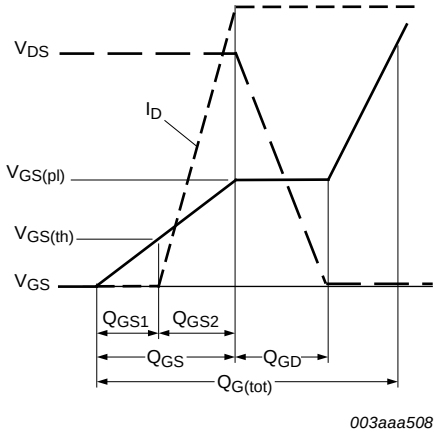
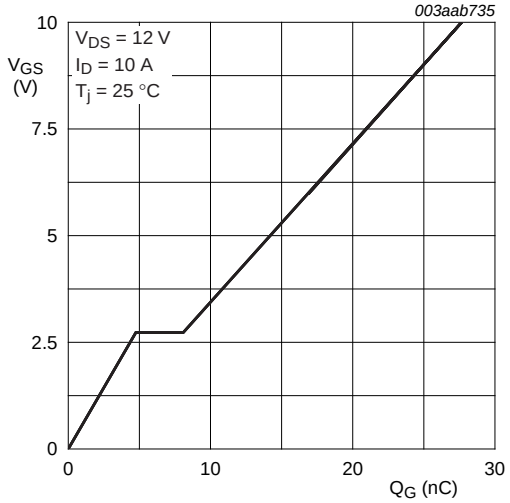


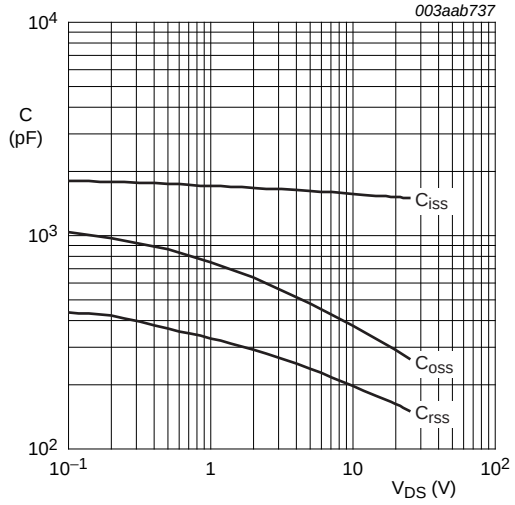
Fig 10. Gate charge waveform definitions

© NXP B.V. 2008. All rights reserved.



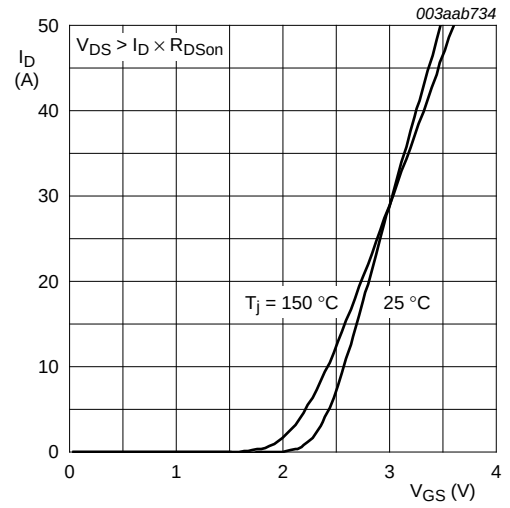
$I_D = 10A; V_{DS} = 12V$

Fig 11. Gate-source voltage as a function of gate charge; typical values



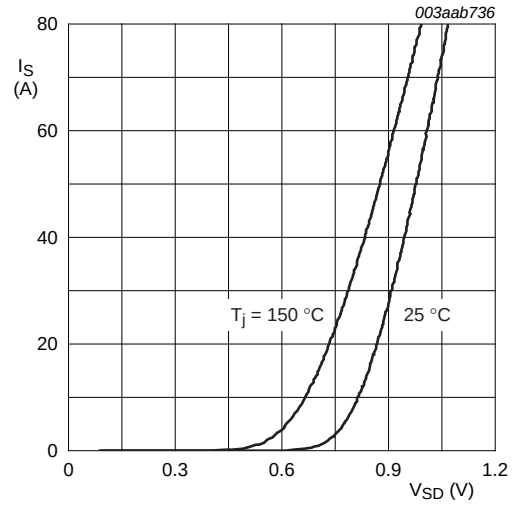
$V_{GS} = 0V; f = 1MHz$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25\,°C$ and $150\,°C; V_{DS} > I_D \times R_{DSon}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



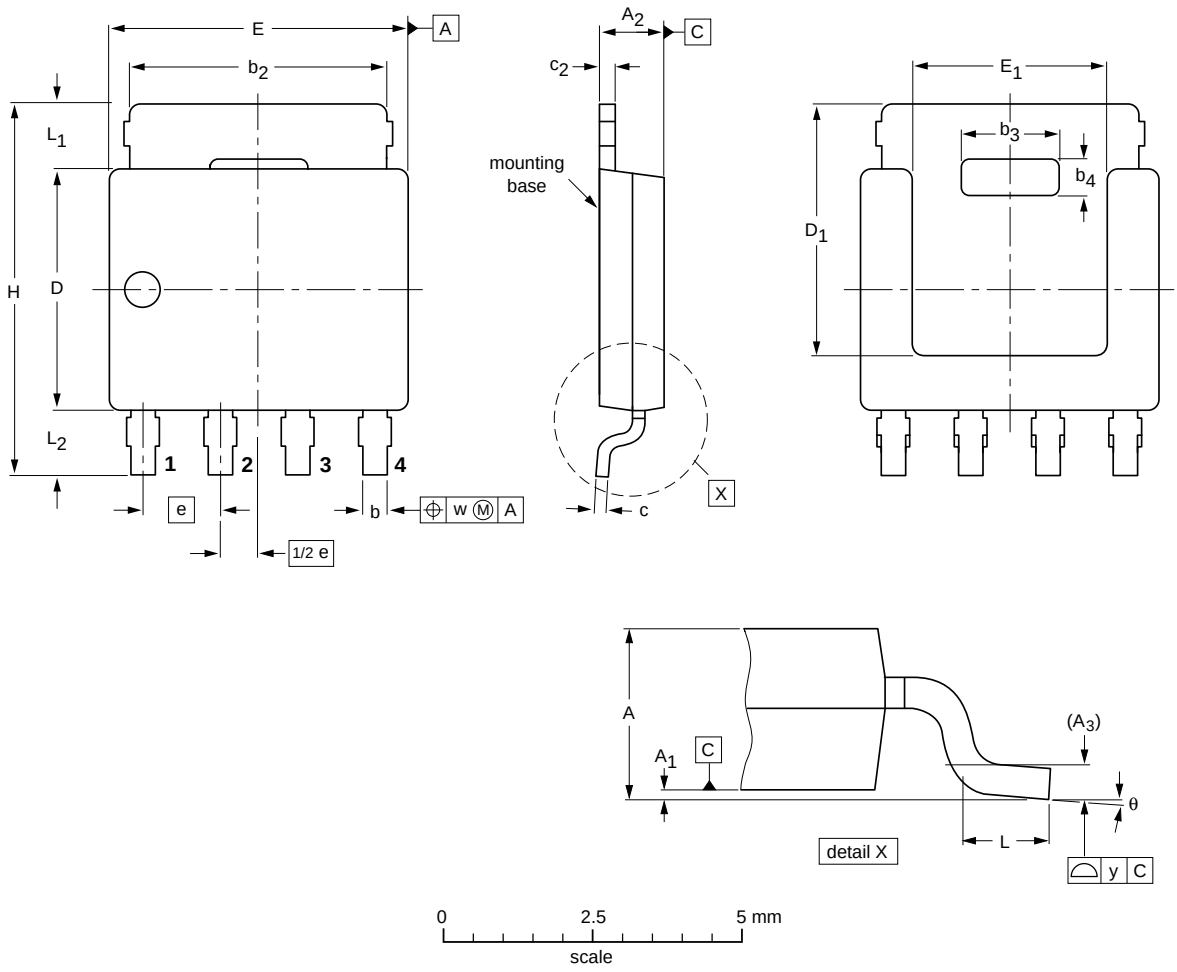
$T_j = 25\,°C$ and $150\,°C; V_{GS} = 0V$

Fig 14. Source current as a function of source-drain voltage; typical values

© NXP B.V. 2008. All rights reserved.

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	$D^{(1)}$	$D_1^{(1)}$ max	$E^{(1)}$	$E_1^{(1)}$	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~04-10-13~~ 06-03-16

Fig 15. Package outline SOT669 (LFPAK)

© NXP B.V. 2008. All rights reserved.

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH9030L_1	20080729	Product data sheet	-	-

© NXP B.V. 2008. All rights reserved.

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

9.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

TrenchMOS — is a trademark of NXP B.V.

10. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

© NXP B.V. 2008. All rights reserved.

11. Contents

1. Product profile 1
1.1 General description 1
1.2 Features and benefits 1
1.3 Applications 1
1.4 Quick reference data 1
2. Pinning information 2
3. Ordering information 2
4. Limiting values 2
5. Thermal characteristics 4
6. Characteristics 5
7. Package outline 9
8. Revision history 10
9. Legal information 11
9.1 Data sheet status 11
9.2 Definitions 11
9.3 Disclaimers 11
9.4 Trademarks 11
10. Contact information 11

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2008. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 29 July 2008
Document identifier: PH9030L_1

founded by

PHILIPS