



Features

- **Single Supply Operation:**
+ 2.7V ... + 5.25V
- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Up to 200ksps Conversion Rate**
- **± 1 LSB INL and DNL**
- **No Missing Codes**
- **True fully differential Operation**
- **Software-Configurable Unipolar or Bipolar output coding**
- **Internal 3.2MHz oscillator for independent operation from external clock**
- **Internal 2.5V Reference**
- **Low Power**
 - < 1.2mA (200ksps, 5V supply)
 - < 0.5µA (power-down mode)
- **SPI™ / QSPI™ / MICROWIRE™ - compatible 4-Wire Serial Interface**
- **20-Pin SSOP**
- **Alternate Source for MAX146 / MAX147**

Description

ZADCS146 and ZADCS147 are low power, 12-bit, successive approximation analog-to-digital (A/D) converters with up to 200ksps conversion rate, 8-channel input multiplexer, high-bandwidth track/hold and synchronous serial interface.

The ADC operates from a single + 2.7V to + 5.25V supply. Its analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface connects directly to SPI™/ (QSPI™ and MICROWIRE™) devices without external logic.

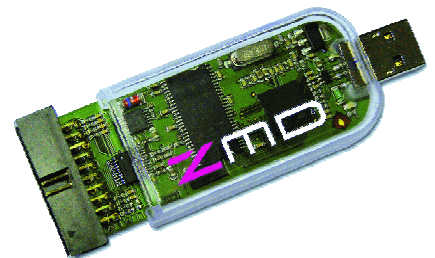
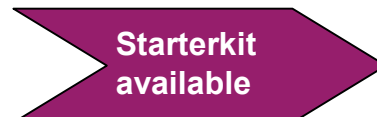
Both devices can use either the external serial-interface clock or an internal clock to perform successive-approximation analog-to-digital conversions. The internal clock can be used to run independent conversions on more than one device in parallel.

The ZADC146 is equipped with a highly accurate internal 2.5V reference with an additional external ±1.5% voltage adjustment range.

ZADCS146 / ZADCS147 provide a hard-wired shut-down pin (nSHDN) pin and software-selectable power-down modes that can be programmed to automatically shut down the IC at the end of a conversion. Accessing the serial interface automatically powers up the IC. A quick turn-on time allows the device to be shut down between all conversions.

Applications

- Data Acquisition
- Industrial Process Control
- Portable Data Logging
- Battery-Powered Systems



Functional Block Diagram

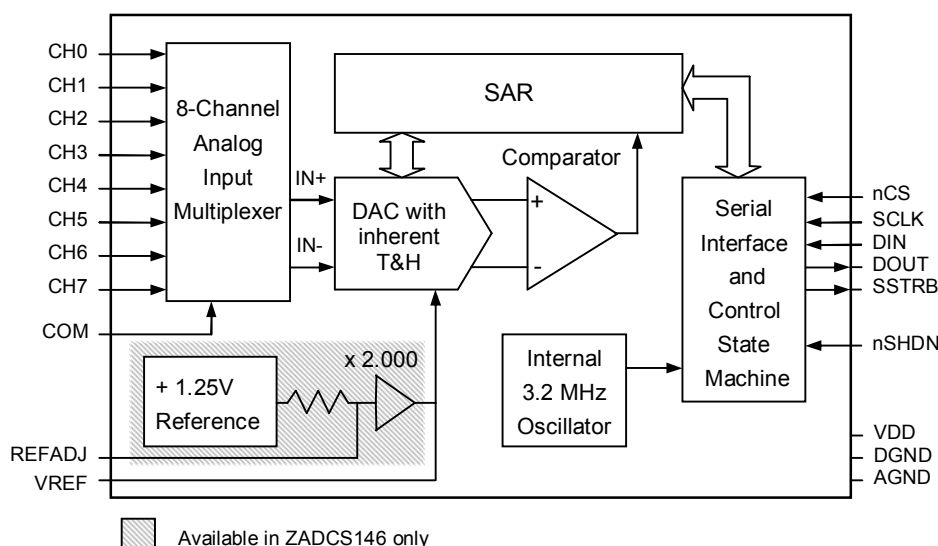


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1 General Device Specification

1.1 Absolute Maximum Ratings (Non Operating)

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
V_{DD-GND}	VDD to AGND, DGND	-0.3	6	V	
$V_{AGND-DGND}$	AGND to DGND	-0.3	0.3	V	
	CH0 – CH7, COM to AGND, DGND	-0.3	VDD+0.3	V	
	VREF, VREFADJ to AGND	-0.3	VDD+0.3	V	
	Digital Inputs to DGND	-0.3	6	V	
	Digital Outputs to DGND	-0.3	VDD+0.3	V	
	Digital Output Sink Current		25	mA	
I_{in}	Input current into any pin except supply pins (Latch-Up)	-100	100	mA	
V_{HBM}	Electrostatic discharge – Human Body Model (HBM)	2000		V	1
θ_{JCT}	Maximum Junction Temperature		+150°	°C	
θ_{OP}	Operating Temperature Range ZADCS146VIS20 / ZADCS147IS20	-25	+85	°C	
θ_{STG}	Storage temperature	-65	+150	°C	
θ_{lead}	Lead Temperature 100%Sn	JEDEC-J-STD-20C 260		°C	
H	Humidity non-condensing				2
P_{tot}	Total power dissipation		250	mW	
R_{thj}	Thermal resistance of Package SSOP20 / 5.3mm		100	K/W	

¹ HBM: C = 100pF charged to V_{HBM} with resistor R = 1.5k Ω in series, valid for all pins

² Level 4 according to JEDEC-020A is guaranteed

1.2 Package Pin Assignment

Table 2: Pin list

Package pin number	Name	Direction	Type	Description
1	CH0	IN	Analog	Analog Input Channel 0
2	CH1	IN	Analog	Analog Input Channel 1
3	CH2	IN	Analog	Analog Input Channel 2
4	CH3	IN	Analog	Analog Input Channel 3
5	CH4	IN	Analog	Analog Input Channel 4
6	CH5	IN	Analog	Analog Input Channel 5
7	CH6	IN	Analog	Analog Input Channel 6
8	CH7	IN	Analog	Analog Input Channel 7
9	COM	IN	Analog	Negative input reference (IN.) for analog inputs in Single-Ended Mode
10	nSHDN	IN	Analog	Active Low Shutdown
11	VREF	I/O	Analog	Reference Buffer Output / External Reference Input
12	REFADJ	I/O	Analog	Input to Reference Buffer Amplifier / Not connected at ZADCS147
13	AGND		SUPPLY	Analog Ground
14	DGND		SUPPLY	Digital Ground
15	DOUT	OUT	CMOS Digital	Serial Data Output
16	SSTRB	OUT	CMOS Digital	Serial Strobe Output
17	DIN	IN	CMOS Digital	Serial Data Input
18	nCS	IN	CMOS Digital	Active Low Chip Select
19	SCLK	IN	CMOS Digital	Serial Clock Input
20	VDD		SUPPLY	Positive Supply Voltage

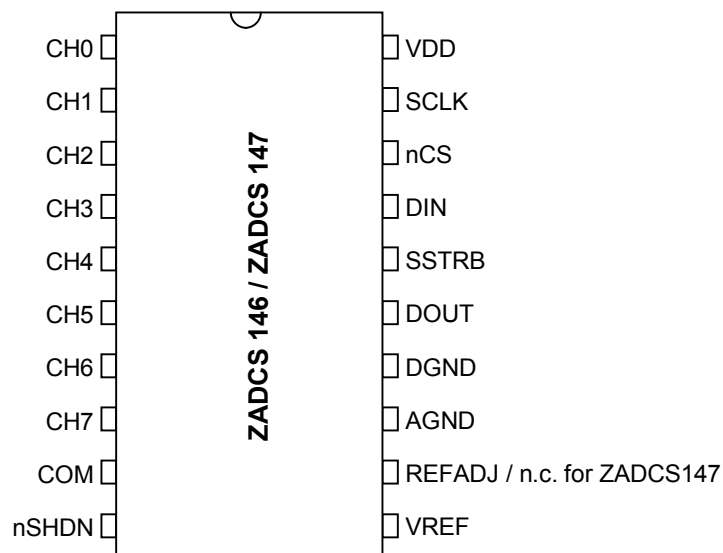


Figure 1: Package Pin Assignment for ZADCS146 & ZADCS147

1.3 Electrical Characteristics

1.3.1 General Parameters

(VDD = +2.7V to + 5.25V; f_{SCLK} = 3.2MHz (50% duty cycle); 16 clocks/conversion cycle (200 ksps); V_{REF} = 2.500V applied to VREF pin; $\theta_{OP} = \theta_{OPmin} \dots \theta_{OPmax}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC Accuracy						
Resolution				12		Bits
Relative Accuracy		ZADCS146 / ZADCS147			± 1.0	LSB
No Missing Codes	NMC		12			Bits
Differential Nonlinearity		ZADCS146 / ZADCS147			± 1.0	LSB
Offset Error				± 0.5	± 3.0	LSB
Gain Error				± 0.5	± 4.0	LSB
Gain Temperature Coefficient				± 0.25		ppm/°C
Dynamic Specifications (10kHz sine-wave input, 0V to 2.500Vpp, 200ksps, 3.2MHz external clock)						
Signal-to-Noise + Distortion Ratio	SINAD		68	73		dB
Total Harmonic Distortion	THD	Up to the 5 th harmonic		-88	-75	dB
Spurious-Free Dynamic Range	SFDR		74	80		dB
Small-Signal Bandwidth		-3dB roll off		3.8		MHz
Conversion Rate						
Sampling Time (= Track/Hold Acquisition Time)	t _{ACQ}	Ext. Clock = 3.2MHz, 2.5 clocks/ acquisition	0.781			µs
Conversion Time	t _{CONV}	Ext. Clock = 3.2MHz, 12 clocks/ conversion			3.75	µs
		Int. Clock = 3.2MHz +/- 12% tolerance	3.30		4.20	µs
Aperture Delay				30		ns
Aperture Jitter				< 50		ps
External Clock Frequency			0.1		3.2	MHz
Internal Clock Frequency			2.81	3.2	3.58	MHz
Analog Inputs						
Input Voltage Range, Single-Ended and Differential		Unipolar, COM = 0V			0 to VREF	V
		Bipolar, COM = VREF/2			± VREF / 2	
Input Capacitance				16		pF

1.3.2 ZADCS146 Specific Parameters

(VDD = +2.7V to + 5.25V; f_{SCLK} = 3.2MHz (50% duty cycle); 16 clocks/conversion cycle (200 ksps); θ_{OP} = θ_{OPmin} ... θ_{OPmax})

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Reference at VREF						
VREF Output Voltage		T _A = + 25°C	2.480	2.500	2.520	V
VREF Short-Circuit Current					30	mA
VREF Temperature Coefficient				± 30	± 50	ppm/°C
Load Regulation		0 to 0.2mA output load		0.35		mV
Capacitive Bypass at VREF			4.7			µF
Capacitive Bypass at REFADJ			0.047			µF
REFADJ Adjustment Range				± 1.5		%
External Reference at VREF (internal buffer disabled by V(REFADJ) = VDD)						
VREF Input Voltage Range			1.0		VDD + 50mV	V
VREF Input Current		VREF = 2.5V		180	215	µA
VREF Input Resistance			11.5	14		kΩ
Shutdown VREF Input Current					0.1	µA
REFADJ Buffer Disable Threshold			VDD-0.5			V
External Reference at VREF_ADJ						
Reference Buffer Gain				2.00		
VREF_ADJ Input Current					±80	µA
Full Power Down VREFADJ Input Current		Full Power-Down mode			0.1	µA
Power Requirements						
Positive Supply Voltage	VDD		2.7		5.25	V
Positive Supply Current	IDD	VDD=3.6V	Operating Mode ext. VREF	0.85	1.0	mA
			Operating Mode int. VREF	1.3	1.4	mA
			Fast Power-Down int. VREF	250	300	µA
			Full Power-Down	0.5	4.0	µA
Positive Supply Current	IDD	VDD=5.25V	Operating Mode ext. VREF	1.00	1.3	mA
			Operating Mode int. VREF	1.40	1.6	mA
			Fast Power-Down	250	300	µA
			Full Power-Down	0.5	4.0	µA

1.3.3 ZADCS147 Specific Parameters

(VDD = +2.7V to + 5.25V; f_{SCLK} = 3.2MHz (50% duty cycle); 16 clocks/conversion cycle (200 ksp/s); $\theta_{OP} = \theta_{OPmin} \dots \theta_{OPmax}$)

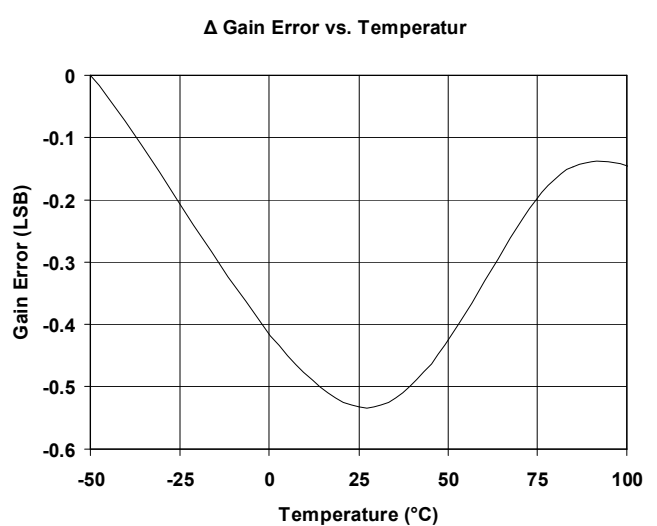
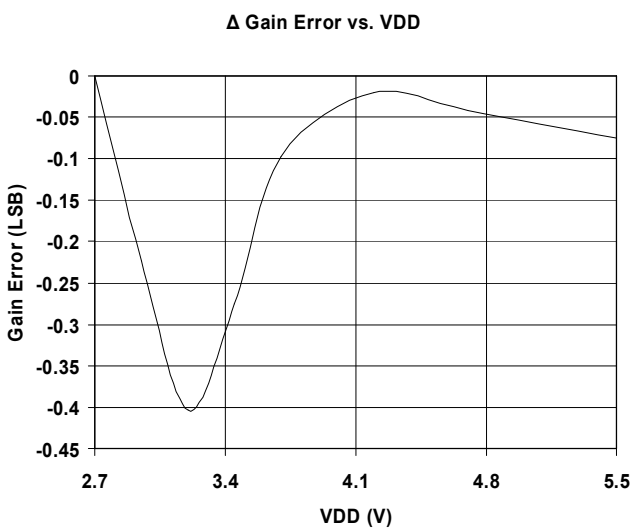
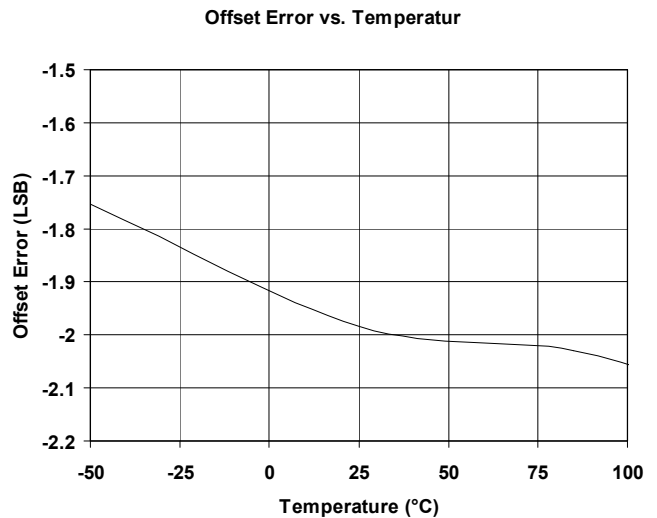
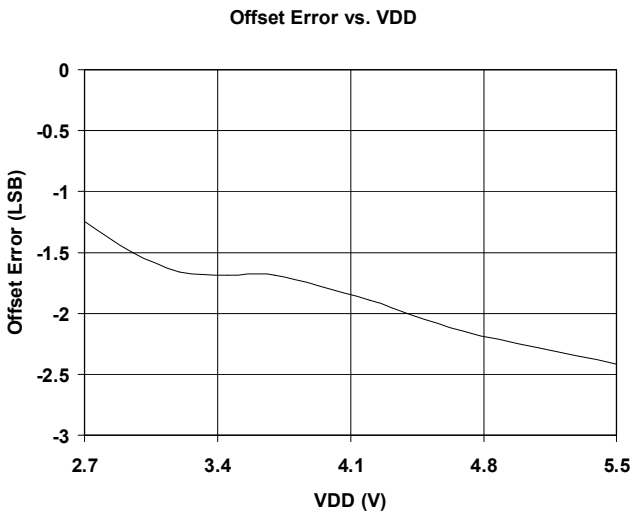
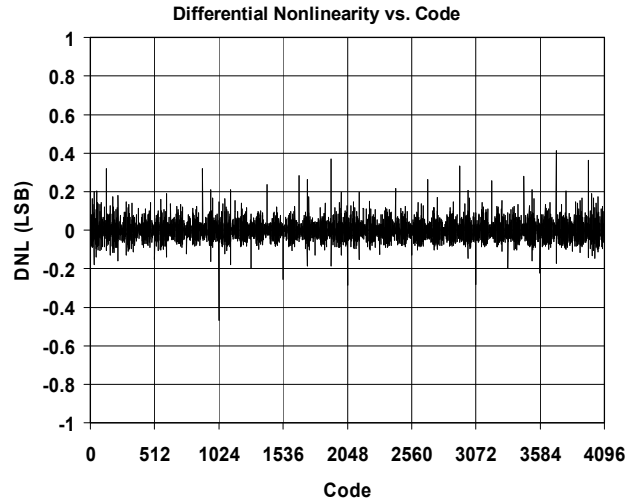
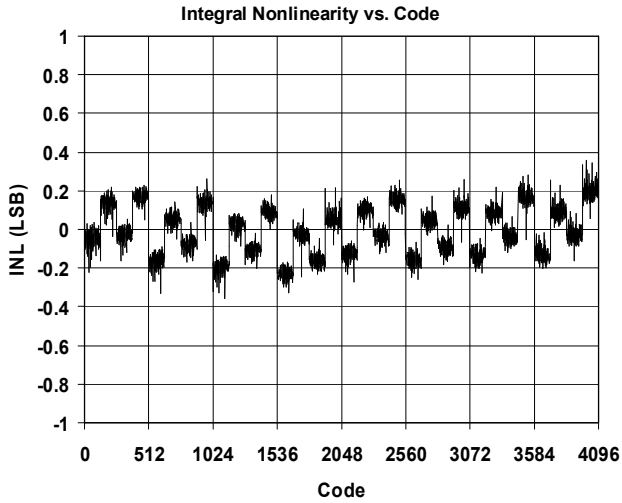
Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
External Reference at VREF							
VREF Input Voltage Range			1.0		VDD + 50mV	V	
VREF Input Current		VREF = 2.5V		180	215	μA	
VREF Input Resistance			11.5	14		kΩ	
Shutdown VREF Input Current					0.1	μA	
Capacitive Bypass at VREF			4.7			μF	
Power Requirements							
Positive Supply Voltage	VDD		2.7		5.25	V	
Positive Supply Current	IDD	VDD = 3.6V	Operating Mode		0.85	1.0	μA
			Full Power-Down		0.5	4.0	
Positive Supply Current	IDD	VDD = 5.25V	Operating Mode		1.00	1.3	μA
			Full Power-Down		0.5	4.0	

1.3.4 ZADCS146 / ZADCS147 Digital Pin Parameters

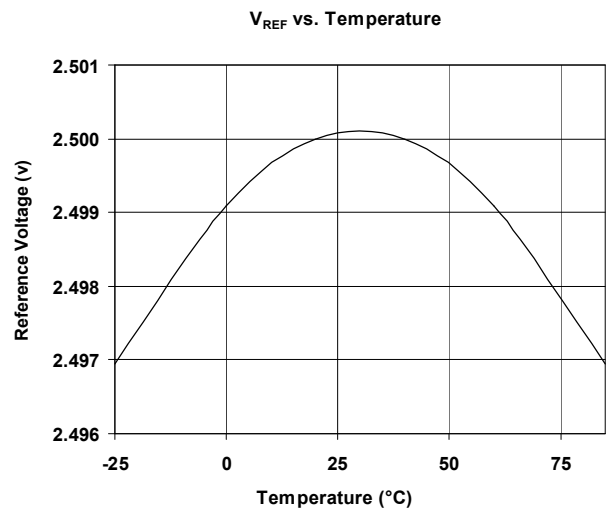
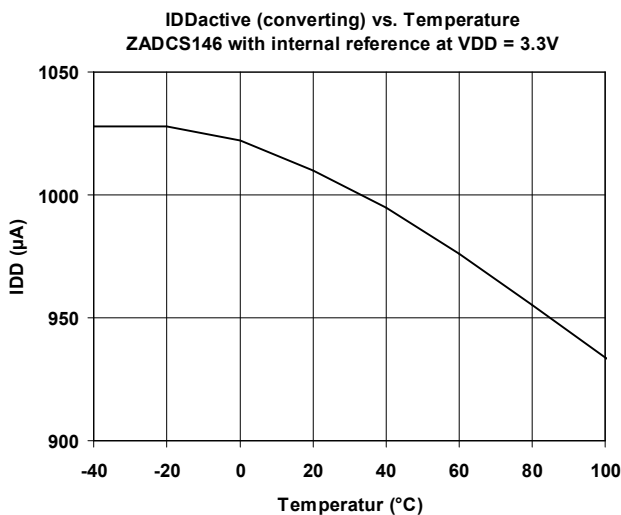
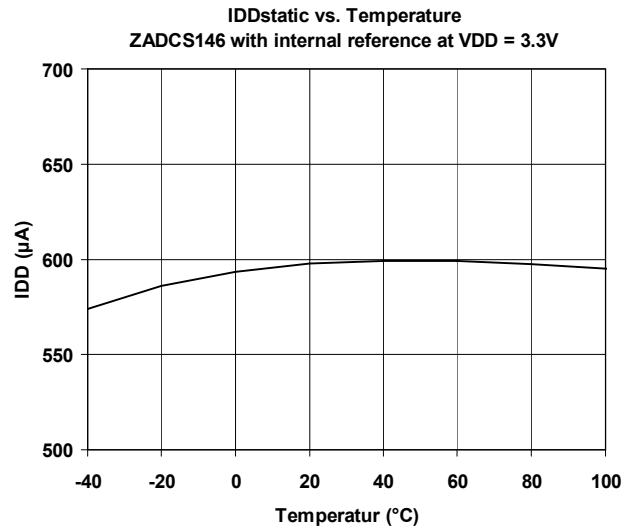
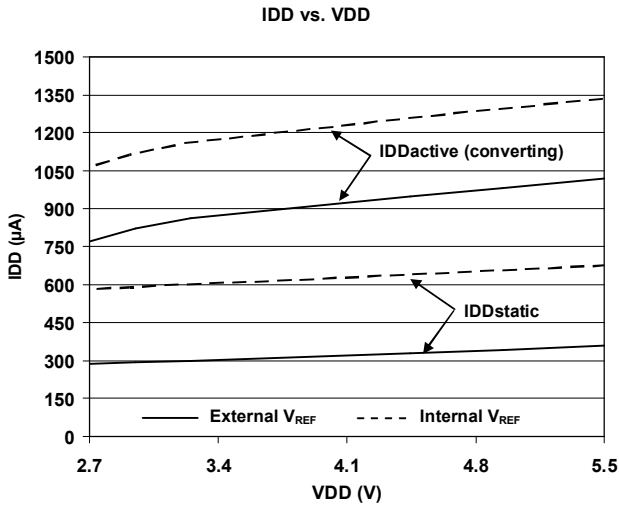
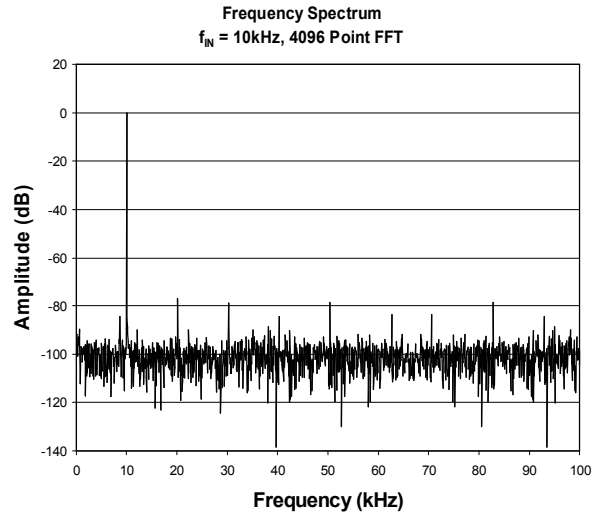
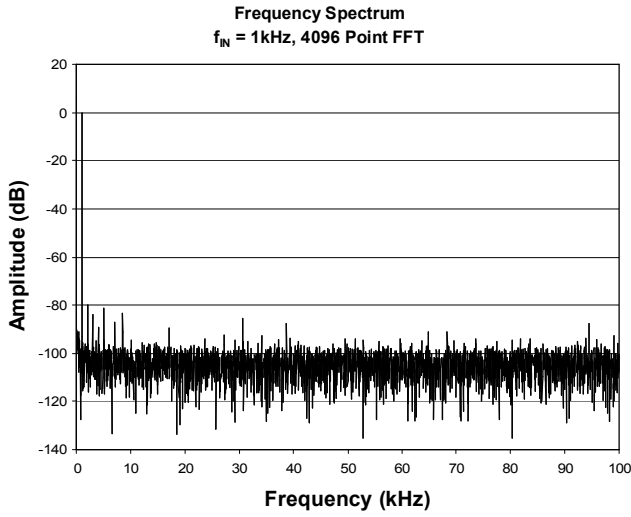
(VDD = +2.7V to + 5.25V; f_{SCLK} = 3.2MHz (50% duty cycle); 16 clocks/conversion cycle (200 ksp/s); $\theta_{OP} = \theta_{OPmin} \dots \theta_{OPmax}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Inputs (DIN, SCLK, CS, nSHDN)						
Logic High Level	V _{IH}	VDD = 2.7V	1.9			V
		VDD = 5.25V	3.3			V
Logic Low Level	V _{IL}	VDD = 2.7V			0.7	V
		VDD = 5.25V			1.4	V
Hysteresis	V _{Hyst}		0.7			V
Input Leakage	I _{IN}	VIN = 0V or VDD		± 0.1	± 1.0	μA
Input Low Leakage @ nSHDN	I _{IN_nSHDN}	VIN = 0V			- 5.0	μA
Input Capacitance	C _{IN}			5		pF
Digital Output (DOUT, SSTRB)						
Output High Current	I _{OH}	V _{OH} = VDD - 0.5V	VDD = 2.7V	3.5	8.5	mA
			VDD = 5.25V	5.5	10.8	mA
Output Low Current	I _{OL}	V _{OL} = 0.4V	VDD = 2.7V	4	11.5	mA
			VDD = 5.25V	6.4	15.3	mA
Three-State Leakage Current	I _{Leak}	nCS = VDD		± 0.1	± 1.0	μA
Three-State Output Capacitance	C _{OUT}	nCS = VDD		5		pF

1.4 Typical Operating Characteristics



(VDD = +5.0V; $f_{\text{Sample}} = 200\text{kHz}$, $f_{\text{CLK}} = 16 * f_{\text{Sample}} = 3.2\text{MHz}$; VREF = 2.500V applied to VREF pin; $\theta_{\text{OP}} = +25^\circ\text{C}$)



2 DETAILED DESCRIPTION

2.1 General Operation

The ZADCS146 / ZADCS147 are classic successive approximation register (SAR) type converters. The architecture is based on a capacitive charge redistribution DAC merged with a resistor string DAC building a hybrid converter with excellent monotonicity and DNL properties. The Sample & Hold function is inherent to the capacitive DAC. This avoids additional active components in the signal path that could distort the input signal or introduce errors.

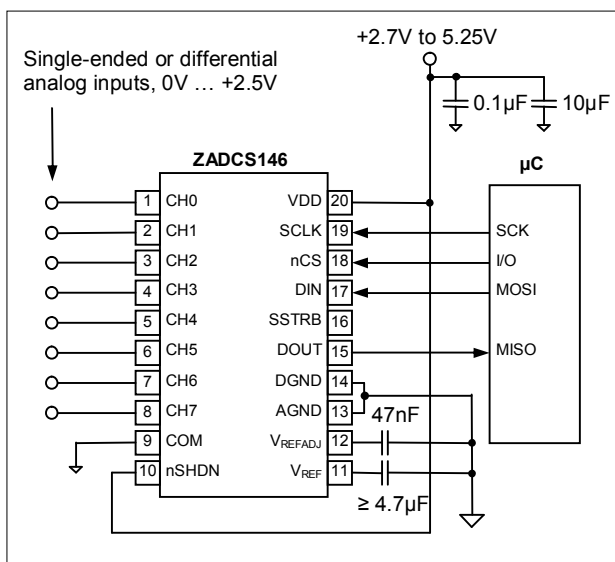
Both devices ZADCS146 / ZADCS147 build on the same converter core and differ only in the availability of an internal reference voltage generator. ZADCS146 is equipped with a highly accurate internal 1.25V bandgap reference which is available at the VREFADJ pin. The bandgap voltage is further amplified by an internal buffer amplifier to 2.50V that is available at pin VREF. ZADCS147 comes without the internal reference and the internal buffer amplifier. It requires an external reference supplied at VREF, with the benefit of considerably lower power consumption.

A basic application schematic of ZADC146 is shown in Figure 2, for ZADC147 in Figure 3. ZADCS146 can also be operated with an external reference, if VREFADJ is tied to VDD.

Table 3: Channel selection in Single Ended Mode (SGL/DIF = HIGH)

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	IN+								IN-
1	0	0		IN+							IN-
0	0	1			IN+						IN-
1	0	1				IN+					IN-
0	1	0					IN+				IN-
1	1	0						IN+			IN-
0	1	1							IN+		IN-
1	1	1								IN+	IN-

Figure 2: Basic application schematic for ZADCS146



2.2 Analog Input

The analog input to the converter is fully differential. Both converter input signals IN+ and IN- (see Functional Block diagram at front page) get sampled during the acquisition period enabling the converter to be used in fully differential applications where both signals can vary over time.

The ZADCS146 / ZADCS147 converters do not require that the negative input signal be kept constant within $\pm 0.5\text{LSB}$ during the entire conversion as is commonly required by converters featuring pseudo differential operation only.

The input signals can be applied single ended, referenced to the COM pin, or differential, using four pairs of the eight input channels. The desired configuration is selectable for every conversion via the Control-Byte received on DIN pin of the digital interface (see further description below)

A block diagram of the input multiplexer is shown in Figure 4. Table 3 and Table 4 show the relationship of the Control-Byte bits A2, A1, A0 and SGL/DIF to the configuration of the analog multiplexer.

Both input signals IN+ and IN- are generally allowed to swing between -0.2V and $\text{VDD}+0.2\text{V}$. However, depending on the selected conversion mode – unipolar or bipolar – certain input voltage relations can limit the output code range of the converter.

In unipolar mode the voltage at IN+ must exceed the

Table 4: Channel selection in Differential Mode (SGL/DIF = LOW)

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	IN+	IN-						
0	0	1			IN+	IN-				
0	1	0					IN+	IN-		
0	1	1							IN+	IN-
1	0	0	IN-	IN+						
1	0	1			IN-	IN+				
1	1	0					IN-	IN+		
1	1	1							IN-	IN+

Figure 3: Basic application schematic for ZADCS147

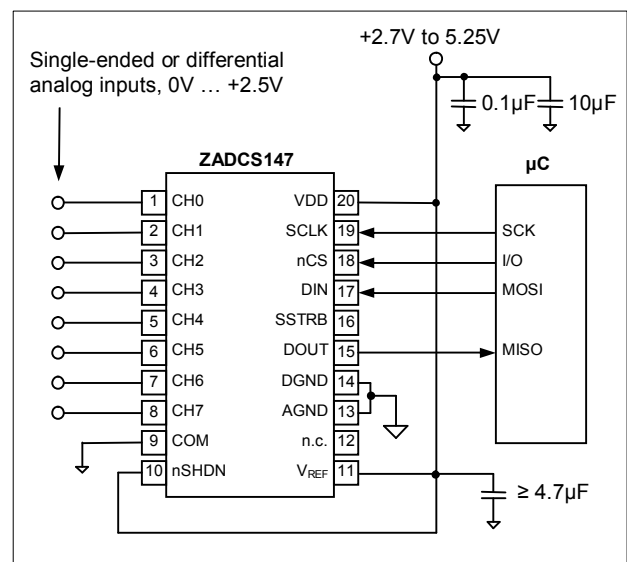
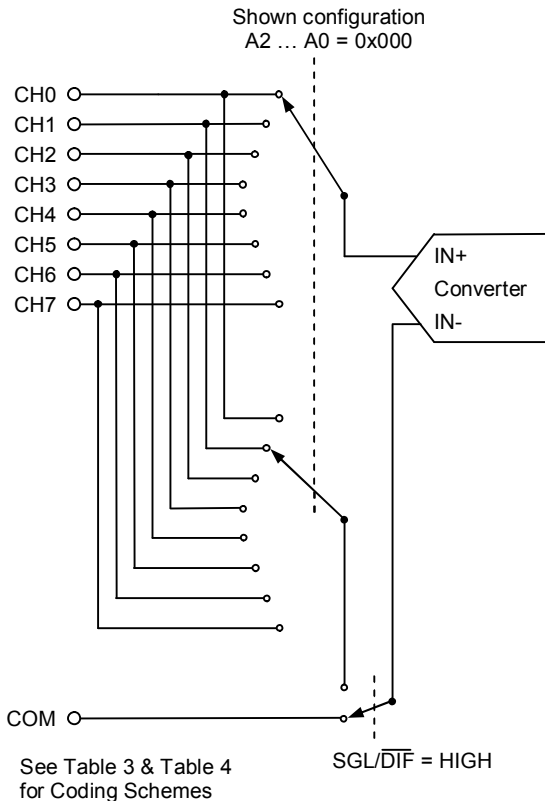


Figure 4: Block diagram of input multiplexer



voltage at IN₋ to obtain codes unequal to 0x000. The entire 12 bit transfer characteristic is then covered by IN₊ if IN₊ ranges from IN₋ to (IN₋ + V_{ref}). Any voltage on IN₊ > (IN₋ + V_{ref}) results in code 0xFFFF. Code 0xFFFF is not reached, if (IN₋ + V_{ref}) > V_{DD} + 0.2V because the input voltage is clamped at V_{DD} + 0.2V by ESD protection devices.

The voltage at IN₋ can range from -0.2V ... 1/2 V_{REF} without limiting the Code Range, assuming the fore mentioned V_{DD} condition is true. See also Figure 5 for input voltage ranges in unipolar conversion mode.

In bipolar mode, IN₊ can range from (IN₋ - V_{ref}/2) to (IN₋ + V_{ref}/2) keeping the converter out of code saturation. For instance, if IN₋ is set to a constant DC voltage of V_{ref}/2, then IN₊ can vary from 0V to V_{ref} to cover the entire code range. Lower or higher voltages of IN₊ keep the output code at the minimum or maximum code value.

Figure 6 shows the input voltage ranges in bipolar mode when IN₋ is set to a constant DC voltage.

As explained before, ZADCS146 / ZADCS147 can also be used to convert fully differential input signals that change around a common mode input voltage.

The bipolar mode is best used for such purposes since it allows the input signals to be positive or negative in relation to each other.

The common mode level of a differential input signal is calculated $V_{CM} = (V(IN_+) + V(IN_-)) / 2$. To avoid code clipping or over steering of the converter, the common mode level can change from 1/4 V_{ref} ... 3/4 V_{ref}. Within this range

Figure 5: Input voltage range in unipolar mode

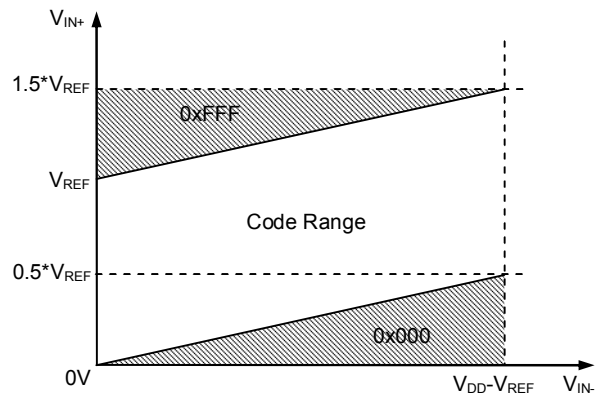
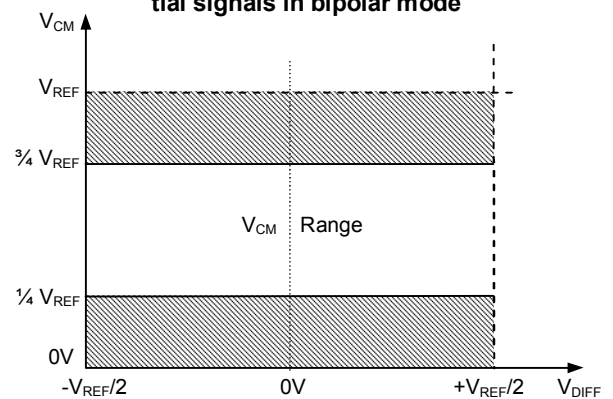


Figure 6: Input voltage range for fully differential signals in bipolar mode



the peak to peak amplitude of the differential input signal can be $\pm V_{ref}/2$.

The average input current on the analog inputs depends on the conversion rate. The signal source must be capable of charging the internal sampling capacitors (typically 16pF on each input of the converter: IN₊ and IN₋) within the acquisition time t_{ACQ} to the required accuracy. The equivalent input circuit in sampling mode is shown in Figure 7.

The following equation provides a rough hand calculation for a source impedance R_S that is required to settle out a DC input signal referenced to AGND with 12 bit accuracy in a given acquisition time

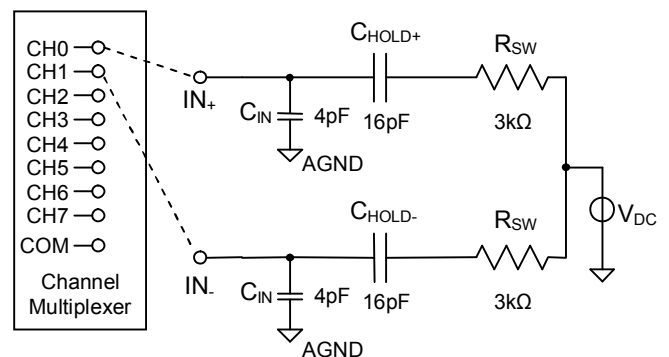


Figure 7: Equivalent input circuit during sampling

$$R_S \leq \frac{t_{ACQ}}{9 \times C_{IN}} - R_{SW}$$

For example, if $f_{SCLK} = 3.2\text{MHz}$, the acquisition time is $t_{ACQ} = 781.25\text{ns}$. Thus the output impedance of the signal source R_S must be less than

$$R_S \leq \frac{781.25\text{ns}}{9 \times 20\text{pF}} - 3\text{k}\Omega = 1.34\text{k}\Omega$$

If the output impedance of the source is higher than the calculated maximum R_S the acquisition time must be extended by reducing f_{SCLK} to ensure 12 bit accuracy. Another option is to add a capacitor of $>20\text{ nF}$ to the individual input. Although this limits the bandwidth of the input signal because an RC low pass filter is built together with the source impedance, it may be useful for certain applications.

The small-signal bandwidth of the input tracking circuitry is 3.8 MHz. Hence it is possible to digitize high-speed transient events and periodic signals with frequencies exceeding the ADC's sampling rate. This allows the application of certain under-sampling techniques like down conversion of modulated high frequency signals.

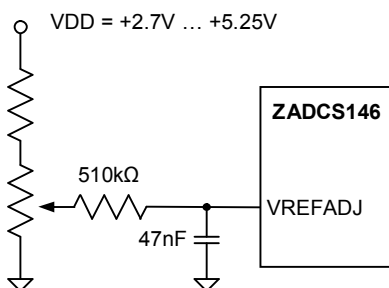
Be aware that under-sampling techniques still require a bandwidth limitation of the input signal to less than the Nyquist frequency of the converter to avoid aliasing effects. Also, the output impedance of the input source must be very low to achieve the mentioned small signal bandwidth in the overall system.

2.3 Internal & External Reference

ZADCS146 is equipped with a highly accurate internal 2.5V reference voltage source. The voltage is generated from a trimmed 1.25V bandgap with an internal buffer that is set to a gain of 2.00. The bandgap voltage is supplied at VREFADJ with an output impedance of 20kΩ. An external capacitor of 47nF at VREFADJ is useful to further decrease noise on the internal reference.

The VREFADJ pin also provides an opportunity to externally adjust the bandgap voltage in a limited range (see Figure 8) as well as the possibility to overdrive the internal bandgap with an external 1.25V reference.

Figure 8: Reference Adjust Circuit



The internal bandgap reference and the VREF buffer can be shut down completely by setting VREFADJ to VDD.

This reduces power consumption of the ZADCS146 and allows the supply of an external reference at VREF.

ZADCS147 does not contain the internal bandgap or the VREF buffer. An external reference must be supplied all the time at VREF.

The value of the reference voltage at VREF sets the input range of the converter and the analog voltage weight of each digital code. The size of the LSB (least significant bit) is equal to the value of VREF (reference to AGND) divided by 4096. For example at a reference voltage of 2.500V, the voltage level of a LSB is equal to 610μV.

It is important to know that certain inherent errors in the A/D converter, like offset or gain error, will appear to increase at lower reference voltages while the actual performance of the device does not change. For instance a static offset error of 1.22mV is equal to 2 LSB at 2.5V reference, while it is equivalent to 5.0 LSB for a reference voltage of 1.0V

Likewise, the uncertainty of the digitized output code will increase with lower LSB size (lower VREF). Once the size of an LSB is below the internal noise level, the output code will start to vary around a mean value for constant DC input voltages. Such noise can be reduced by averaging consecutive conversions or applying a digital filter.

The average current consumption at VREF depends on the value of VREF and the sampling frequency. Two effects contribute to the current at VREF, a resistive connection from VREF to AGND and charge currents that result from the switching and recharging of the capacitor array (CDAC) during sampling and conversion.

For an external reference of 2.5V the input current at VREF is approximately 100μA.

2.4 Digital Interface

ZADCS146 and ZADCS147 are both controlled by a 4-wire serial interface that is compatible to SPI™, QSPI™ and MICROWIRE™ devices without external logic.

Any conversion is started by sending a control byte into DIN while nCS is low. A typical sequence is shown in Figure 9.

The control byte defines the input channel(s), unipolar or bipolar operation and output coding, single-ended or differential input configuration, external or internal conversion clock and the kind of power down that is activated after the completion of a conversion. A detailed description of the control bits can be obtained from Table 5.

As it can also be seen in Figure 9 the acquisition of the input signal occurs at the end of the control byte for 2.5 clock cycles. Outside this range, the Track & Hold is in hold mode.

The conversion process is started, with the falling clock edge (SCLK) of the eighth bit in the control byte. It takes twelve clock cycles to complete the conversion and one additional cycle to shift out the last bit of the conversion result. During the remaining three clock cycles the output is filled with zeros in 24-Clock Conversion Mode.

Depending on what clock mode was selected, either the external SPI clock or an internal clock is used to drive the successive approximation. Figure 10 shows the Timing for Internal Clock Mode.

Figure 9: 24-Clock External Clock Mode Timing (SPI™, QSPI™ and MICROWIRE™ compatible, $f_{SCLK} \leq 3.2\text{MHz}$)

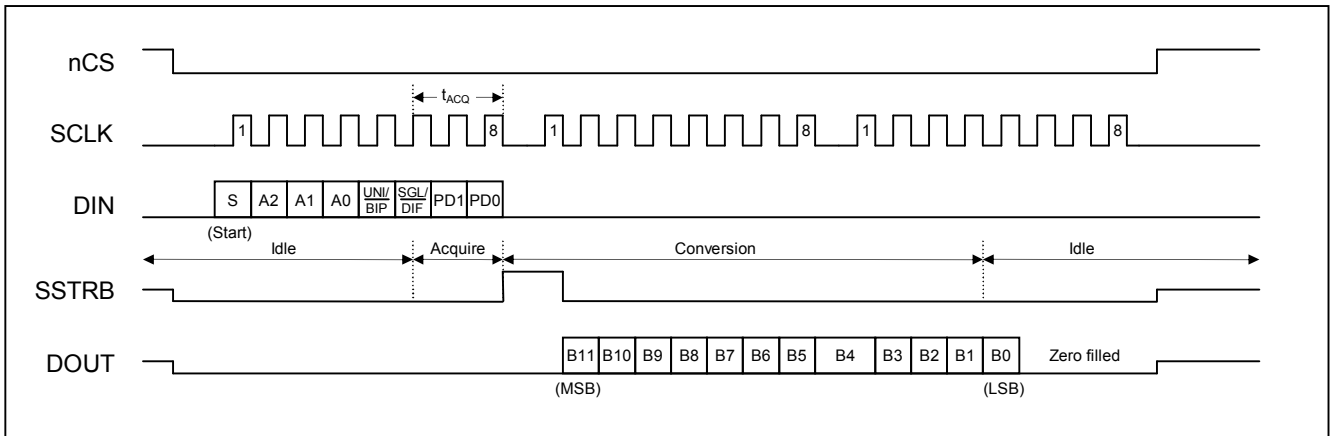


Figure 10: Internal Clock Mode Timing with interleaved Control Byte transmission

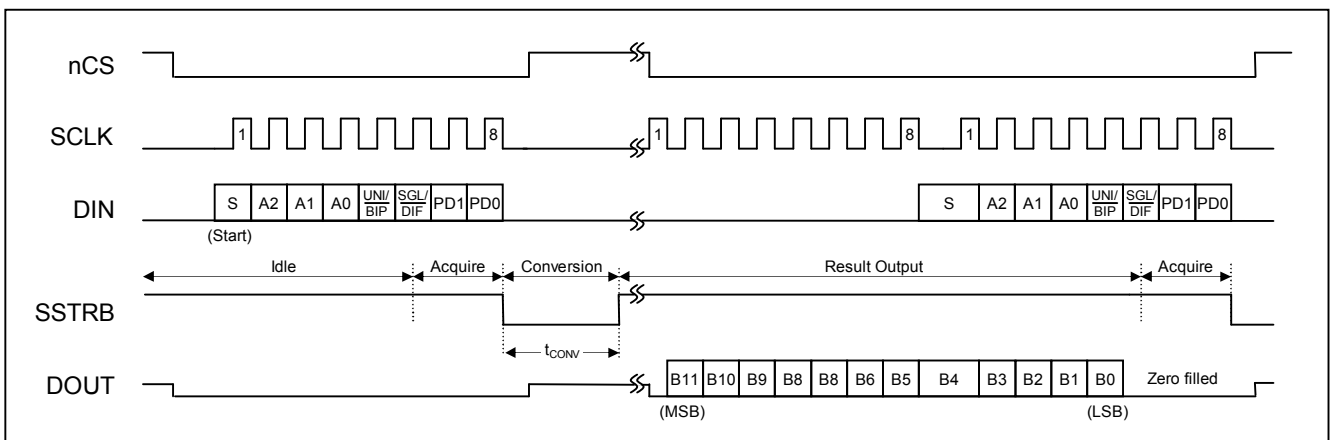


Table 5: Control Byte Format

BIT	Name	Description															
7 (MSB)	START	The Start Bit is defined by the first logic '1' after nCS goes low.															
6 5 4	A2 A1 A0	Channel Select Bits. Along with SGL/DIF these bits control the setting of the input multiplexer. For further details on the decoding see also Table 3 and Table 4.															
3	UNI/BIP	Output Code Select Bit. The value of the bit determines conversion mode and output code format. '1' = unipolar - straight binary coding '0' = bipolar - two's complement coding															
2	SGL/DIF	Single-Ended / Differential Select Bit. Along with the Channel Select Bits A2 .. A0 this bit controls the setting of the input multiplexer '1' = single ended - all channels CH0 ... CH7 measured referenced to COM '0' = differential - the voltage between two channels is measured															
1 0 (LSB)	PD1 PD0	Power Down and Clock Mode Select Bits <table border="1" style="display: inline-table; vertical-align: top;"> <thead> <tr> <th>PD1</th> <th>PD0</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Full Power-Down</td> </tr> <tr> <td>0</td> <td>1</td> <td>Fast Power-Down</td> </tr> <tr> <td>1</td> <td>0</td> <td>Internal clock mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>External clock mode</td> </tr> </tbody> </table>	PD1	PD0	Mode	0	0	Full Power-Down	0	1	Fast Power-Down	1	0	Internal clock mode	1	1	External clock mode
PD1	PD0	Mode															
0	0	Full Power-Down															
0	1	Fast Power-Down															
1	0	Internal clock mode															
1	1	External clock mode															

Figure 11: 16-Clock External Clock Mode Conversion

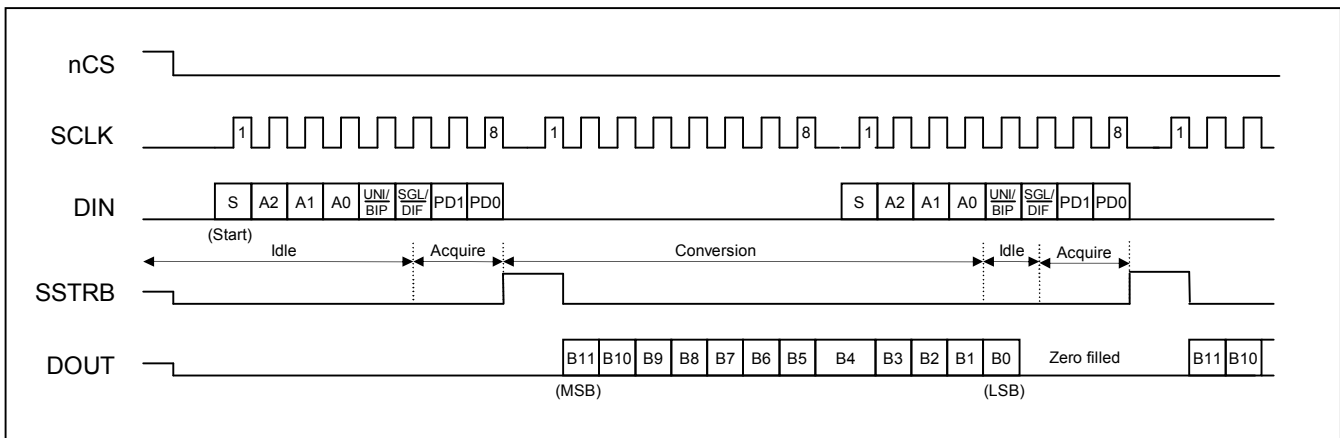
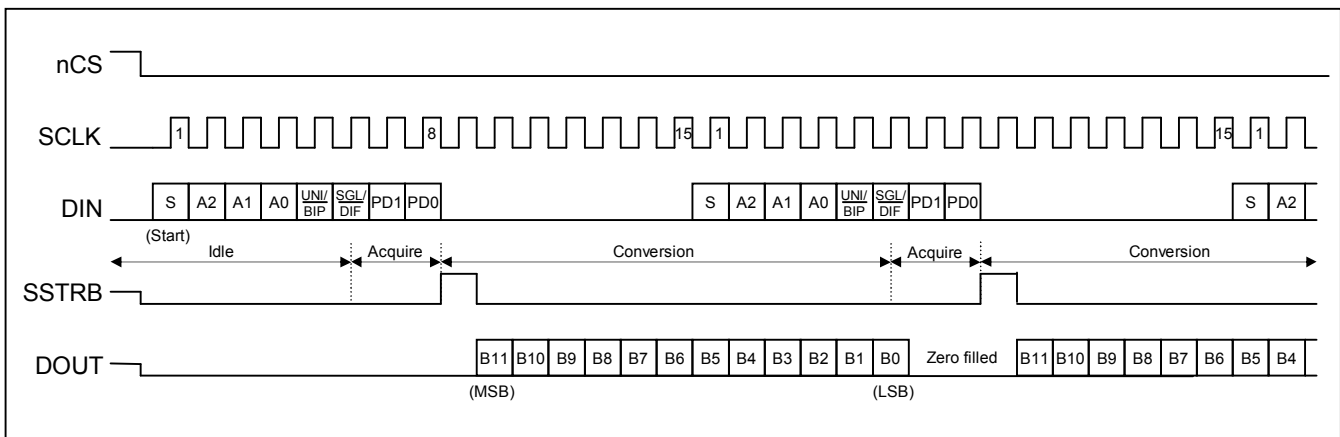


Figure 12: 15-Clock External Clock Mode Conversion



Internal Clock Mode

In Internal Clock Mode, the conversion starts at the falling clock edge of the eighth control bit just as in External Clock Mode. However, there are no further clock pulses required at SCLK to complete the conversion. The conversion clock is generated by an internal oscillator that runs at approximately 3.2MHz. While the conversion is running, the SSTRB signal is driven LOW. As soon as the conversion is complete, SSTRB is switched to HIGH, signaling that the conversion result can be read out on the serial interface.

To shorten cycle times ZADCS146 and ZADCS147 allow interleaving of the read out process with the transmission of a new control byte. Thus it is possible to read the conversion result and to start a new conversion with just two consecutive byte transfers, instead of three bytes that would have to be send without the interleaving function.

While the IC is performing a conversion in Internal Clock Mode, the Chip Select signal (nCS) may be tied HIGH allowing other devices to communicate on the bus. The output driver at DOUT is switched into a high impedance state while nCS is HIGH. The conversion time t_{CONV} may vary in the specified limits depending on the actual VDD and temperature values.

16-Clocks per Conversion

Interleaving of the data read out process and transmission of a new Control Byte is also supported for External Clock Mode operation. Figure 11 shows the transmission timing for conversion runs using 16 clock cycles per run. In fact, the specified converter sampling rate of 200ksps will be reached in this mode, provided the clock frequency is set to 3.2MHz.

15-Clocks per Conversion

ZADS146 and ZADCS147 do also support a 15 clock cycle conversion mode (see Figure 12). This is the fastest conversion mode possible. Usually micro controllers do not support this kind of 15 bit serial communication transfers. However, specifically designed digital state machines implemented in Field Programmable Gate Arrays (FPGA) or Application Specific Integrated Circuits (ASIC) may use this operation mode. Applications that utilize the 15 clock cycle conversion mode gain an increase in sampling rate to 213.3ksps keeping the clock frequency unchanged at 3.2MHz.

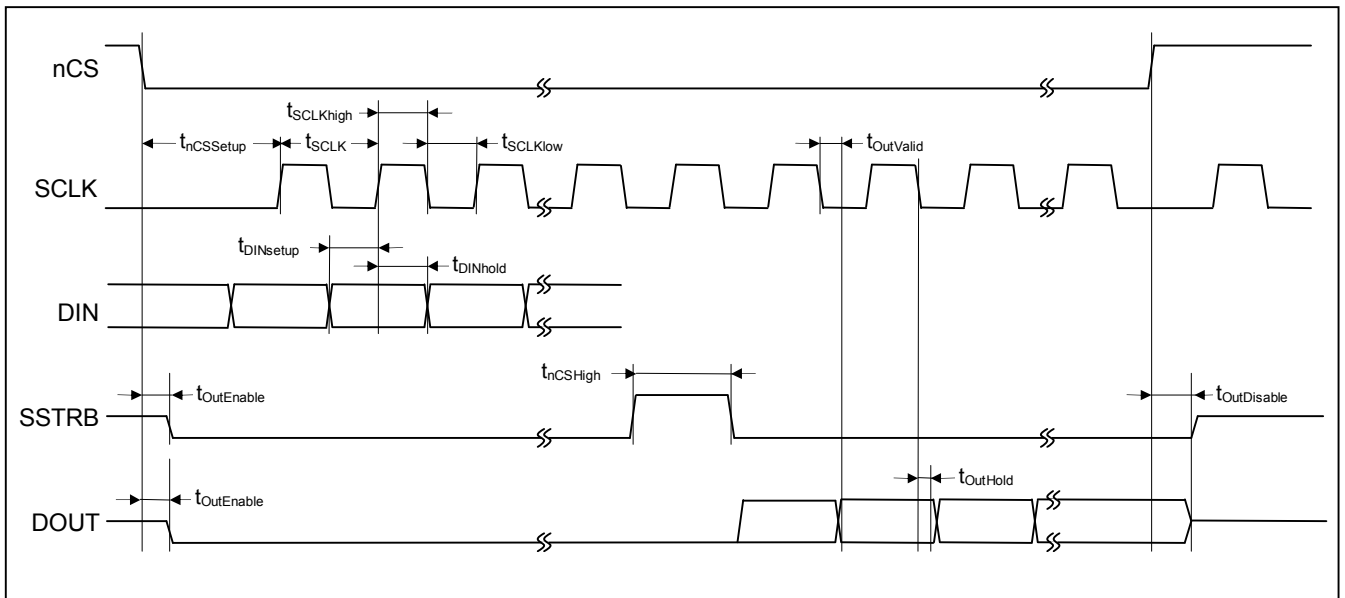
Digital Timing

In general the clock frequency at SCLK may vary from 0.1MHz to 3.2MHz. Considering all telegram pauses or other interruptions of a continuous clock at SCLK, each conversion must be completed within 1.2ms from the

Table 6: ZADCS146 / ZADCS147 Timing Characteristics ($V_{DD} = +2.7V$ to $+5.25V$; $\theta_{OP} = \theta_{OPmin} \dots \theta_{OPmax}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCLK Periode	t_{SCLK}		312.50			ns
SCLK Pulse Width High	$t_{SCLKhigh}$		156.25			ns
SCLK Pulse Width Low	$t_{SCLKlow}$		156.25			ns
DIN to SCLK Setup	$t_{DinSetup}$		30			ns
DIN to SCLK Hold	$t_{DinHold}$		10			ns
nCS Fall to SCLK Setup	$t_{nCSSetup}$		30			ns
SCLK Fall to DOUT & SSTRB Hold	$t_{OutHold}$	$C_{Load} = 20pF$	10			ns
SCLK Fall to DOUT & SSTRB Valid	$t_{OutValid}$	$C_{Load} = 20pF$			40	ns
nCS Rise to DOUT & SSTRB Disable	$t_{OutDisable}$	$C_{Load} = 20pF$	10		60	ns
nCS Fall to DOUT & SSTRB Enable	$t_{OutEnable}$	$C_{Load} = 20pF$			60	ns
nCS Pulse Width High	$t_{nCSHigh}$		100			ns

Figure 13: Detailed Timing Diagram



falling clock edge of the eighth bit in the Control Byte. Otherwise the signal that was captured during sample/hold may drop to noticeable affect the conversion result.

Further detailed timing information on the digital interface is provided in Table 6 and Figure 13.

Output Code Format

ZADCS146 and ZADCS147 both support unipolar and bipolar operation modes. The digital output code is straight binary in unipolar mode. It ranges from 0x000 for an input voltage difference of 0V to 0xFFF for an input

voltage difference of V_{REF} (Full Scale = FS). The first code transition (0x000 → 0x001) occurs at a voltage equivalent to $\frac{1}{2}$ LSB, the last (0xFFE → 0xFFFF) at $V_{REF} - 1.5$ LSB. See also Figure 14 for details.

In bipolar mode a two's complement coding is applied. Code transitions occur again halfway between successive integer LSB values. The transfer function is shown in Figure 15.

Figure 14: Unipolar Transfer Function

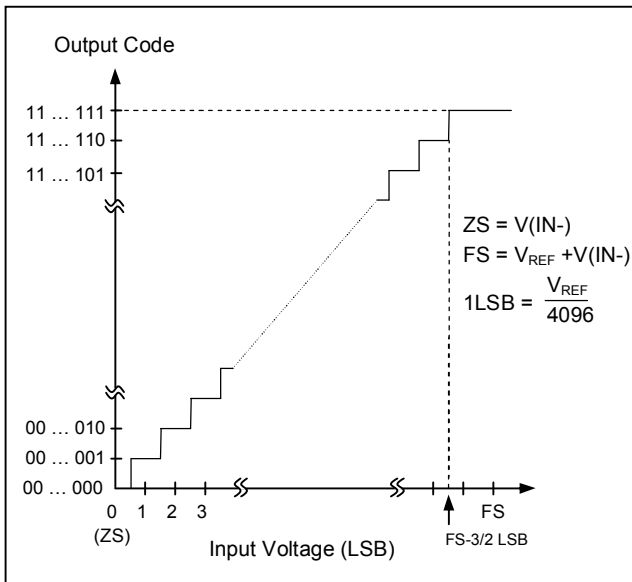
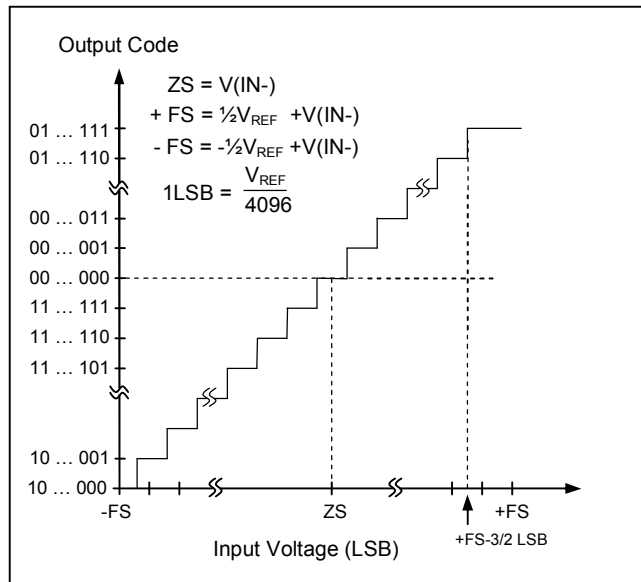


Figure 15: Bipolar Transfer Function



2.5 Power Dissipation

ZADCS146 and ZADCS147 offer three different ways to save operating current between conversions. Two different software controlled power down modes can be activated to automatically shut-down the device after completion of a conversion. They differ in the amount of circuitry that is powered down.

Software Power Down

Full Power Down Mode shuts down the entire analog part of the IC, reducing the static I_{DD} of the device to less than $0.5\mu A$ if no external clock is provided at SCLK.

Fast Power Down mode is only useful with ZADCS146 if the internal voltage reference is used. During Fast Power-Down the bandgap and the VREFADJ output buffer are kept alive while all other internal analog circuitry is shut down. The benefit of Fast Power Down mode is a shorter turn on time of the reference compared to Full Power Down Mode. This is basically due to the fact that the low pass which is formed at the VREFADJ output by the internal $20k\Omega$ resistor and the external buffer capacitor of $47nF$ is not discharged in Fast Power Down Mode.

The settling time of the low pass at VREFADJ is about 9 ms to reach 12 bit accuracy. The Fast Power Down mode omits this settling and reduces the turn on time to about $200\mu s$.

To wake up the IC out of either software power down mode, it is sufficient to send a Start Bit while nCS is LOW. Since micro controllers can commonly transfer full bytes per transaction only, a dummy conversion is usually carried out to wake the device.

In all application cases where an external reference voltage is supplied (ZADCS147 and ZADCS146 with VREFADJ tied to VDD) there is no turn on time to be considered. The first conversion is already valid. Fast Power-Down and Full Power-Down Mode do not show any difference in this configuration.

Hardware Power Down

The third power down mode is called Hardware Power-Down. It is initiated by pulling the nSHDN pin LOW. If this condition is true, the device will immediately shut down all circuitry just as in Full Power Down-Mode.

The IC wakes up if nSHDN is tied HIGH. There is no internal pull-up that would allow nSHDN to float during normal operation. This ensures the lowest possible power consumption in power down mode.

General Power Considerations

Even without activating any power down mode, ZADCS146 and ZADCS147 reduce their power consumption between conversions automatically. The comparator, which contributes a considerable amount to the overall current consumption of the device is shut off as soon as a conversion is ended. It gets turned on at the start of the next acquisition period. This explains the difference between the $I_{DDstatic}$ and $I_{DDactive}$ measurements shown in chapter 1.4 Typical Operating Characteristics.

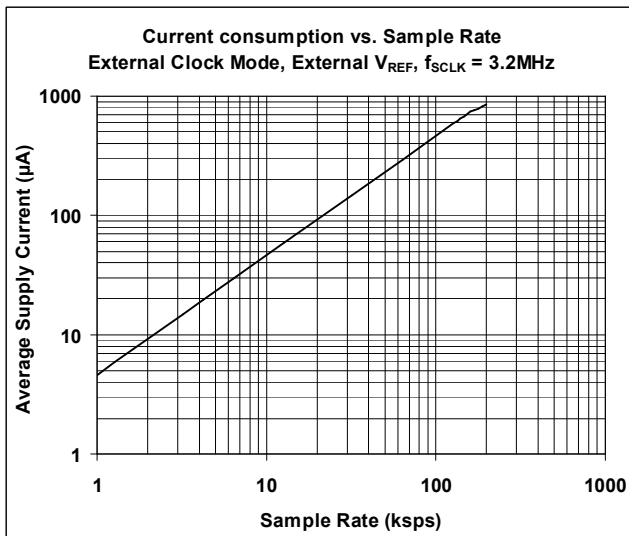
The average current consumption of the device depends very much on the sampling frequency and the type of protocol used to communicate with the device.

In order to achieve the lowest power consumption at low sampling frequencies, it is suggested to keep the conversion clock frequency at the maximum level of 3.2MHz and to power down the device between consecutive conversions. Figure 16 shows the characteristic current consumption of ZADCS146 and ZADCS147 with external reference supply versus Sampling Rate

3 Layout

To achieve optimum conversion performance care must be taken in design and layout of the application board. It is highly recommended to use printed circuit boards instead of wire wrap designs and to establish a single point star connection ground system towards AGND (see Figure 17).

Figure 16: Average Supply Current versus Sampling Rate



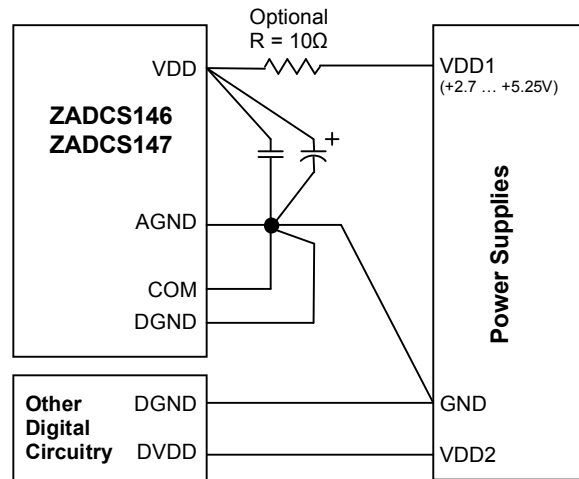
For optimal noise performance the star point should be located very close to the AGND pin of the converter. The ground return to the power supply should be as short as possible and low impedance.

All other analog ground points of external circuitry that is related to the A/D converter as well as the DGND pin of the device should be connected to this ground point too. Any other digital ground system should be kept apart as far as possible and connect on the power supply point only.

Analog and digital signal domains should also be separated as well as possible and analog input signals should be shielded by AGND ground planes from electromagnetic interferences. Four-layer PCB boards that allow smaller vertical distances between the ground plane and the shielded signals do generally show a better performance than two-layer boards.

The sampling phase is the most critical portion of the overall conversion timing for signal distortion. If possible, the switching of any high power devices or nearby digital logic should be avoided during the sampling phase of the converter.

Figure 17: Optimal Power-Supply Grounding System



The fully differential internal architecture of ZADCS146 and ZADCS147 ensures very good suppression of power supply noise. Nevertheless, the SAR architecture is generally sensitive to glitches or sudden changes of the power supply that occur shortly before the latching of the comparator output. It is therefore recommended to bypass the power supply connection very close to the device with capacitors of 0.1µF (ceramic) and >1µF (electrolytic).

In case of a noisy supply, an additional series resistor of 5 to 10 ohms can be used to low-pass filter the supply voltage.

The reference voltage should always be bypassed with capacitors of 0.1µF (ceramic) and ≥ 4.7µF (electrolytic) as close as possible to the VREF pin. If VREF is provided by an external source, any series resistance in the VREF supply path can cause a gain error of the converter. During conversion, a DC current of about 100µA is drawn through the VREF pin that could cause a noticeable voltage drop across the resistance.

4 Package Drawing

The IC is packaged in a 20 pin SSOP-package that has the dimensions as shown in Figure 18 and Table 7.

Figure 18: Package Outline Dimensions

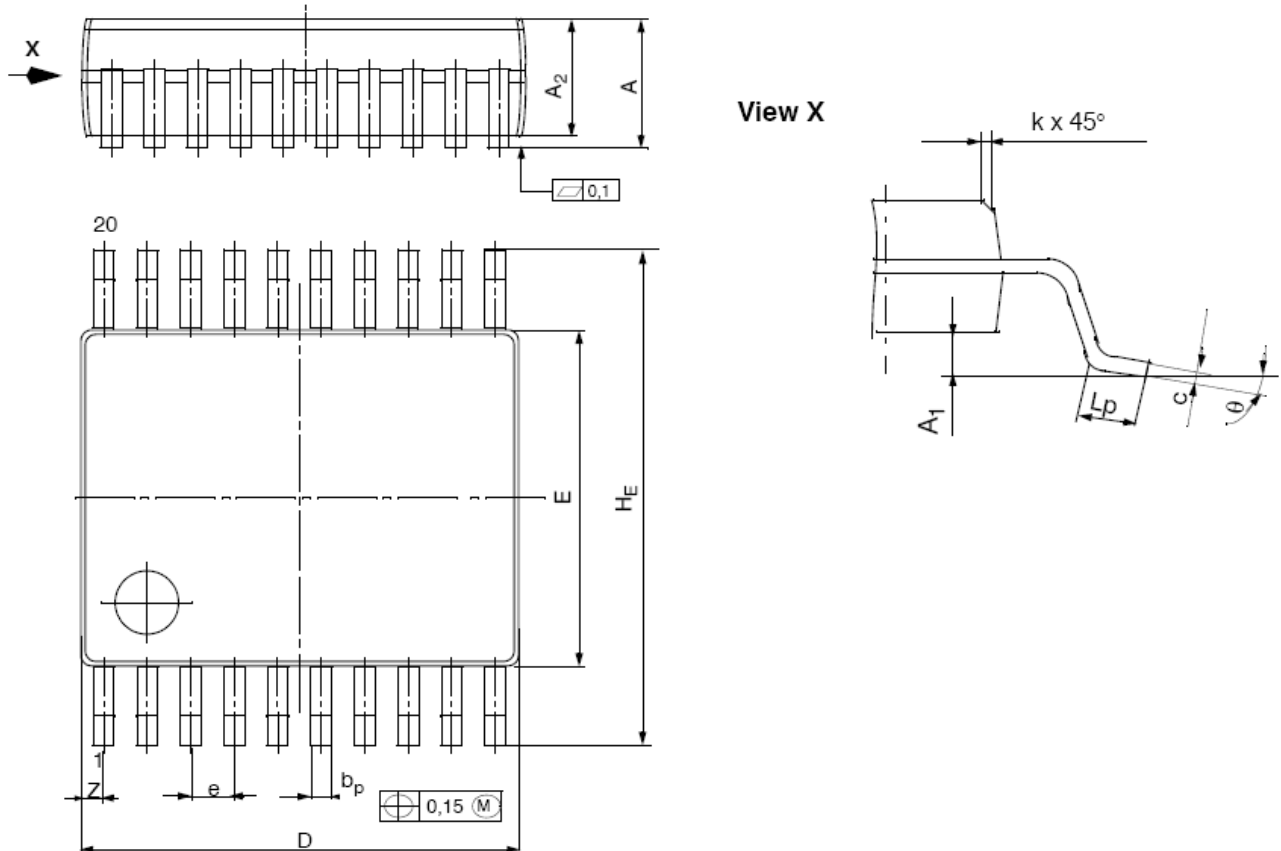


Table 7: Package Dimensions (mm)

Symbol	A	A ₁	A ₂	b _p	c	D	E	e _{nom}	H _E	L _p	Z	k	θ	
Nominal	1.86	0.13	1.73	0.30	0.15	7.20	5.30	0.65	7.80				4°	
Maximum	1.99	0.21	1.78	0.38	0.20	7.33	5.38		7.90		0.74			8°
Minimum	1.73	0.05	1.68	0.25	0.09	7.07	5.20		7.65	0.63		0.25		0°

5 Ordering Information

Order Code	Resolution [Bit]	Channels [number]	Sample Rate [ksps]	Temperature range [°C]	QC 100 Qualified	Internal V _{ref}	INL	DNL	Pins [number]	Package [Type]	packing
ZADCS146VIS20T	12	8	200	-25°C to +85°C	--	✓	± 1 LSB	± 1 LSB	20	SSOP	Tube
ZADCS147IS20T	12	8	200	-25°C to +85°C	--	--	± 1 LSB	± 1 LSB	20	SSOP	Tube

6 ZMD Distribution Partner

ZMD ADC products as well as the ZADCS146/ZADCS147 Starterkit can be purchased from RUTRONIK Elektronische Bauelemente GmbH.

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