SamHop Microelectronics Corp.

STA6620

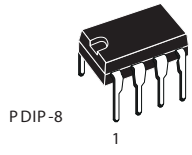
Nov. 24 2006

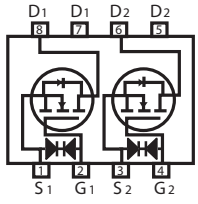
Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V_{DSS}	I_D	$R_{DS(ON)}$ (mΩ) Max
40V	7A	25 @ V_{GS} = 10V 42 @ V_{GS} = 4.5V

FEATURES

- Super high dense cell design for low $R_{DS(ON)}$.
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.





ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous [a] @ Ta	25°C	I_D	7	A
	70°C		5.9	A
-Pulsed [b]		I_{DM}	30	A
Drain-Source Diode Forward Current [a]		I_S	1.7	A
Maximum Power Dissipation [a]	Ta= 25°C	P_D	3	W
	Ta=70°C		2	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient [a]	$R_{\theta JA}$	41.5	°C/W

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N-Channel ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ [c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=32V, V_{GS}=0V			1	uA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}= 0V			±10	nA
ON CHARACTERISTICS [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D = 250uA	1	2	3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D =7A		19	25	m ohm
		V_{GS}=4.5V, I_D= 5A		28	42	m ohm
On-State Drain Current	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	15			A
Forward Transconductance	g_{FS}	V_{DS} = 5V, I_D = 7A		13		S
DYNAMIC CHARACTERISTICS [c]						
Input Capacitance	C_{ISS}	V_{DS}=25V, V_{GS} = 0V f=1.0MHz		710		pF
Output Capacitance	C_{OSS}			110		pF
Reverse Transfer Capacitance	C_{RSS}			68		pF
SWITCHING CHARACTERISTICS [c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 20V I_D = 1 A V_{GS} = 10V R_{GEN} = 3.3 ohm		16.5		ns
Rise Time	t_r			14		ns
Turn-Off Delay Time	$t_{D(OFF)}$			40		ns
Fall Time	t_f			6.5		ns
Total Gate Charge	Q_g	V_{DS} =20V, I_D =7A,V_{GS} =10V		13.3		nC
		V_{DS} =20V, I_D =7A,V_{GS} =4.5V		6.7		nC
Gate-Source Charge	Q_{gs}	V_{DS} =20V, I_D = 7 A V_{GS} =4.5V		2		nC
Gate-Drain Charge	Q_{gd}			3.7		nC

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS [b]						
Diode Forward Voltage	V_{SD}	V_{GS} = 0V, Is =1.7A		0.8	1.2	V

Notes

a.Surface Mounted on FR4 Board, t≤10sec.
b.Pulse Test:Pulse Width≤ 300us, Duty Cycle≤ 2%.
c.Guaranteed by design, not subject to production testing.

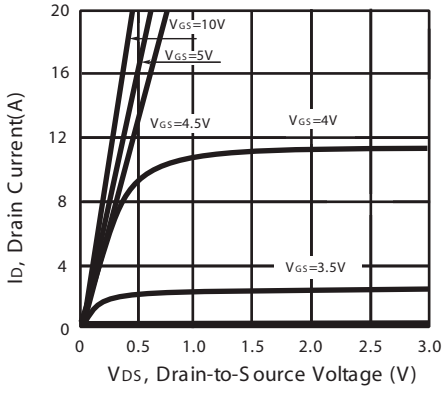


Figure 1. Output Characteristics

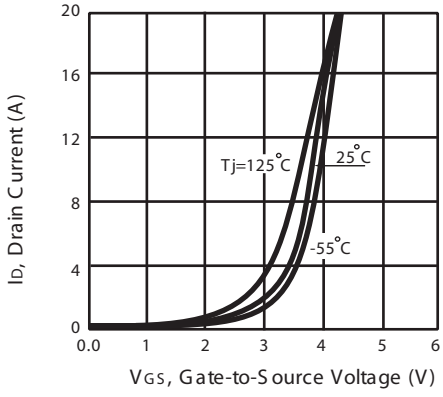


Figure 2. Transfer Characteristics

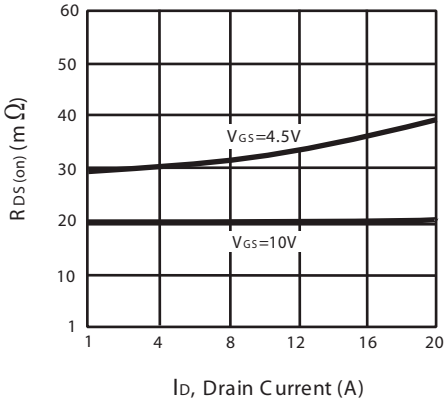


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

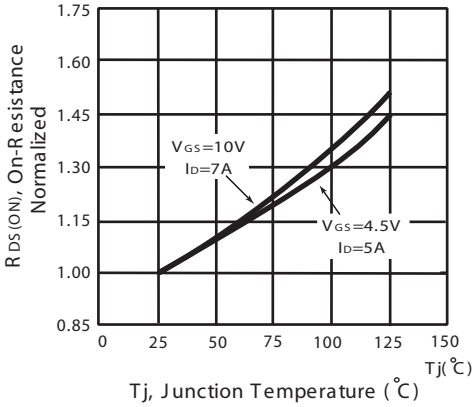


Figure 4. On-Resistance Variation with Drain Current and Temperature

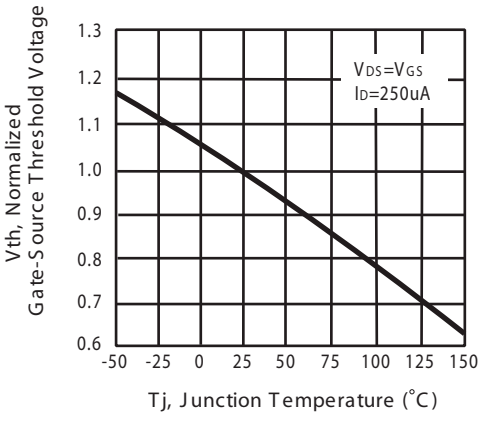


Figure 5. Gate Threshold Variation with Temperature

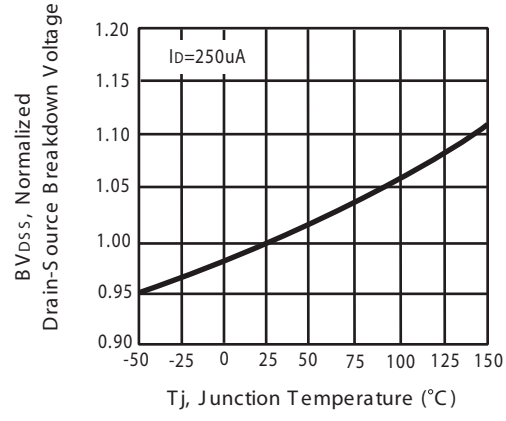


Figure 6. Breakdown Voltage Variation with Temperature

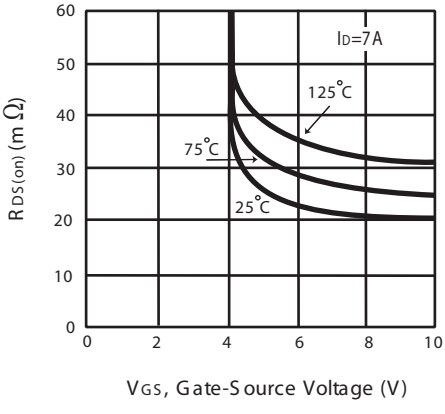


Figure 7. On-Resistance vs. Gate-Source Voltage

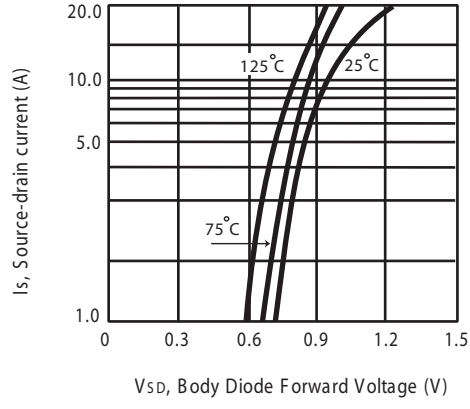


Figure 8. Body Diode Forward Voltage Variation with Source Current

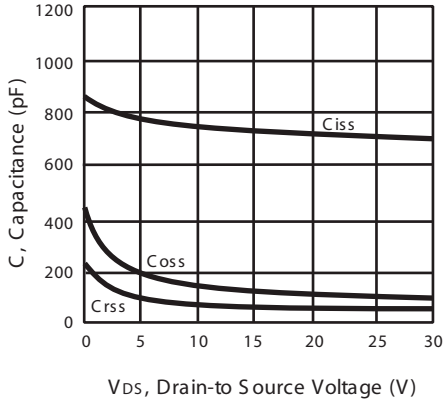


Figure 9. Capacitance

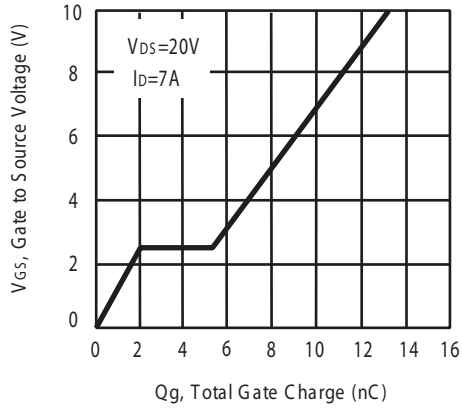


Figure 10. Gate Charge

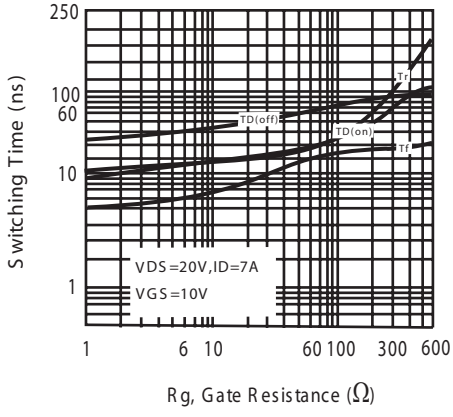


Figure 11.switching characteristics

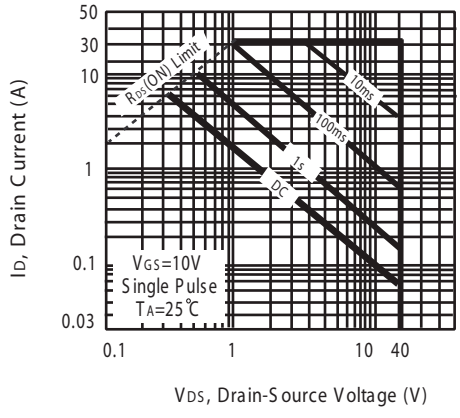
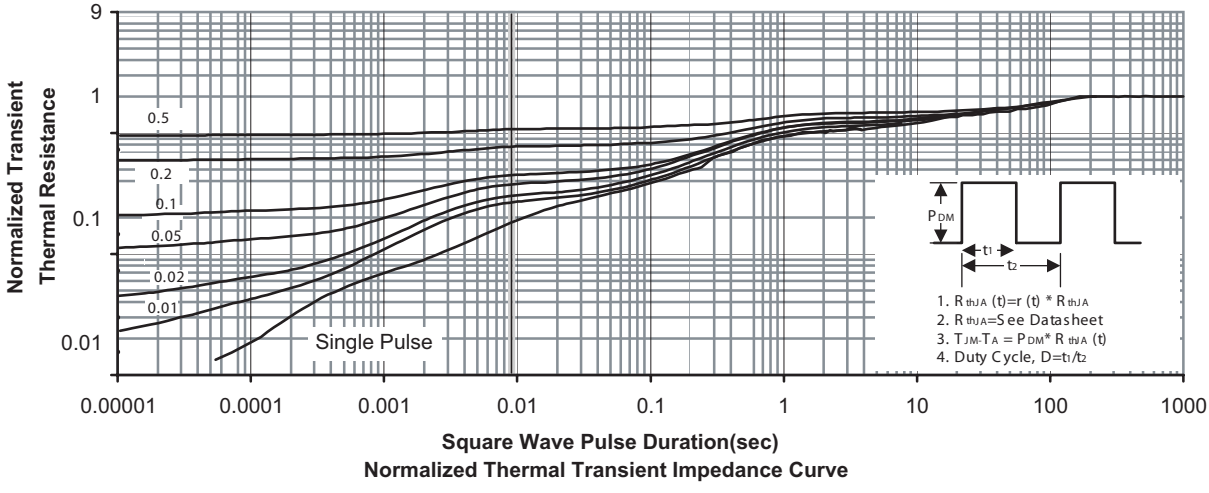


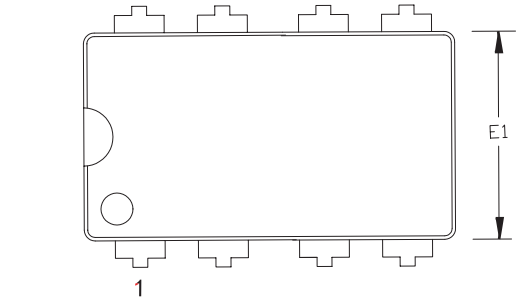
Figure 12. Maximum Safe Operating Area



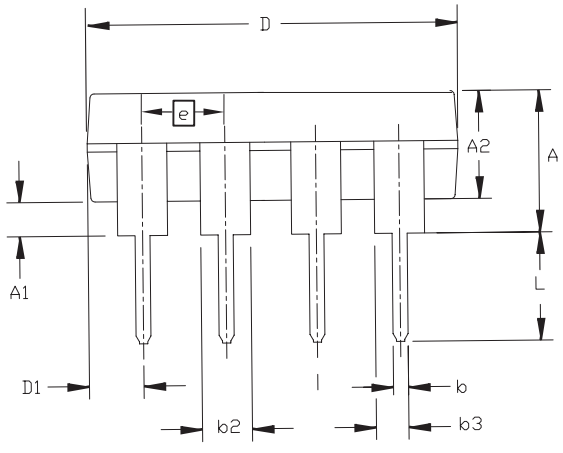
Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE DIMENSIONS

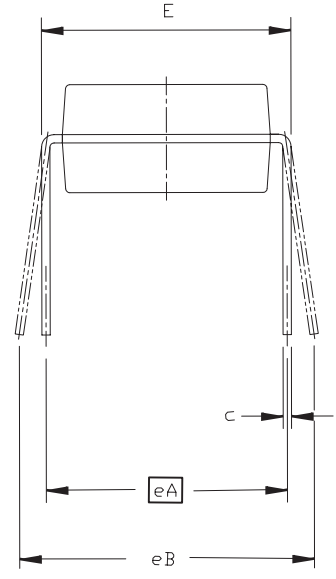
PDIP 8



TOP VIEW



FRONT VIEW



SIDE VIEW

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	.145	.172	.200	3.68	4.37	5.08
A1	.020	-	-	0.51	-	-
A2	.125	.130	.135	3.18	3.30	3.43
b	.015	.018	.021	0.38	0.46	0.53
c	.009	.012	.014	0.23	0.30	0.36
b2	.045	.060	.070	1.14	1.52	1.78
b3	.030	.039	.045	0.76	0.99	1.14
L	.125	.132	.140	3.18	3.35	3.56
e	.090	.100	.110	2.29	2.54	2.79
D	.373	.386	.400	9.47	9.80	10.16
D1	.030	.045	.060	0.76	1.14	1.52
E	.300	.310	.320	7.62	7.87	8.13
E1	.245	.250	.255	6.22	6.35	6.48
eA	.280	-	-	7.11	-	-
eB	.310	.325	.365	7.87	8.26	9.27