M65667FP

Picture-in-Picture Signal Processing

REJ03F0185-0201
Rev.2.01
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Description

The M65667FP is a NTSC PIP (Picture in Picture) signal processing LSI, whose sub and main-picture inputs are composite and Y/C separated signals, respectively. The built-in field memory (96 Kbit RAM), V-chip data slicer and analog circuitries lead the PIP system low cost and small size.

Features

- Built-in 96 Kbit field memory (sub-picture data storage)
- Internal V-chip data slicer (for sub-picture)
- Vertical filter for sub-picture (Y signal)
- Single sub-picture (selectable picture size: 1/9, 1/16)
- Sub-picture processing specification (1/9 size / 1/16 size)
  - Quantization bits Y, B-Y, R-Y: 6 bits
  - Horizontal sampling 171 pixels (Y), 28.5 pixels (B-Y, R-Y)
  - Vertical lines 69/52 lines
- Frame (sub-picture) on/off
- Built-in analog circuits
  - Two 8-bit A/D converters (main and sub-picture signals)
  - Two 8-bit D/A converters (Y and C sub-picture signals)
  - Sync-tip-clamp, VCXO, Analog switch, etc.
- I^2C BUS control (parallel/serial control)
  PIP on/off, Sub-picture size (1/9 or 1/16), Frame on/off (programmable luma level), PIP position (4 corners fixed position), Picture freeze, Y delay adjustment, Chroma level, Tint, Black level, Contrast, etc.

Application

NTSC color TV

Recommended Operating Condition

Supply voltage range ..... 3.1 to 3.5 V

Operating frequency ..... 14.32 MHz

Operating temperature ..... –20 to 75°C

Input voltage (CMOS interface) "H" ..... Vdd ± 0.7 to Vdd V

"L" ..... 0 to Vdd ± 0.3 V

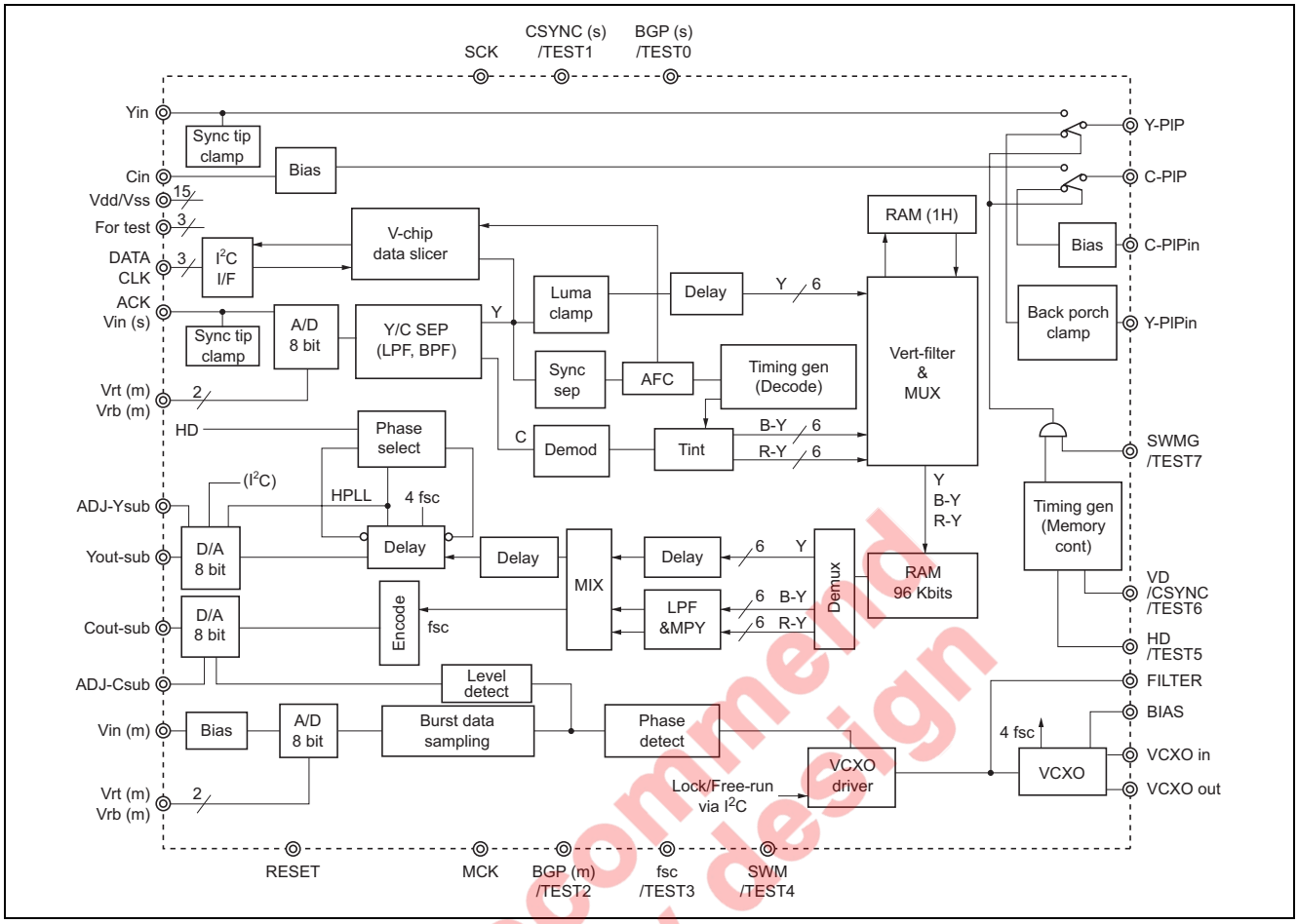
Output current (output buffer) ..... 4 mA (Max)

Output load capacitance ..... 20 pF (Max) Note2

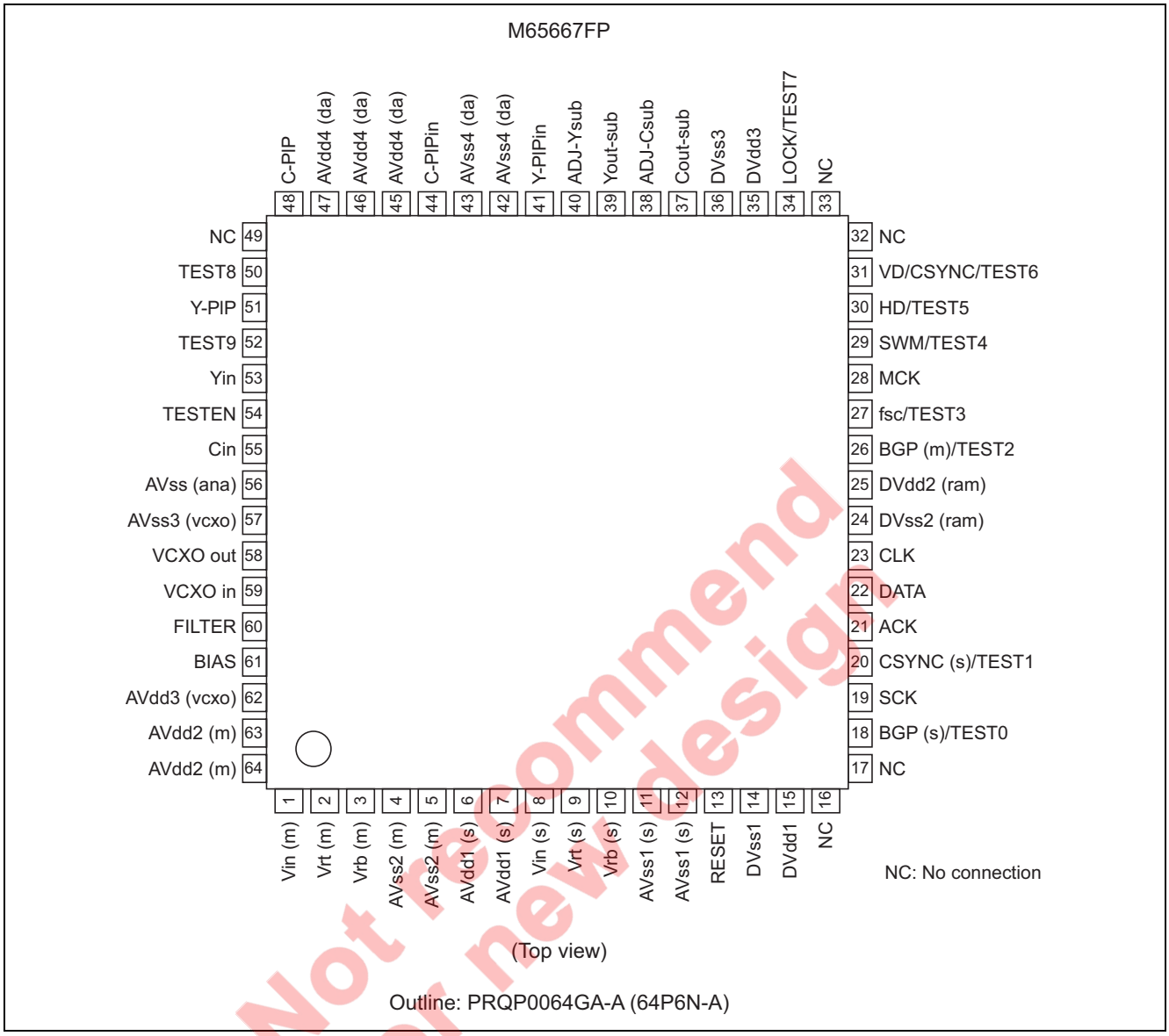
Circuit current ..... 160 mA

Notes: 1. Connect a 0.1 µF or larger capacitor between Vdd and Vss pins.
2. Include pin capacitance (7 pF)

Block Diagram



Pin Arrangement



Pin Description

Pin No.	Name	I/O	Function	Remarks
1	Vin (m)	I	Chroma signal input (main-picture)	
2	Vrt (m)	O	A/D Vref+ (main-picture)	
3	Vrb (m)	O	A/D Vref– (main-picture)	
4	AVss2 (m)	GND	Connect to analog GND	
5	AVss2 (m)	GND	Connect to analog GND	
6	AVdd1 (s)	Vdd	Connect to analog power supply	
7	AVdd1 (s)	Vdd	Connect to analog power supply	
8	Vin (s)	I	Composite video signal input (sub-picture)	
9	Vrt (s)	O	A/D Vref+ (sub-picture)	
10	Vrb (s)	O	A/D Vref– (sub-picture)	
11	AVss1 (s)	GND	Connect to analog GND	
12	AVss1 (s)	GND	Connect to analog GND	
13	RESET	I	Power on reset input signal ("L" reset)	100 kΩ to Vdd, 10 μF to GND
14	DVss1	GND	Connect to digital GND	
15	DVdd1	Vdd	Connect to digital power supply	
16	NC	—	No connection	
17	NC	—	No connection	
18	BGP (s) /TEST0	(I/) O	For test	Non connect
19	SCK	I	For test (connect to digital GND)	Connect to GND
20	CSYNC (s) /TEST1	I (/O)	For test (connect to digital GND)	Pull down 15 kΩ
21	ACK	O	I^2C bus-data/Acknowledge output signal	
22	DATA	I	I^2C bus-data input signal	
23	CLK	I	I^2C bus-clock input signal	
24	DVss2 (ram)	GND	Connect to digital GND	
25	DVdd2 (ram)	Vdd	Connect to digital power supply	
26	BGP (m) /TEST2	(I/) O	For test	Non connect
27	fsc/TEST3	I (/O)	For test (pull down to digital GND by resistor 15 kΩ)	Pull down 15 kΩ
28	MCK	I	For test (connect to digital GND)	Connect to GND
29	SWM/TEST4	(I/) O	For test	Non connect
30	HD/TEST5	I (/O)	Horizontal sync input signal (Positive going edge is used)	
31	VD/CSYNC/TEST6	I (/O)	Vertical sync input signal (active "H")	
32	NC	—	No connection	
33	NC	—	No connection	
34	SWMG/TEST7	I (/O)	Enable input signal to display sub picture ("H" enable)	Pull down 15 kΩ
35	DVdd3	Vdd	Connect to digital power supply	
36	DVss3	GND	Connect to digital GND	
37	Cout-sub	O	D/A output signal (Chroma signal of sub-picture)	
38	ADJ-Csob	I	D/A adjust for chroma signal (sub-picture)	
39	Yout-sub	O	D/A output signal (Luma signal of sub-picture)	
40	ADJ-Ysub	I	D/A adjust for luma signal (sub-picture)	
41	Y-PIPin	I	PIP luma signal re-input	
42	AVss4 (da)	GND	Connects to analog GND	
43	AVss4 (da)	GND	Connects to analog GND	
44	C-PIPin	I	PIP chroma signal re-input	
45	AVdd4 (da)	Vdd	Connect to analog power supply	
46	AVdd4 (da)	Vdd	Connect to analog power supply	
47	AVdd4 (da)	Vdd	Connect to analog power supply	
48	C-PIP	O	PIP chroma signal output	

Pin Description (cont.)

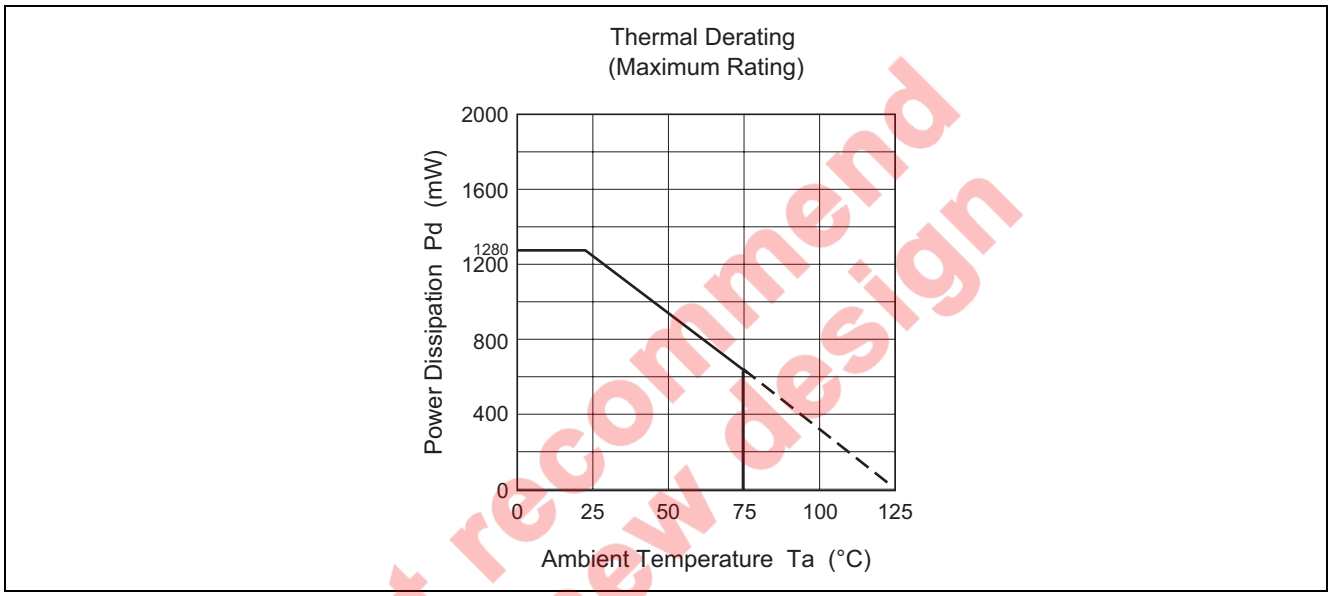
Pin No.	Name	I/O	Function	Remarks
49	NC	—	No connection	
50	TEST8	I	For test (connect to analog GND)	Pull up 15 kΩ
51	Y-PIP	O	PIP luma signal output	
52	TEST9	I	For test (connect to analog GND)	Connect to GND
53	Yin	I	Luma input signal (main-picture)	
54	TESTEN	I	For test (connect to analog GND)	Connect to GND
55	Cin	I	Chroma input signal (main-picture)	
56	AVss (ana)	GND	Connect to analog GND	
57	AVss3 (vcxo)	GND	Connects to analog GND	
58	VCXO out	O	VCXO output signal	
59	VCXO in	I	VCXO input signal	
60	FILTER	I	Filter	
61	BIAS	O	Bias	
62	AVdd3 (vcxo)	Vdd	Connect to analog power supply	
63	AVdd2 (m)	Vdd	Connect to analog power supply	
64	AVdd2 (m)	Vdd	Connect to analog power supply	

Absolute Maximum Ratings

(Vss = 0 V)

Item	Symbol	Limits		Unit
		Min	Max	
Supply voltage (3.3 V)	V_{DD3}	–0.3	4.6	V
Input voltage	V_I	–0.3	V_{DD3} + 0.3	V
Output voltage	V_O	–0.3	V_{DD3} + 0.3	V
Output current Note1	I_O	—	I_{OL} = 20	mA
			I_{OH} = –26	
Power dissipation	Pd	—	1400	mW
Operating temperature	Topr	–20	75	°C
Storage temperature	Tstg	–50	125	°C

Note: 1. Output current per output terminal. But Pd limits all current.

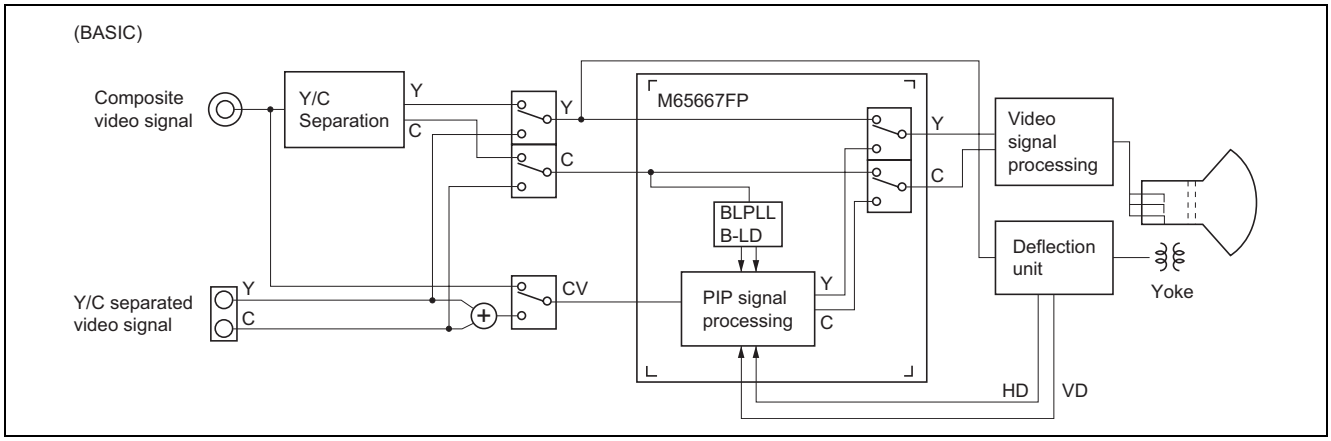


DC Characteristics

(Ta = 25°C, unless otherwise noted, Vss = 0 V)

Item		Symbol	Limits			Unit	Test Conditions
			Min	Typ	Max		
Input voltage (CMOS interface)	L	V_{IL}	0	—	0.81	V	V_{DD} = 2.7 V
	H	V_{IH}	2.52	—	3.6	V	V_{DD} = 3.6 V
Input voltage schmitt trigger (CMOS interface)	–	V_{T-}	0.5	—	1.65	V	V_{DD} = 3.3V
	+	V_{T+}	1.4	—	2.4	V	
	Hysteresis	V_H	0.3	—	1.2	V	
Output voltage	L	V_{OL}	—	—	0.05	V	V_{DD} = 3.3 V, $\|I_O\|$ < 1 µA
	H	V_{OH}	3.25	—	—	V	
Output current	L	I_{OL}	4	—	—	mA	V_{DD} = 3.0 V, V_{OL} = 0.4 V
	H	I_{OH}	—	—	–4	mA	V_{DD} = 3.0 V, V_{OH} = 2.6 V
Input current	L	I_{IL}	–1	—	1	µA	V_{DD} = 3.6 V, V_I = 0 V
	H	I_{IH}	–1	—	1	µA	V_{DD} = 3.6 V, V_I = 3.6 V
Output leakage current	L	I_{OZL}	–1	—	1	µA	V_{DD} = 3.6 V, V_O = 0 V
	H	I_{OZH}	–1	—	1	µA	V_{DD} = 3.6 V, V_O = 3.6 V
Input pin capacitance		C_I	—	7	15	pF	f = 1 MHz, V_{DD} = 0 V
Output pin capacitance		C_O	—	7	15	pF	
Bidirectional pin capacitance		C_{IO}	—	7	15	pF	
Operating current	3.3 V supply	I_{DD}	—	—	140	mA	

PIP TV System Block Diagram



Driving Method and Operating Specification for Serial Interface Data

(1) Serial data transmission completion and start

A low-to-high transition of the DATA (serial data) line while the CLK (serial clock) is high, that completes the serial transmission and makes the bus free.

A high-to-low transition of the DATA line while the CLK is high, that starts the serial transmission and waits for the following CLK and DATA inputs.

(2) Serial data transmission

The data are transmitted in the most significant bit (MSB) first by one-byte unit on the DATA line successively. One-byte data transmission is completed by 9 clock cycles, the former 8 cycles are for address/data and the latter one is for acknowledge detection. (In reading state, ACK is "H" under these two conditions;

1. The coincidence of two address data for the address data transmission.
2. The completion of 8-bit setting data transfer. In writing state, ACK is "H" with the address coincidence and ACK is "L" for detecting acknowledge input from the master (micro processor) after sending 8-bit setting data).

For address/data transmission, DATA must change while CLK is "L". (The data change while CLK is "H" or the simultaneous change of CLK and DATA, that will be a false operation because of undistinguished condition from the completion/start of serial data transfer.)

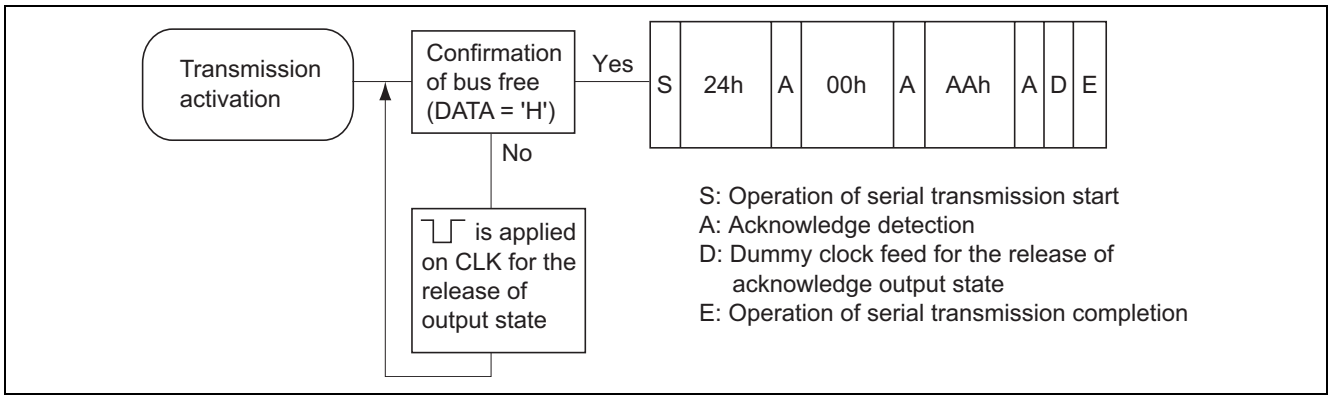
After the beginning of serial data transmission, the total number of data bytes that can be transferred are not limited.

(3) The byte format of data transmission (The sequence of data transmission)

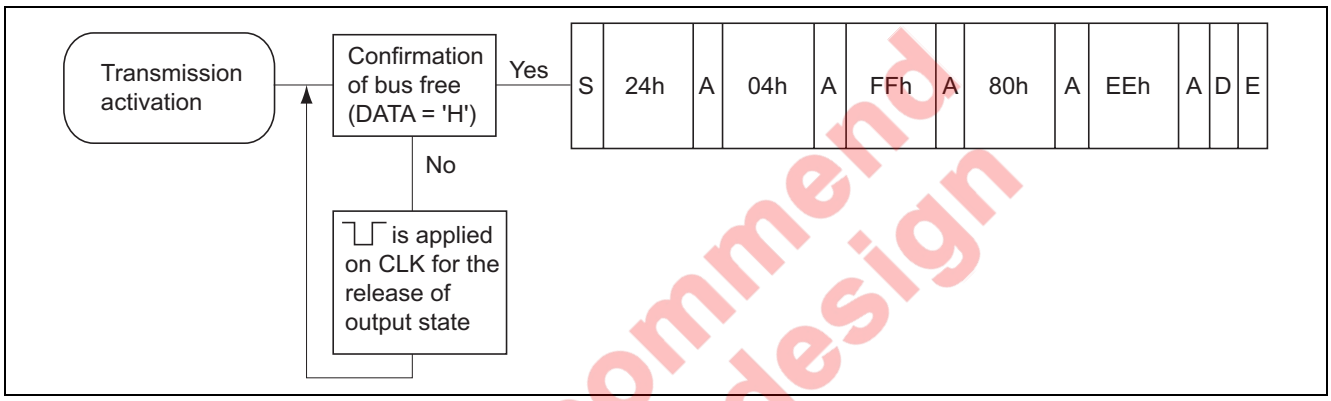
1. The byte format during data setting to M65667FP are shown as follows.
   In right after the forming of serial data transmitting state, the slave address 24h (00100100b) is transferred. Afterwards, the internal register address (1 byte) and setting data (by 1 byte unit) are transferred successively. Several bytes of setting data can be handled in the one transmission. In this operation, the setting data are written into the address resister whose address is increased one in initially transferred internal register address. (The next address of 7Fh, it returns to 00h.)
2. The byte format during data reading from M65667FP are shown as follows.
   Before data reading from M65667FP, whose internal address need to be set by the data reading/transmitting. After the data reading/transmitting, the operation of "serial data transmission completion and start" (described in (1)) is necessary. Continuously, the slave address 25h (00100101b) is sent, and then the inverted read out data are available on ACK. Several bytes of writing data can be handled in the one transmission, too. In this operation, the setting data also are written into the address register whose address is increased one in initially transferred internal register address. (The next address of 7Fh, it returns to 00h.)

The Examples of Serial Byte Transmission Format

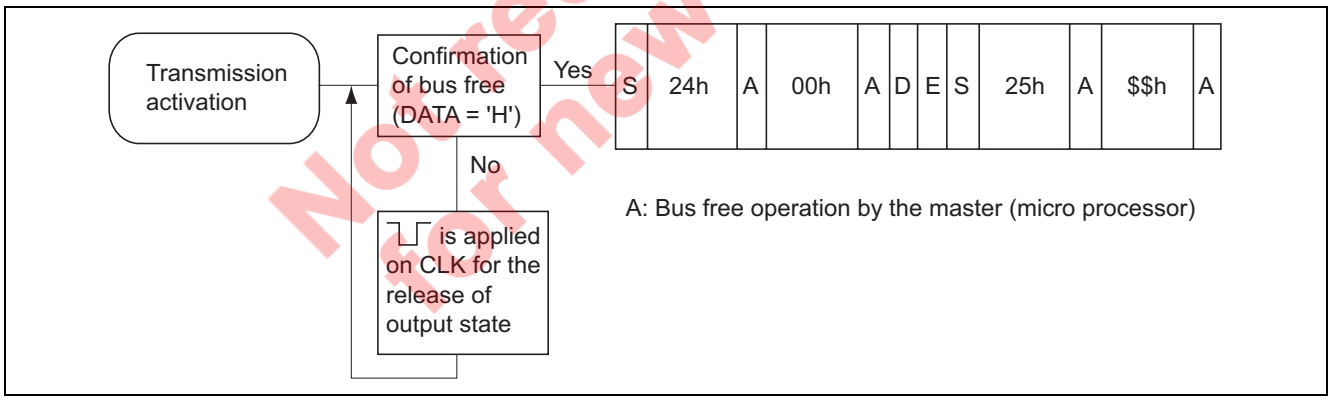
(1) The writing operation of the setting data (AAh) into M65667FP internal address of 00h



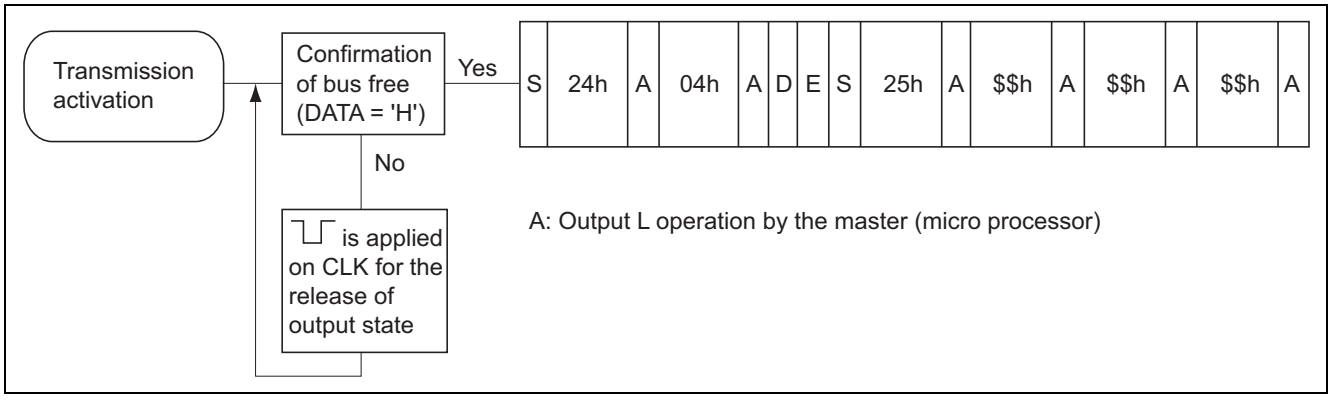
(2) The writing operation of the setting data (FFh, 80h, EEh) into M65667FP internal address of 04h to 06h



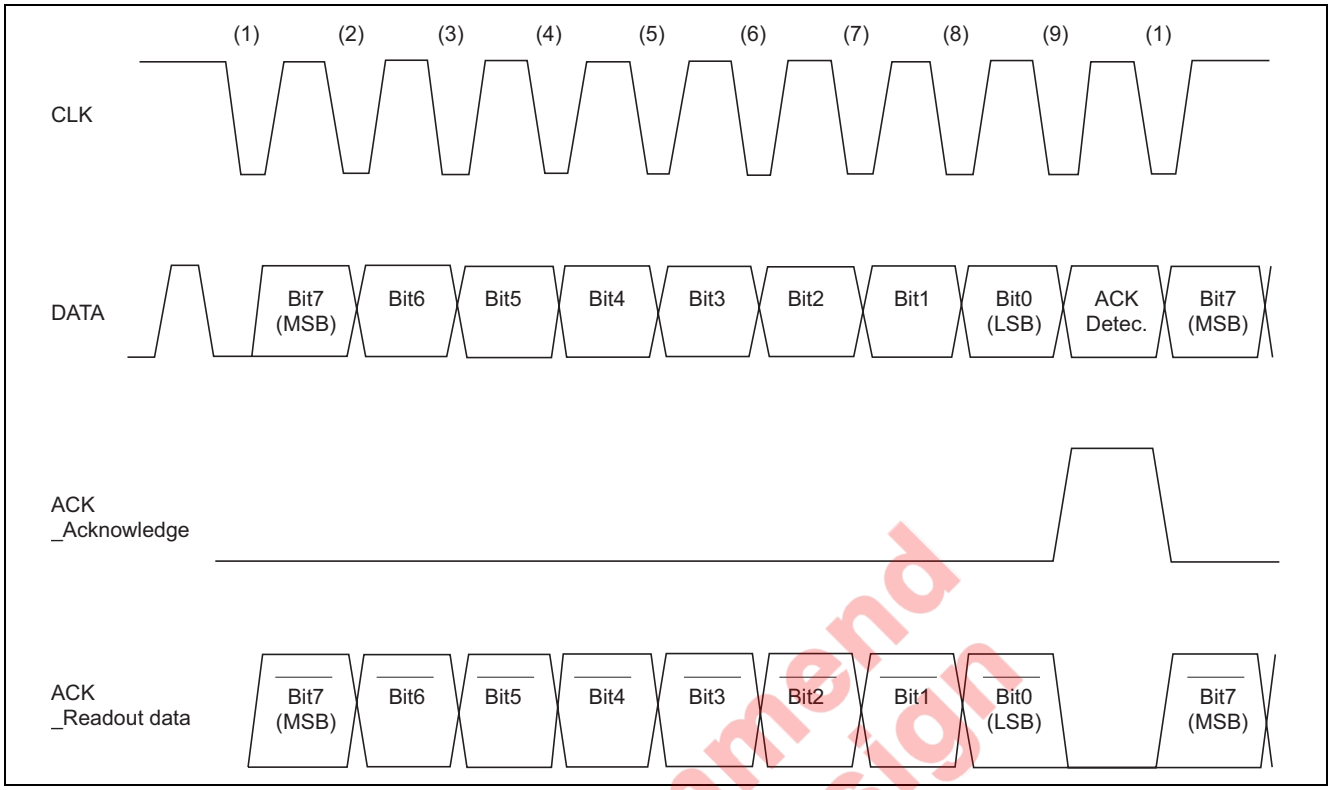
(3) The reading operation of the setting data from M65667FP internal address of 00h



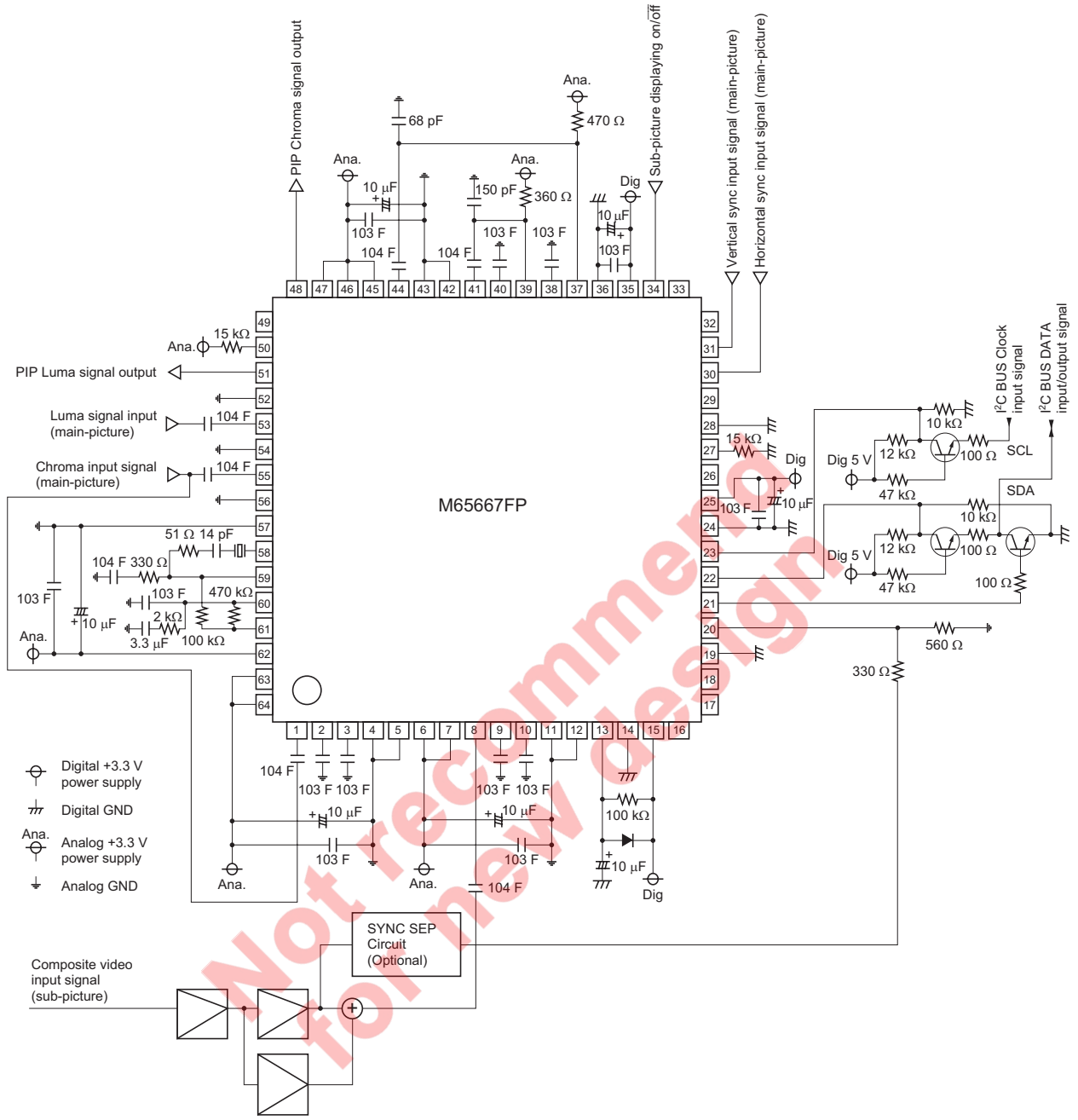
(4) The reading operation of the setting data from M65667FP internal address of 04h to 06h



Timing Diagram



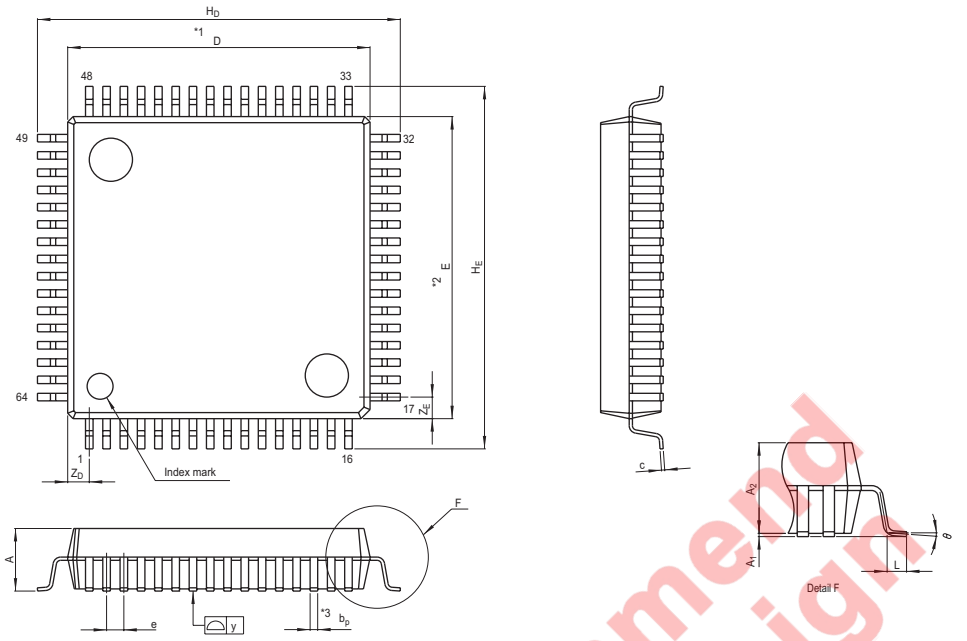
Application Example



Note: Separate Y/C signals by using LC-tank circuit or LPF, BPF for Y/C signals level adjust. And then mix both signals for sub-picture input video signal.

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP64-14x14-0.80	PRQP0064GA-A	64P6N-A	1.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.8	14.0	14.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	16.5	16.8	17.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.3	0.35	0.45
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.65	0.8	0.95
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.4	0.6	0.8

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Colophon .7.2