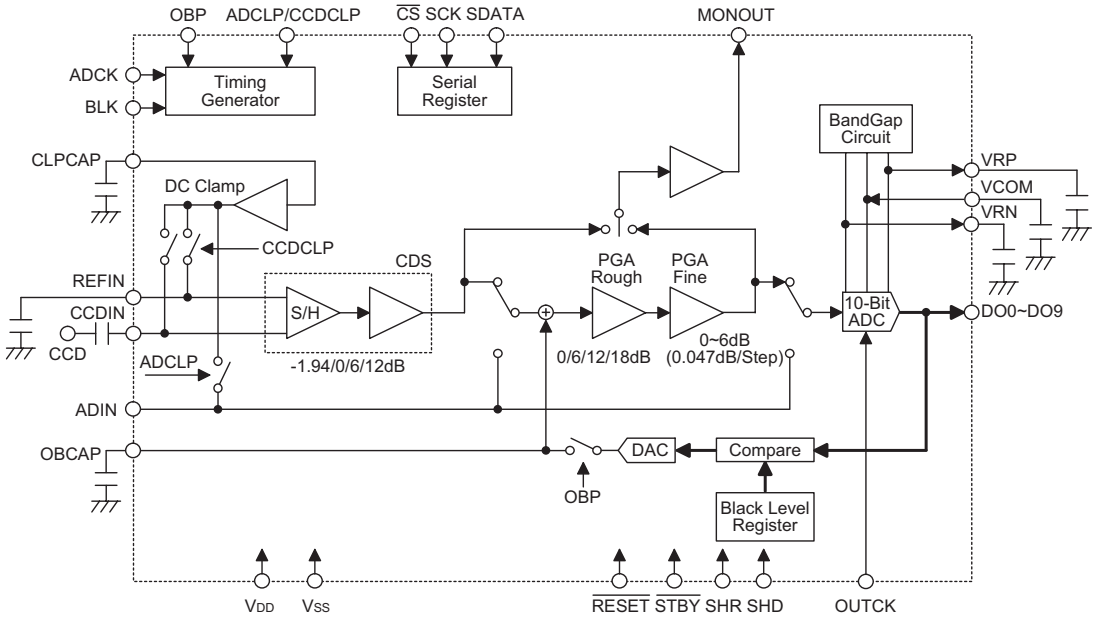
Features

- Operating voltage: 2.7V~3.6V
- Low power consumption: 70mW (Typ.)
- Power down mode: less than 30μW
- Accepts a direct signal input to ADC or PGA at 1.0 V_{PP} (Typ.)
- CCD signal input level: 1.1 V_{P-P} (Max.)
- 10-bit ADC (up to 20MHz)
  - DNL: ±0.6 LSB (Typ.)
- Black level neutralizer, target setting: 16~127LSB
- Built-in serial interface
- Independent ADC input conversion clock and data output clock
- Independent CDS and PGA gain control
  - CDS: −1.94/0/6/12dB
  - PGA: 0~24dB
- Wide gain range: −1.94~36dB
- High speed sample and hold circuit: pulse width 11ns (Min.)
- 48-pin LQFP package

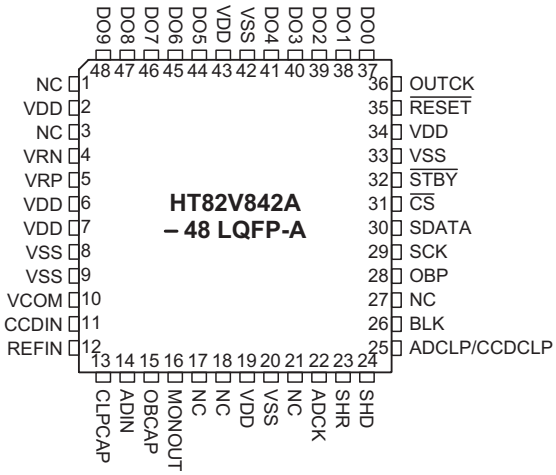
General Description

The HT82V842A is a CMOS single-chip signal processing device for CCD area sensors. It consists of a clamp circuit, Correlated Double Sampler (CDS), Programmable Gain Amplifier (PGA), reference voltage generator, black level detection circuit, 20MHz 10-bit A/D converter (ADC), timing generator for internally required pulses, serial interface for internal function control and PGA gain control.

Block Diagram



Pin Assignment



Pin Description

Pin No.	Pin Name	I/O	Description
1, 3, 17~18, 21	NC	—	No connection
2, 6~7, 19, 34, 43	VDD	—	Positive power supply for analog circuit
4	VRN	O	Negative reference voltage for internal ADC Connect to V_{SS} via 0.1μF
5	VRP	O	Positive reference voltage for internal ADC Connect to V_{SS} via 0.1μF
8~9, 20, 33, 42	VSS	—	Negative power supply for analog circuit
10	VCOM	O	Common reference voltage for internal ADC
11	CCDIN	I	CDS circuit data input
12	REFIN	I	CDS circuit reference input
13	CLPCAP	O	Clamp level output Connect to V_{SS} via 0.1μF
14	ADIN	I	ADIN signal input
15	OBCAP	O	Black level integration voltage Connect to V_{SS} via 0.1μF~1μF (by applications)
16	MONOUT	O	Monitor output of CDS or PGA
22	ADCK	I	ADC sampling clock input
23	SHR	I	Reference sampling pulse input
24	SHD	I	Data sampling pulse input
25	ADCLP/CCDCLP	I	Pulse input for ADIN clamp and black calibration control. Clamp control input.
26	BLK	I	Blanking pulse input
27	NC	—	No connection
28	OBP	I	Black level period pulse input
29	SCK	I	Serial clock input
30	SDATA	I	Serial data input

Pin No.	Pin Name	I/O	Description
31	$\overline{CS}$	I	Serial port chip selection (Active at low)
32	$\overline{STBY}$	I	Power down control (Active low)
35	$\overline{RESET}$	I	Reset signal (Active low)
36	OUTCK	I	Clock source for ADC output
37~41, 44~48	DO0~DO9	O	Digital output from ADC

Absolute Maximum Ratings

Supply Voltage .....GND–0.3V to GND+6V

Input Voltage .....V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature .....–55°C to 150°C

Operating Temperature .....–20°C to 70°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IH}	High Level Input Voltage	3V	—	$0.7V_{DD}$	—	V_{DD}	V
V_{IL}	Low Level Input Voltage	3V	—	0	—	$0.3V_{DD}$	V
I_{IH}	High Level Input Current	3V	V_{IL}=0V	—	—	200	μA
I_{IL}	Low Level Input Current	3V	V_{IH}=3.0V	—	—	1	μA
I_{MD}	Operation Current at Monitor Disable	3V	f_S=20MHz	—	23	—	mA
I_{MA}	Supply Current at Monitor Active	3V	f_S=20MHz	—	26	—	mA
I_{SS}	Power Down Current	3V	—	—	—	10	μA
V_{CCDIN}	Analog Input Range	3V	CCDIN input, f_{IN}=1MHz	—	1.1	—	V_{P-P}
V_{ADIN}		3V	ADIN input, f_{IN}=1MHz	—	1.0	—	V_{P-P}
V_{CLPCAP}	Clamp Voltage	3V	—	1.5	1.7	1.9	V
t_{BLKCAL}	Black Calibration Time	3V	—	—	—	200	Pixel
V_{BLKCAL}	Maximum Calibration Offset Voltage	3V	—	—	±200	—	mV
G (0)	CDS Gain (Set 0 dB)	3V	Absolute gain	–2	–1	0	dB
G (1)	CDS Gain (Set 6.02 dB)	3V	Relative gain	5.52	6.02	6.52	dB
G (2)	CDS Gain (Set 12.04 dB)	3V		11.54	12.04	12.04	dB
G (3)	CDS Gain (Set –1.94 dB)	3V		–2.44	–1.94	–1.44	dB
Gmin	PGA Gain (Minimum Gain)	3V	Absolute gain	–1.2	–0.2	0.8	dB
Gmax	PGA Gain (Maximum Gain)	3V	Relative gain	22.906	23.906	24.906	dB
Gstep	PGA Gain (Gain Step)	3V		0	0.047	0.094	dB
ER_{PA}	Total (CDS+PGA) Gain Monotony	3V	—	—	—	±4	LSB
RES	Resolution	3V	—	—	—	10	Bits

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
DNL	Differential Nonlinearity	3V	f_S=20MHz	—	±0.6	±1.0	LSB
SN	S/N	3V	—	—	58	—	dB
SND	S/(N+D)	3V	—	—	56	—	dB
V_{COM}	ADC Common Voltage	3V	—	1.25	1.4	1.55	V
V_{RP}	V_{RP} Voltage (Positive)	3V	—	1.55	1.65	1.75	V
V_{RN}	V_{RN} Voltage (Negative)	3V	—	1.05	1.15	1.25	V
C_{CAL}	ADC Output Black Level Calibration Code	3V	—	16	—	127	LSB
				1	—	127	LSB
ST_{CAL}	Calibration Code Resolution	3V	—	—	1	—	LSB

Note: Black calibration period is specified when C_{CAL} is from 16 to 127LSB. Although black level codes of 1 to 15 could be set, t_{BLKCAL} is not guaranteed for these codes.

A.C. Characteristics

V_{SS}=0V, Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_S	Conversion Frequency	3.0V	—	0.5	—	20	MHz
t_{CYC}	Clock Cycle Time	3.0V	—	50	—	—	ns
t_R	Clock Rising Time	3.0V	—	—	—	2	ns
t_F	Clock Falling Time	3.0V	—	—	—	2	ns
t_L	Clock Low Period	3.0V	—	23	—	—	ns
t_H	Clock High Period	3.0V	—	23	—	—	ns
t_{WR}	SHR Pulse Width	3.0V	—	11	—	—	ns
t_{WD}	SHD Pulse Width	3.0V	—	11	—	—	ns
t_{DR}	SHR Sampling Aperture	3.0V	—	—	—	4	ns
t_{DD}	SHD Sampling Aperture	3.0V	—	—	—	4	ns
t_{PSUP}	Data Pulse Setup	3.0V	—	2	—	—	ns
t_{HOLD}	Data Pulse Hold	3.0V	—	5	—	—	ns
t_{SP}	Sampling Pulse Non-overlay	3.0V	—	1	—	—	ns
t_{SUPE}	Enable Pulse Setup	3.0V	—	10	—	—	ns
t_{HOLDE}	Enable Pulse Hold	3.0V	—	10	—	—	ns
t_{SUPOC}	OUTCK Setup	3.0V	—	0	—	—	ns
t_{HOLDOC}	OUTCK Hold	3.0V	—	10	—	—	ns
t_{DLD}	3-state Disable Delay	3.0V	Active → High-Z	—	20	—	ns
t_{DLE}	3-state Disable Delay	3.0V	High-Z→ Active	—	20	—	ns
t_{OL}	ADC Output Data Delay	3.0V	—	—	18	—	ns

Functional Description

CDS (Correlated Double Sampling) Circuit

Connect the CCDIN pin to the CCD sensor thru a capacitor. Connect also the REFIN pin to V_{SS} thru a capacitor. The CDS circuit holds the pre-charge voltage of the CCD at SHR pulse and do sampling of the CCD pixel data at SHD pulse. Correlated noise is removed by subtracting the pre-charge voltage from the pixel data level. CDS could choose a gain setting from 0, 6.02, 12 or −1.94dB (Mode 3, register D4 and D5 bits). A CDS gain is controlled by PGA gain. It is recommended to increase the CDS gain then increase the PGA gain to reduce the noise level.

Clamp Circuits

- DC clamp

  The DC level of the CCDIN/REFIN input is fixed by an internal DC clamp circuit. The DC level of the C-coupled CCD signal at the CDS input is set to CLPCAP by the internal DC clamp circuit. The clamp switches are usually turned on at the black level calibration period. The CLPCAP pin connects to V_{SS} thru a 0.1μF capacitor.

- ADIN signal clamp

  Clamp operation can also be used for the ADIN path. The clamp voltage is different from the CCDIN/REFIN signal and it could be turned off by register setting. At ″ADIN signal to ADC″ mode, the ADCLP signal controls the ″clamp circuit″. Black level calibration circuit is also controlled by ADCLP at ″ADIN signal to PGA″ mode.

- Clamp control
  - Clamp current (Mode 2 register D7). Charge current can select normal or fast clamp.
  - Clamp target (Mode 2 register D5 and D4), input signals (REFIN and CCDIN) to be clamped are selectable. The clamp function can be turned off.

Black Level Cancel Circuit

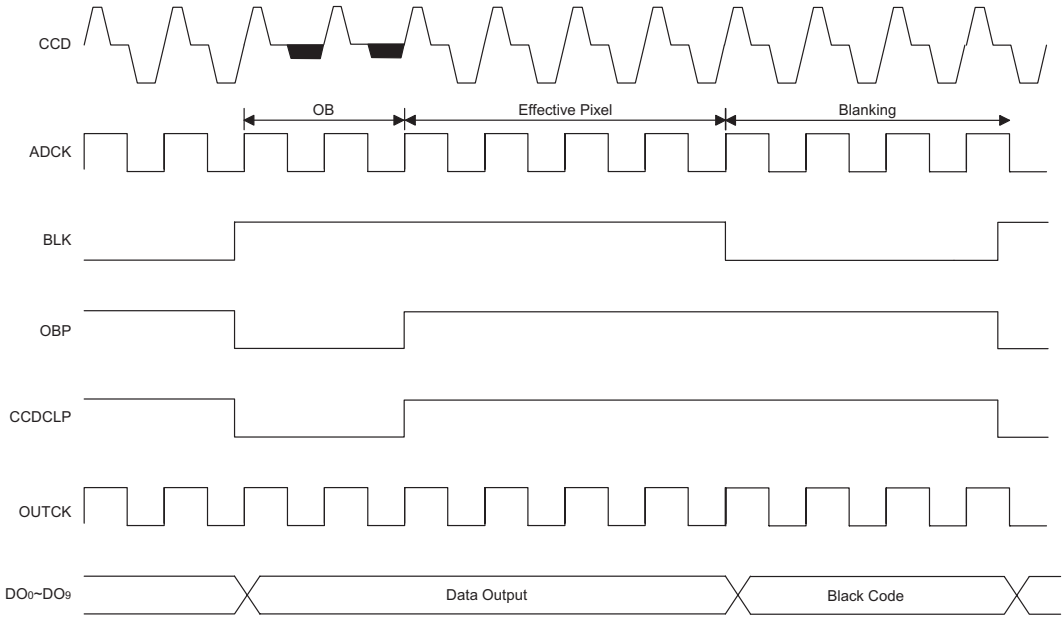
The purpose of a black level cancel circuit is to control the DC level of the PGA input. The ADC output code at an optical black period may correspond to the black level code set up by the register. A black level code of (1 to) 16 to 127 LSB is available (the default is 64 LSB).

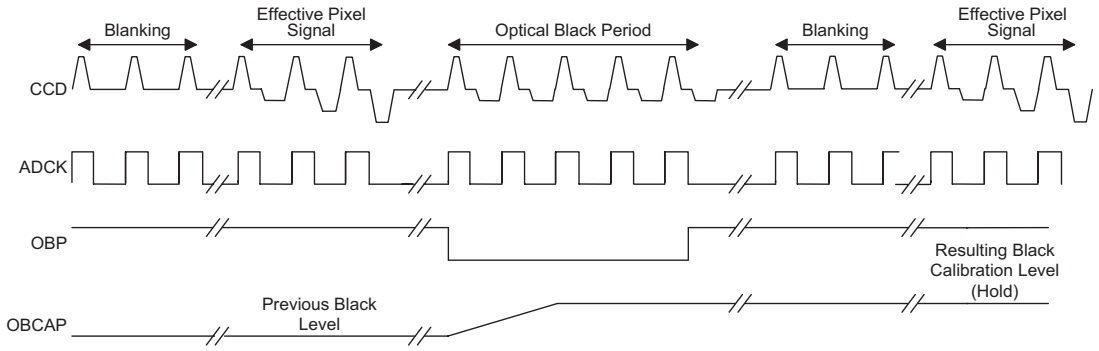
While the OBP pin is active a black level cancel loop is established. In the loop, a comparison is made between the ADC output code and the black level code, the result controls the voltage of the OBCAP capacitor. Hence, the OBCAP voltage settles gradually and the signal level of the optical black period corresponds to the established value.

The following conditions will reset the OBCAP capacitor:

- Set the black level reset register to ″1″ (Mode 1 register D1=1).
- Set the $\overline{\text{RESET}}$ pin to low
- Power down by $\overline{\text{STBY}}$ pin or register control

The DC clamping (CCDCLP) is allowed while the OBP pin is low. The black level cancellation is available at ″ADIN signal to PGA″ mode. The black level cancellation is available at the ADCLP period in this mode. The clamping function and black level canceling function are done simultaneously.





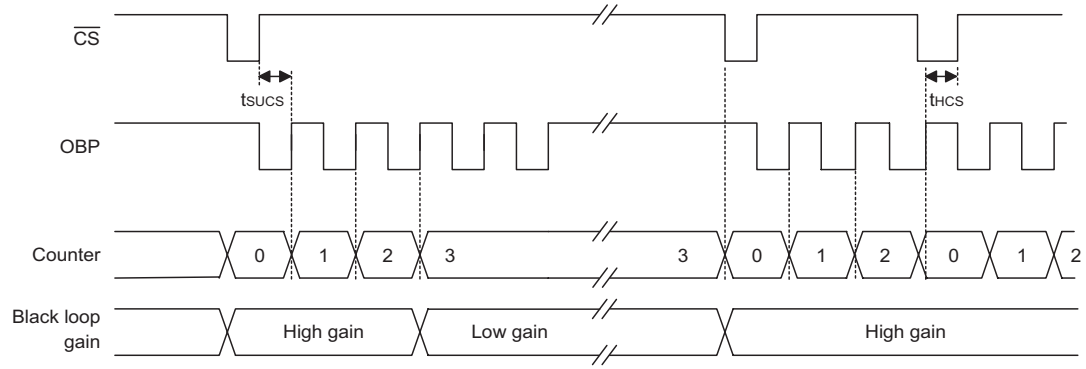
Black Level Calibration Timing

High-speed Black Level Cancellation

The HT82V842A has a high speed black level cancellation function, which by means of a register setting enhances the settling speed within a fixed period from access to the serial interface. It increases the gain of the setting DAC within a fixed period and in turn increases the charge/discharge current to the OBCAP capacitor.

The Mode 3 register D3 to D0 data controls the black level boost function. The default setting is always low gain (D3~D0=5′b0). By setting the register D2~D0, the gain becomes high by 1 to 7 times that of the OBP pulse period after any access to the serial interface. After that period, the gain returns to low. When setting D3 to 1′b1, the gain is always high. The $\overline{CS}$ signal becomes the starting point of the OBP pulse count.

The following figure shows the black loop settling gain boost timing chart when the boost control is on (D3=″0″) and the boost period is set to 3.



Black Loop Settling Gain Boost Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{SUCS}	$\overline{CS}$ Setup Time	—	10	—	—	ns
t_{HCS}	$\overline{CS}$ Hold Time	—	10	—	—	ns

Gain Control Circuit

The total gain for a CCD input signal covers from −1.94dB to 36dB. The CDS range is 0/6/12/-1.94 dB. The PGA rough is 0/6/12/18dB and ADC fine is 0 to 6dB, 0.047dB/step. The CDS gain is controlled by a 2-bit register and the PGA gain is controlled by a 9-bit register.

A/D Converter Circuit

The HT82V842A includes one 20MHz 10 bits AD converter. The ADC converts the following signals.

- The signal from the CCDIN input through a CDS and PGA.
- The signal from the ADIN input through an PGA at the ADIN mode.
- The signal from the ADIN input at the ADIN mode.

A/D Conversion Range

The analog input range of the ADC is determined by the internal reference voltage. The full scale of the ADC is 1.0 V_{PP}.

A/D Converter Output Code (Mode 1 Register D5=1)

The format of an ADC digital output is a straight binary. When in the input zero reference voltage, the output code will be all zero and when the input is a full scale voltage, the output code will be all one.

Clock, Pipeline Delay, Digital Data Output Timing

The ADCK input is used for an A/D conversion. The ADC input signal is sampled at the falling edge of the ADCK input and 10 bits parallel data is output at the rising edge of the ADCK input after a 5.5 clock of pipeline delay.

High-Z Control of ADC Digital Output

ADC digital outputs become High-Z under the following conditions:

- Set the ADC output bit to one. (Mode 1 register D2=1)
- Set the $\overline{\text{STBY}}$ pin to low
- Set the power control bit to one (Mode 1 register D0=1)

A/D Input	Digital Output Code									
	MSB									LSB
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale	1	1	1	1	1	1	1	1	1	1
:	:	:	:	:	:	:	:	:	:	:
:	1	0	0	0	0	0	0	0	0	0
:	0	1	1	1	1	1	1	1	1	1
:	:	:	:	:	:	:	:	:	:	:
Zero Scale	0	0	0	0	0	0	0	0	0	0

ADC Data Output (Coding: Straight Binary)

Miscellaneous Function
(ADC Direct Input, ADIN Mode)

The direct input path to the ADC or the PGA is achieved by means of a register setting. The selectable paths are as follows:

- Function disable (default, Mode 1 register D5=0, D4=0)
- ADIN input to the PGA (Mode 1 register D5=0, D4=1)
- ADIN input to the PGA (Mode 1 register D5=1, D4=Don't care)

The BLK, SHD and SHR inputs are ignored at the ADIN mode.

Power Down Mode

The power down mode can be set either by register setting or by the $\overline{\text{STBY}}$ pin.

Monitor Output

When setting Mode 2 (D1 and D0), the signal from MONOUT is selectable. The alternatives are OFF, CDS output, PGA output or REFIN/CCDIN output. The MONOUT pin gain is fixed to 0dB regardless of the gain control register setting when the CDS output is selected. The MONOUT level becomes V_{COM} at zero reference level. The signals are output in reverse for the CCD input.

Polarity Inversion

The following input polarities can be inverted by register setting:

- ADCK (A/D converter sampling clock, Mode 1 register D6)
- SHR and SHD (CDS sampling clock, Mode 2 register D3 and D2)
- BLK, OBP, CCDCLP and ADCLP (Mode 2 register D3 and D2)

Data Output Clock

The ADCK input or the OUTCK input is selectable as an ADC data output clock.

Serial Interface Circuit

The internal registers of the HT82V842A are controlled by a 3-wire serial interface. The data is a 16-bit length serial data that consists of a 2-bit operation code, 4 bits address and 10 bits data. Each bit is fetched at the rising edge of the $\overline{\text{CS}}$ input. Keep $\overline{\text{CS}}$ to high when not access HT82V842A. It is prohibited to write to a non-defined address. When a data length is below 16 bits, the data is not executed.

Registers

The HT82V842A has 10 bits×7 registers that control the operations. All registers are write only, the serial registers are written by the serial interface.

R/W	Address				Register Name	Function Description
	A3	A2	A1	A0		
W	0	0	0	0	Mode 1	DOUT timing control/OUTCK polarity/ADCK polarity/ADIN connection/ADC output/Black level reset/Power down
W	0	0	0	1	Mode 2	Clamp current/ADIN clamp/Clamp target/S/H, enable logic/Monitor selection
W	0	0	1	0	Mode 3/CDS gain	CDS gain control/Black loop gain boost/Boost period
W	0	0	1	1	PGA gain	PGA gain
W	0	1	0	0	Black level	ADC code at black level (1 LSB step)

Register Map

Register Bit Assignment

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mode 1										
Default	X	0	0	0	0	0	0	0	0	0
Functions										
DOUT timing control		√								
OUTCK polarity			√							
ADCK polarity				√						
ADIN connection					------					
Reserved							√			
ADC output								√		
Black level reset									√	
Power down										√
Mode 2										
Default	X	X	0	0	0	0	0	0	0	0
Functions										
Clamp current			√							
ADIN clamp				√						
Clamp target					------					
S/H, enable logic							------			
Monitor selection									------	
Mode 3										
Default	X	X	X	X	0	0	0	0	0	0
Functions										
CDS gain control					------					
Black loop gain boost							√			
Boost period								----------		
PGA Gain										
Default	X	0	0	0	0	0	0	0	0	0
Functions										
PGA gain		----------								
Black Level										
Default	X	X	X	1	0	0	0	0	0	0
Functions										
Black level				----------						

Register Operations

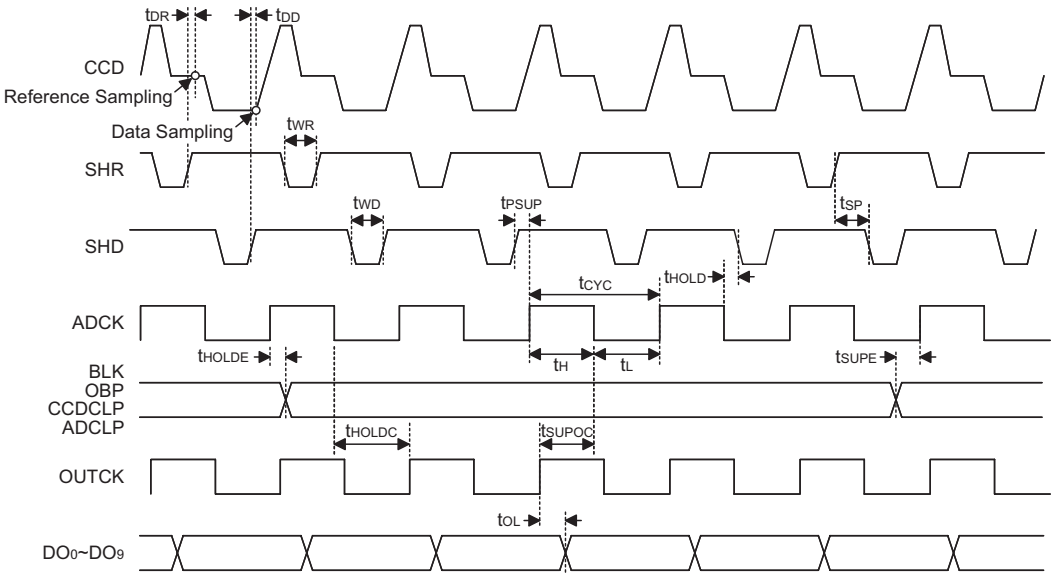
	Control										Operations
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Mode 1											
DOUT timing control		0									DOUT synchronizes to ADCK
		1									DOUT synchronizes to OUTCK
OUTCK polarity			0								DOUT changes at OUTCK rising edge
			1								DOUT changes at OUTCK falling edge
ADCK polarity				0							Normal operation as timing chart
				1							ADCK clock inversion
ADIN connection					0	0					ADIN function OFF
					0	1					ADIN signal to PGA
					1	x					ADIN signal to ADC
Reserved							0				Reserved
							1				Reserved
ADC output								0			Normal operation, ADC data output
								1			ADC output high-Z, or logic of $\overline{\text{STBY}}$
Black level reset									0		Normal operation
									1		Black level reset, or logic of $\overline{\text{RESET}}$
Power down										0	Normal operation
										1	Power down, or logic of $\overline{\text{STBY}}$
Mode 2											
Clamp current			0								Normal clamp ±50μA
			1								Fast clamp ±100μA
ADIN clamp				0							Clamp operation active for ADIN
				1							No clamp for ADIN
Clamp target					0	0					Normal mode, clamp both REFIN and CCDIN
					0	1					Clamp REFIN only
					1	0					Clamp CCDIN only
					1	1					Clamp off
S/H, enable logic							0	0			Normal operation as timing chart
							0	1			S/H control polarity inversion
							1	0			Enable control polarity inversion
							1	1			Both of S/H and enable inversion
Monitor selection									0	0	Monitor off
									0	1	CDS signal to monitor
									1	0	PGA output monitor
									1	1	Output REFIN and CCDIN
Mode 3											
CDS gain control					0	0					CDS gain=odB
					0	1					CDS gain=6.02dB
					1	0					CDS gain=12.04dB
					1	1					CDS gain=−1.94dB
Black loop gain boost							0				Boost control on
							1				Always high gain

	Control										Operations
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Boost period							0	0	0	0	Always low gain
							0	0	0	1	High gain for 1 OBP pulse
							0	0	1	0	High gain for 2 OBP pulse
							0	0	1	1	High gain for 3 OBP pulse
							0	1	0	0	High gain for 4 OBP pulse
							0	1	0	1	High gain for 5 OBP pulse
							0	1	1	0	High gain for 6 OBP pulse
							0	1	1	1	High gain for 7 OBP pulse

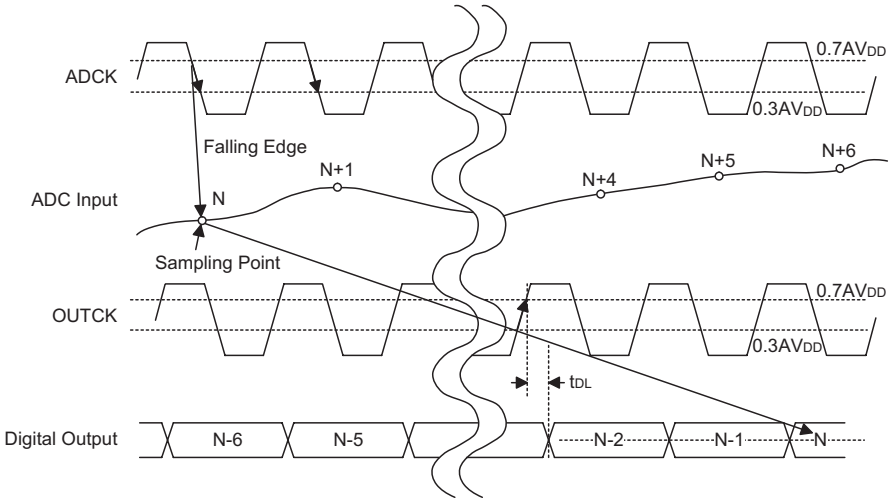
	Control										Decimal	HEX	PGA Gain (dB)
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
PGA gain	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	1	1	1	0.046
	0	0	0	0	0	0	0	0	1	0	2	2	0.093
	0	0	0	0	0	0	0	0	1	1	3	3	0.142
	0	0	0	0	0	0	0	1	0	0	4	4	0.187
	↓										↓	↓	↓
	0	0	0	0	1	1	1	1	1	0	62	3E	2.915
	0	0	0	0	1	1	1	1	1	1	63	3F	2.962
	0	0	0	1	0	0	0	0	0	0	64	40	3.011
	0	0	0	1	0	0	0	0	0	1	65	41	3.056
	↓										↓	↓	↓
	0	0	0	1	1	1	1	1	1	1	127	7F	5.972
	0	0	1	0	0	0	0	0	0	0	128	80	6.021
	0	0	1	0	0	0	0	0	0	1	129	81	6.058
	↓										↓	↓	↓
	0	0	1	1	0	0	0	0	0	0	192	C0	9.031
	↓										↓	↓	↓
	0	0	1	1	1	1	1	1	1	1	255	FF	11.994
	0	1	0	0	0	0	0	0	0	0	256	100	12.041
	0	1	0	0	0	0	0	0	0	1	257	101	12.087
	↓										↓	↓	↓
	0	1	0	1	0	0	0	0	0	0	320	140	15.05
	↓										↓	↓	↓
	0	1	0	1	1	1	1	1	1	1	383	17F	18.14
	0	1	1	0	0	0	0	0	0	0	384	180	18.061
	0	1	1	0	0	0	0	0	0	1	385	181	18.108
	↓										↓	↓	↓
	0	1	1	1	0	0	0	0	0	0	448	1C0	21.071
	↓										↓	↓	↓
	0	1	1	1	1	1	1	1	1	0	510	1FE	23.987
	0	1	1	1	1	1	1	1	1	1	511	1FF	24.032

	Operation, ADC Code										Black Code	
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Decimal	HEX
Black level				0	0	0	0	0	0	0	Forbidden	Forbidden
				0	0	0	0	0	0	1	1	1
							↓				↓	↓
				0	0	0	1	1	1	1	15	F
				0	0	1	0	0	0	0	16	10
				0	0	1	0	0	0	1	17	11
				0	0	1	0	0	1	0	18	12
				0	0	1	0	0	1	1	19	13
							↓				↓	↓
				0	1	0	0	0	0	0	32	20
							↓				↓	↓
				1	0	0	0	0	0	0	64	40
							↓				↓	↓
				1	1	1	1	1	0	0	124	7C
				1	1	1	1	1	0	1	125	7D
				1	1	1	1	1	1	0	126	7E
				1	1	1	1	1	1	1	127	7F

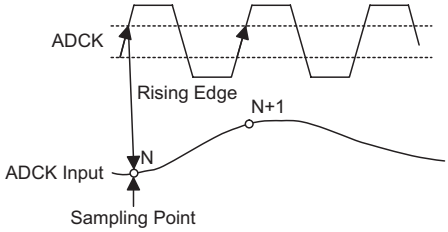
Timing Diagrams



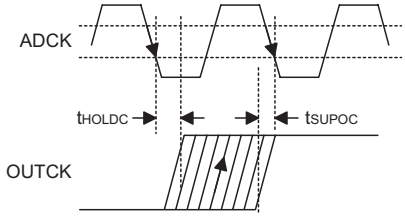
AD Conversion Timing (at ADIN (ADC) Input Mode 1 Register D5=1)



ADC Direct Input Chart



ADCK Inversion Chart



OUTCK Timing Chart

These figures are shown when the Mode 1 D8 bit is set to ″1″, and an external clock is input to the OUTCK pin. When setting D8 bit to ″0″, the ADCK is used as OUTCK.

Note: At default condition in ADIN mode, data are sampled at the falling edge of the ADCK clock, and are output at the rising edge of the OUTCK clock. Set the ADCK polarity register to ″1″ when the data are sampled and are output at the falling edge of the ADCK clock.

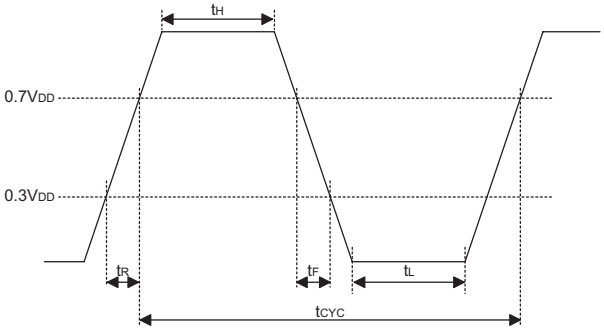
The diagram on the upper portion of this page shows the default timing and the lower left figure shows the inverted timing.

Delay from data sampling to data output
ADCK normal: At Mode 1 register D6=0; 5.5 clk delay
ADCK inversion: At Mode 1 register D6=1; 6.0 clk delay

In ADIN input mode, the above mentioned register setting is available.

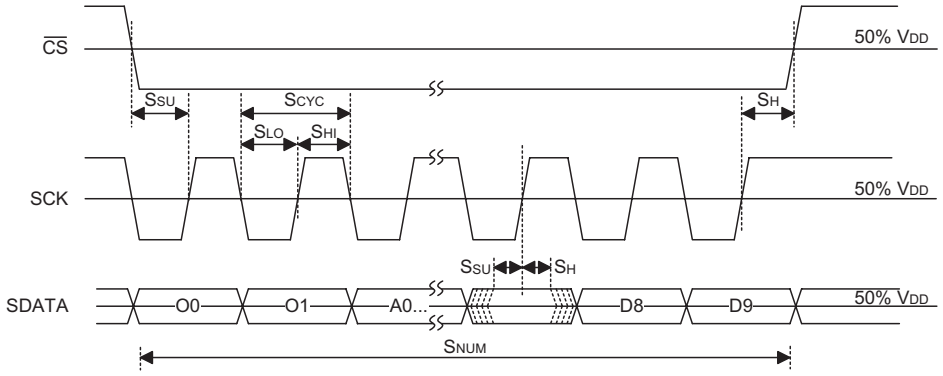
At ADIN (PGA) input Mode 1 register D5=0 and D4=1, digital data output is delayed by 2 clks.

ADCK Clock Waveform



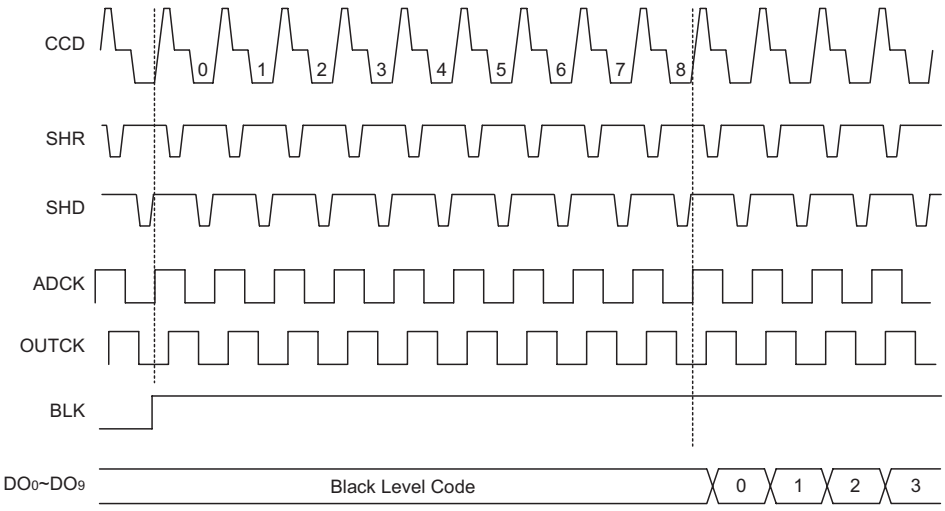
Control Interface Timing V_{SS}=0V, Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
S_{CYC}	SCK Clock Frequency	3.0V	—	—	—	10	MHz
S_{LO}	SCK Clock Low Level Width	3.0V	—	40	—	—	ns
S_{HI}	SCK Clock High Level Width	3.0V	—	40	—	—	ns
S_{SU}	Data Setup Time Period	3.0V	—	20	—	—	ns
S_H	Data hold Time Period	3.0V	—	20	—	—	ns
S_R	SCK, $\overline{CS}$ Rising Time Period	3.0V	30%→70%	—	—	6	ns
S_F	SCK, $\overline{CS}$ Falling Time Period	3.0V	70%→30%	—	—	6	ns
SNUM	Number of Serial Data	3.0V	—	—	16	—	pcs

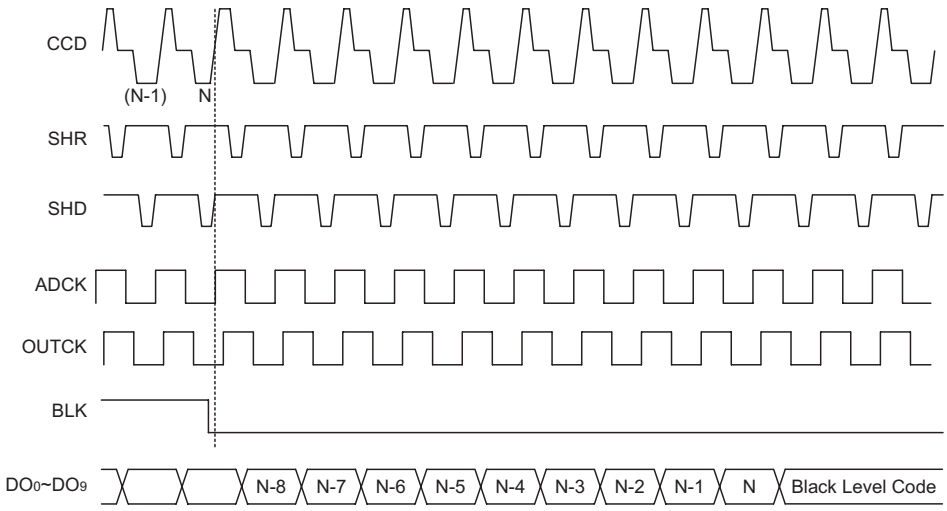


Serial I/F Timing Chart

Data Output Sequence



Pixel Data Readout Sequence (1): Start of Conversion

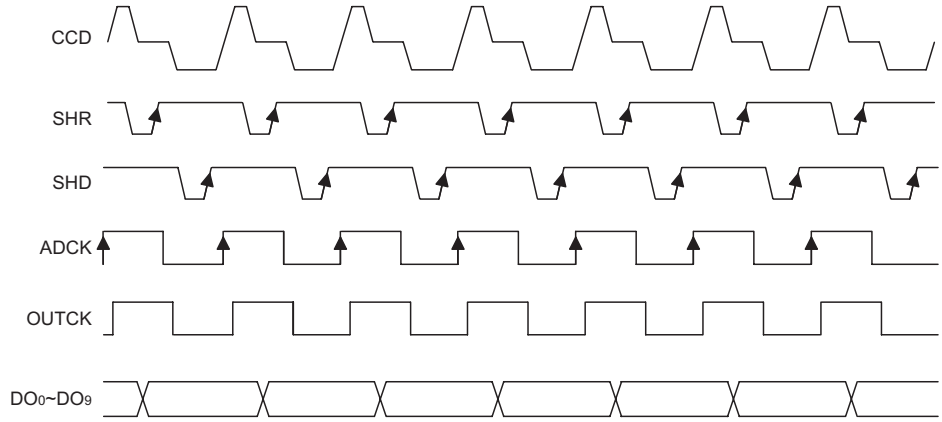


Pixel Data Readout Sequence (2): End of Conversion

Clock Timing Variations by Register Setting

Clock timing variations when it is inverted by register settings.

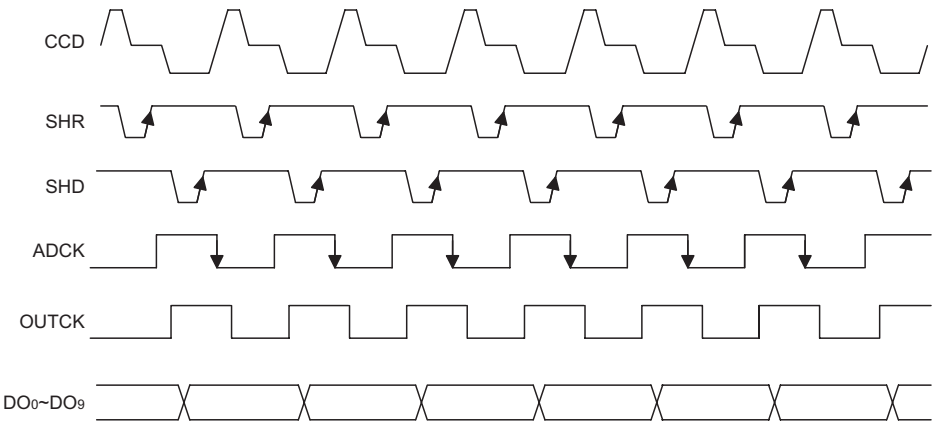
- No inversion
  Mode 1 register D6=0, Mode 2 register D2=0; Default



Pulse Control (Default: No Inversion)

- ADCK inversion

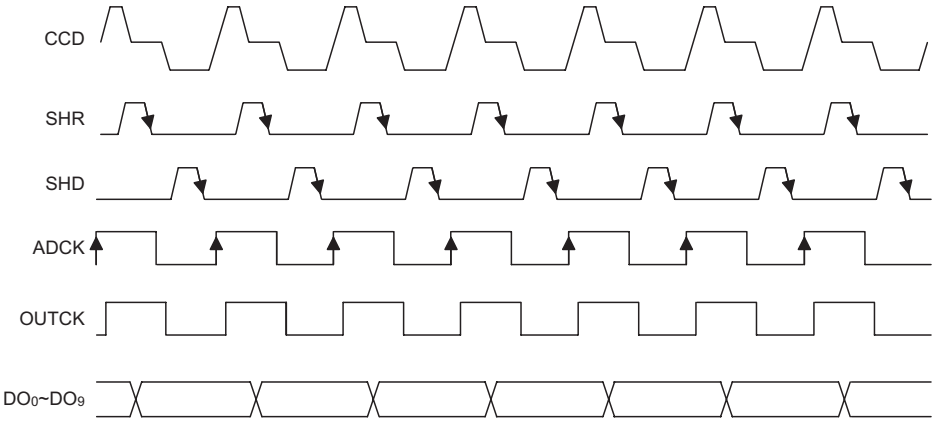
  Mode 1 register D6=1, Mode 2 register D2=0



Pulse Control (ADCK Inversion)

- SHR & SHD inversion

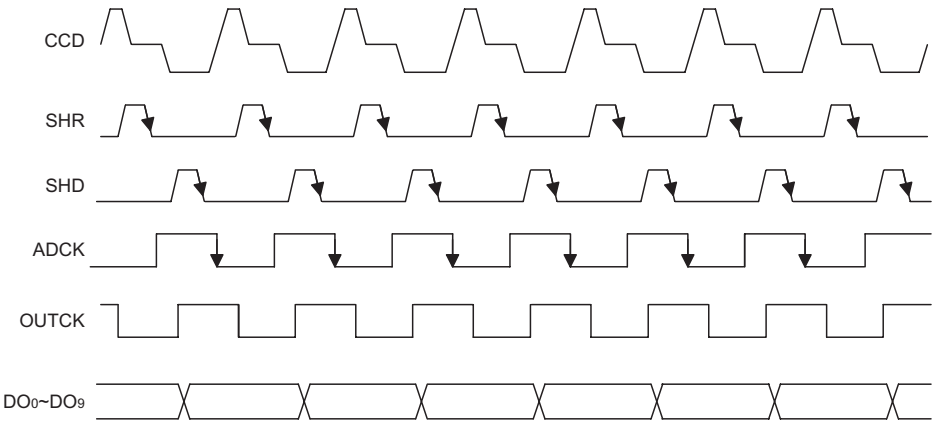
  Mode 1 register D6=0, Mode 2 register D2=1



Pulse Control (SHR & SHD Inversion)

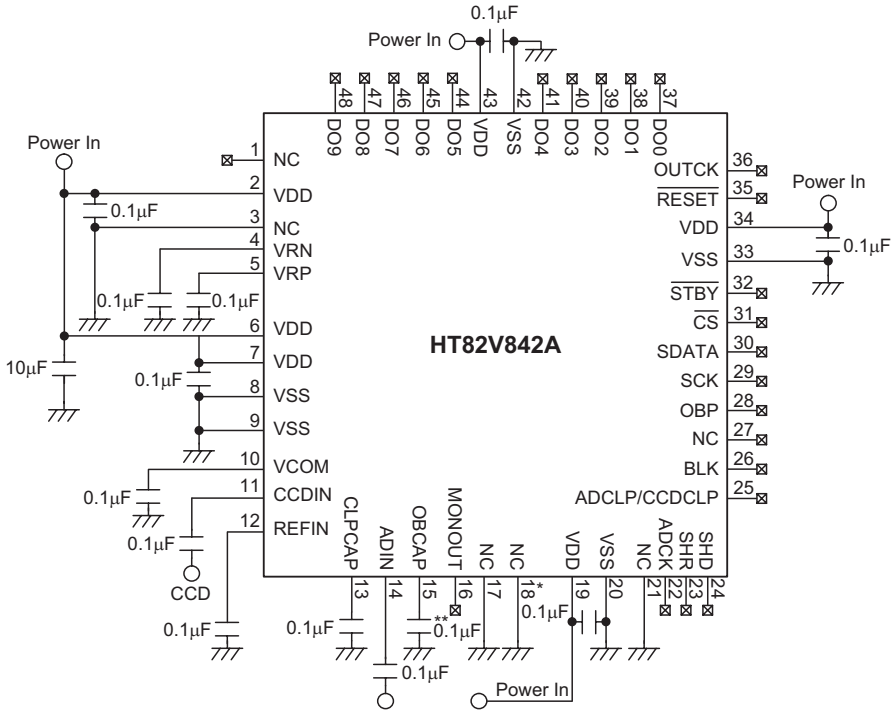
- ADCK, SHR & SHD inversion

  Mode 1 register D6=1, Mode 2 register D2=1



Pulse Control (ADCK, SHR & SHD Inversion)

Application Circuits

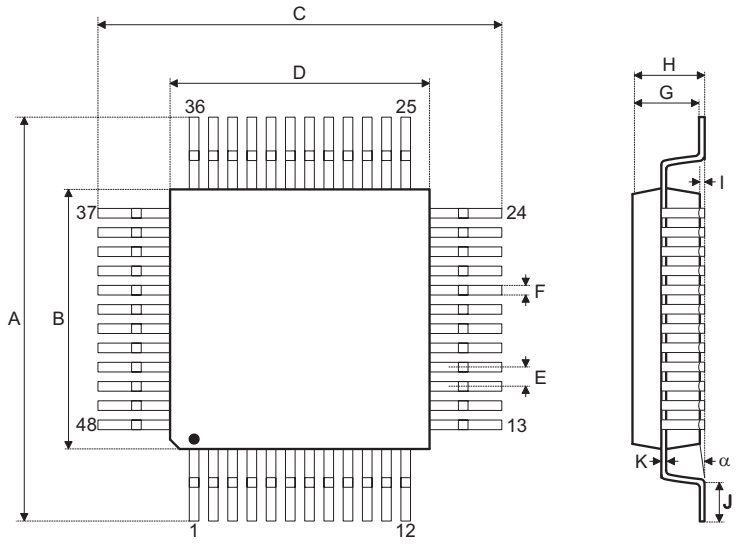


Note: "*" Pin 18 can also connect to ground with a 4.7kΩ resistor.

"**" The capacitor connects to OBCAP pin maybe need adjust by user's applications from 0.1μF~1μF typically.

Package Information

48-pin LQFP (7×7) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

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