1.8 nV/√Hz, 36 V Precision Quad Amplifiers

ADA4004-1/ADA4004-2/ADA4004-4

FEATURES

Very low voltage noise: 1.8 nV/√Hz
Low input bias current: 90 nA maximum
Offset voltage: 125 μV maximum
High gain: 120 dB
Wide bandwidth: 12 MHz
±5 V to ±15 V operation

APPLICATIONS

Precision instrumentation
Filter blocks
Microphone preamplifiers
Industrial control
Thermocouples and RTDs
Reference buffers

GENERAL DESCRIPTION

The ADA4004-1/ADA4004-2/ADA4004-4 are 1.8 nV/√Hz precision quad amplifiers featuring 40 μV offset, 0.7 μV/°C drift, 12 MHz bandwidth, and low 1.7 mA per amplifier supply current.

The ADA4004-1/ADA4004-2/ADA4004-4 are designed on the high performance *i*Polar™ process, enabling improvements such as reduced noise and power consumption, increased speed and stability, and smaller footprint size. Novel design techniques enable the ADA4004-1/ADA4004-2/ADA4004-4 to achieve 1.8 nV/√Hz voltage noise density and a low 6 Hz 1/f noise corner frequency while consuming just 1.7 mA per amplifier. The small package saves board space, reduces cost, and improves layout flexibility.

Applications for these amplifiers include high precision controls, PLL filters, high performance precision filters, medical and analytical instrumentation, precision power supply controls, ATE, and data acquisition systems. Operation is fully specified from ±5 V to ±15 V from −40°C to +125°C.

The ADA4004-1, ADA4004-2, and ADA4004-4 are members of a growing series of low noise op amps offered by Analog Devices, Inc. (see Table 1).

Table 1. Voltage Noise

Pkg.	0.9 nV	1.1 nV	1.8 nV	2.8 nV	3.8 nV
Single	AD797	AD8597	ADA4004-1	AD8675	AD8671
Dual		AD8599	ADA4004-2	AD8676	AD8672
Quad			ADA4004-4		AD8674

PIN CONFIGURATIONS

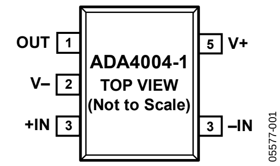

Figure 1. 5-Lead SOT (RJ-5)

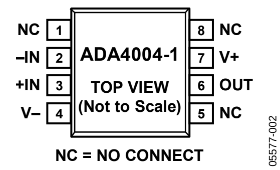

Figure 2. 8-Lead SOIC (R-8)

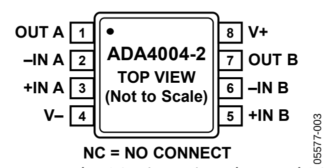

Figure 3. 8-Lead MSOP (RM-8) and 8-Lead SOIC (R-8)

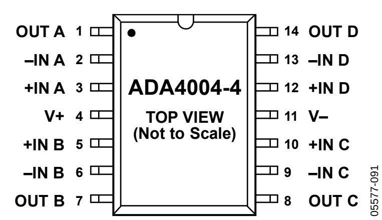

Figure 4. 14-Lead SOIC (R-14)

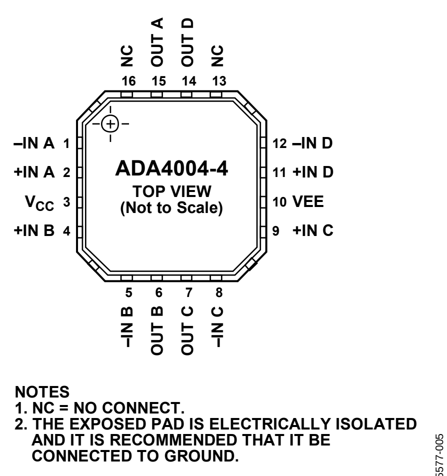

Figure 5. 16-Lead LFCSP (CP-16-4)

Rev. C

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Added Figure 1 to Figure 3; Renumbered Sequentially ... 1
Changes to General Description Section ... 1
Added Table 1; Renumbered Sequentially ... 1
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Added Phase Margin Parameter, Table 2 ... 3
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11/07—Rev. A to Rev. B

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7/06—Rev. 0 to Rev. A

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1/06—Revision 0: Initial Version

SPECIFICATIONS

V_{SY} = ±5 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			40	140	µV
		−40°C ≤ T_A ≤ +125°C			300	µV
Input Bias Current	I_B			40	85	nA
		−40°C ≤ T_A ≤ +125°C			165	nA
Input Offset Current	I_{OS}			40	85	nA
		−40°C ≤ T_A ≤ +125°C			100	nA
Input Voltage Range	IVR		−3.5		+3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −3.0 V to +3.0 V	105	111		dB
		−40°C ≤ T_A ≤ +125°C	95	110		dB
Open-Loop Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = −2.5 V to +2.5 V	250	400		V/mV
		−40°C ≤ T_A ≤ +125°C	170			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.7	1	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to ground	3.7	3.9		V
		−40°C ≤ T_A ≤ +125°C	3.4	3.6		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to ground		−3.6	−3.55	V
		−40°C ≤ T_A ≤ +125°C		−3.6	−3.4	V
Short-Circuit Limit	I_{SC}			25		mA
		−40°C ≤ T_A ≤ +125°C				mA
Output Current	I_O	V_{OUT} = ±3.6 V		±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±5 V to ±15 V	110	118		dB
		−40°C ≤ T_A ≤ +125°C	110			dB
Supply Current per Amplifier	I_{SY}				2.0	mA
		−40°C ≤ T_A ≤ +125°C			2.2	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ to ground		2.7		V/µs
Gain Bandwidth Product	GBP			12		MHz
Phase Margin	Φ_M			48		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	f = 0.1 Hz to 10 Hz		0.1		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		1.8		nV/√Hz
Current Noise Density	i_n	f = 10 Hz		3.5		pA/√Hz
Current Noise Density	i_n	f = 200 Hz		1.2		pA/√Hz

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			40	125	µV
		−40°C ≤ T_A ≤ +125°C			270	µV
Input Bias Current	I_B			40	90	nA
		−40°C ≤ T_A ≤ +125°C			165	nA
Input Offset Current	I_{OS}				60	nA
		−40°C ≤ T_A ≤ +125°C			100	nA
Input Voltage Range	IVR		−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12.5 V to +12.5 V	110	113		dB
		−40°C ≤ T_A ≤ +125°C	100	104		dB
Open-Loop Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = −12.0 V to +12.0 V	500	1200		V/mV
		−40°C ≤ T_A ≤ +125°C	250	500		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.7	1	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to ground	13.4	13.6		V
		−40°C ≤ T_A ≤ +125°C	13.1	13.3		V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to ground		−13.3	−13.2	V
		−40°C ≤ T_A ≤ +125°C		−13.25	−13.15	V
Short-Circuit Limit	I_{SC}			25		mA
Output Current	I_O	V_{OUT} = ±13.6 V		±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±5 V to ±15 V	110	118		dB
		−40°C ≤ T_A ≤ +125°C	110			dB
Supply Current per Amplifier	I_{SY}				2.2	mA
		−40°C ≤ T_A ≤ +125°C			2.4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ to ground		2.7		V/µs
Gain Bandwidth Product	GBP			12		MHz
Phase Margin	Φ_M			48		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\ p\text{-}p}$	f = 0.1 Hz to 10 Hz		0.15		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		1.8		nV/√Hz
Current Noise Density	i_n	f = 10 Hz		3.5		pA/√Hz
Current Noise Density	i_n	f = 200 Hz		1.2		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V or +36 V
Input Voltage	V− < V_{IN} < V+
Differential Input Voltage	±V supply
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

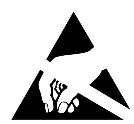
THERMAL RESISTANCE

θ_{JA} is specified with the device soldered on a circuit board with its exposed paddle soldered to a pad (if applicable) on a 4-layer JEDEC standard printed circuit board with zero airflow.

Table 5.

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SOT (RJ-5)	230	92	°C/W
8-Lead SOIC (R-8), ADA4004-1	177	53	°C/W
8-Lead SOIC (R-8), ADA4004-2	155	45	°C/W
8-Lead MSOP (RM-8)	186	52	°C/W
14-Lead SOIC_N (R-14)	115	36	°C/W
16-Lead LFCSP_VQ (CP-16-4)	44	31.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

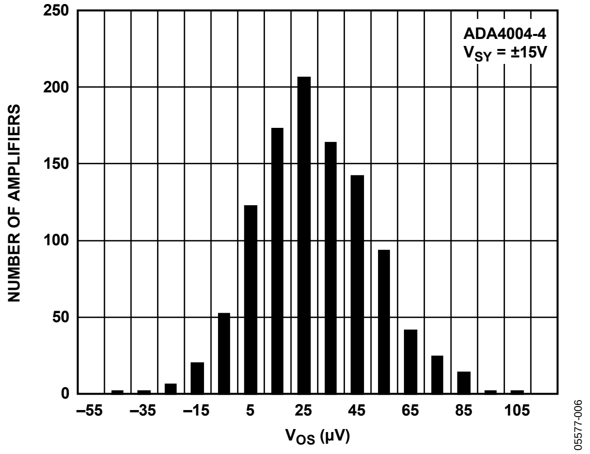


Figure 6. Number of Amplifiers vs. Input Offset Voltage

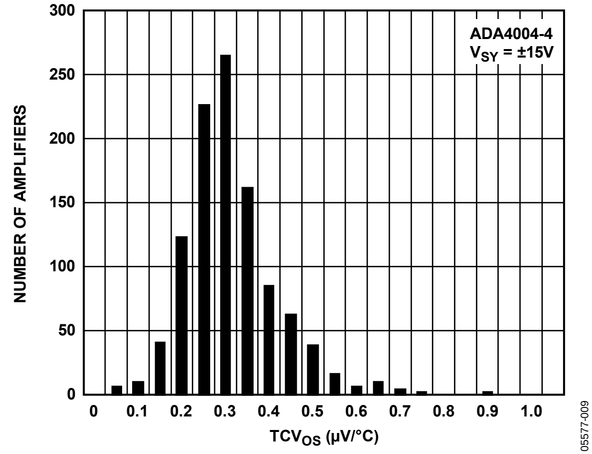


Figure 9. Number of Amplifiers vs. TCV_{OS}

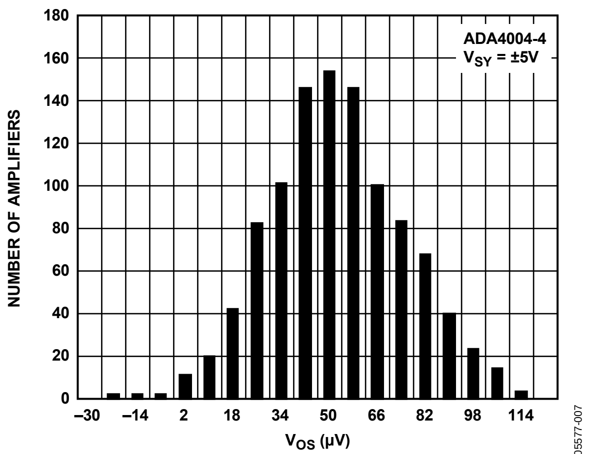


Figure 7. Number of Amplifiers vs. Input Offset Voltage

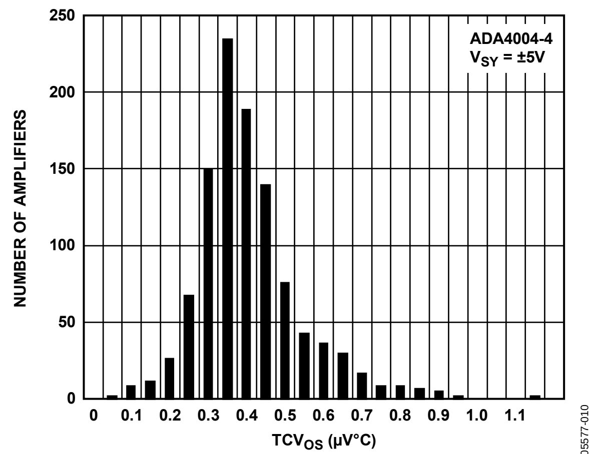


Figure 10. Number of Amplifiers vs. TCV_{OS}

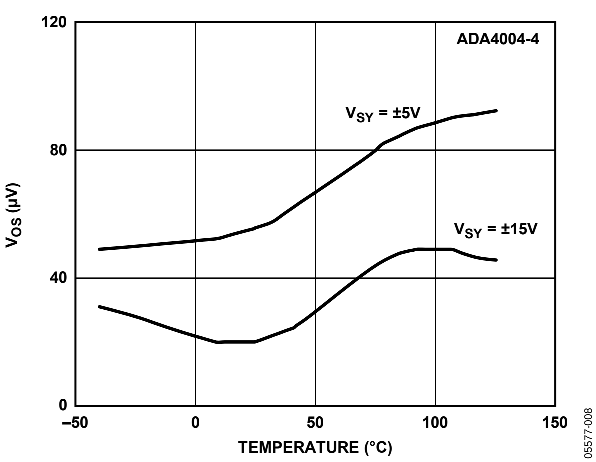


Figure 8. Input Offset Voltage vs. Temperature

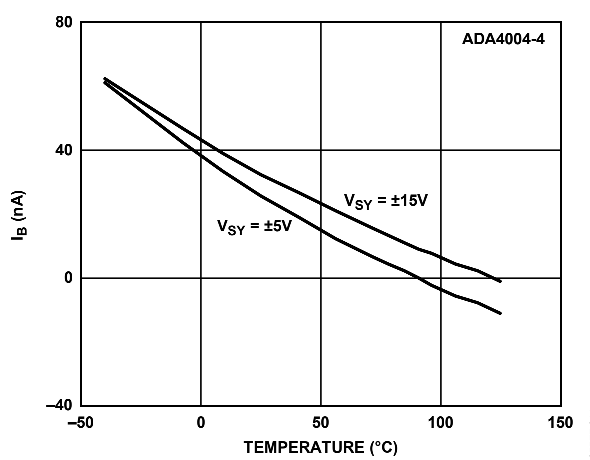


Figure 11. Input Bias Current vs. Temperature

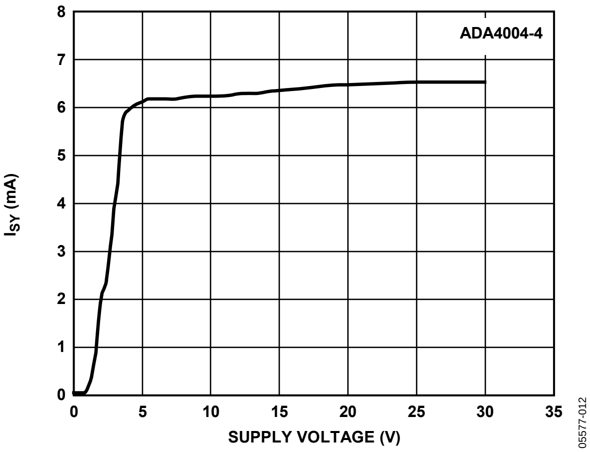


Figure 12. Supply Current vs. Total Supply Voltage

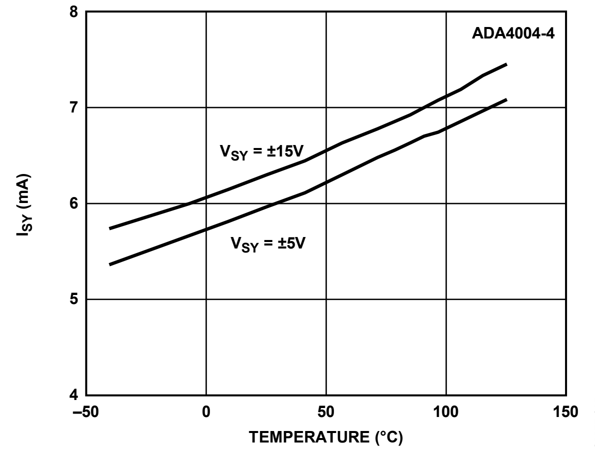


Figure 15. Supply Current vs. Temperature

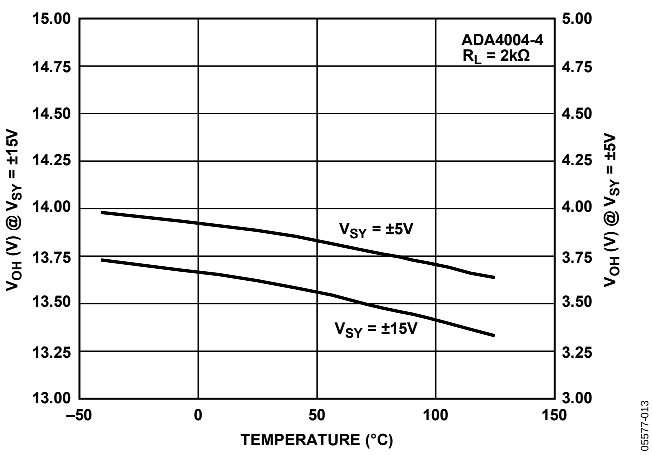
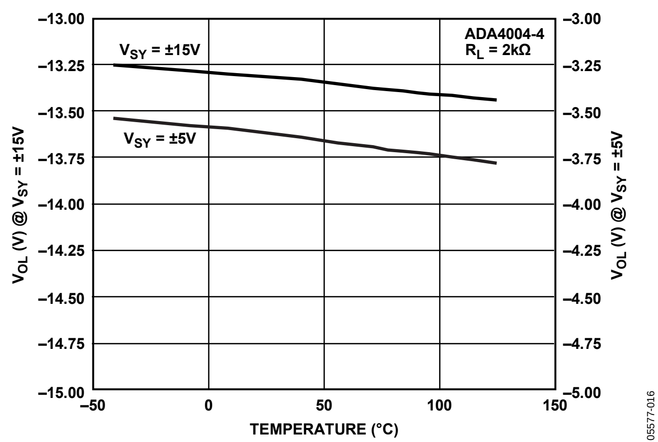


Figure 13. V_{OH} vs. Temperature



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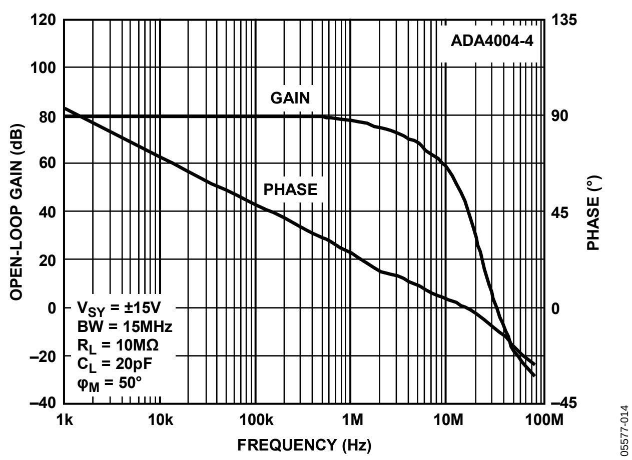
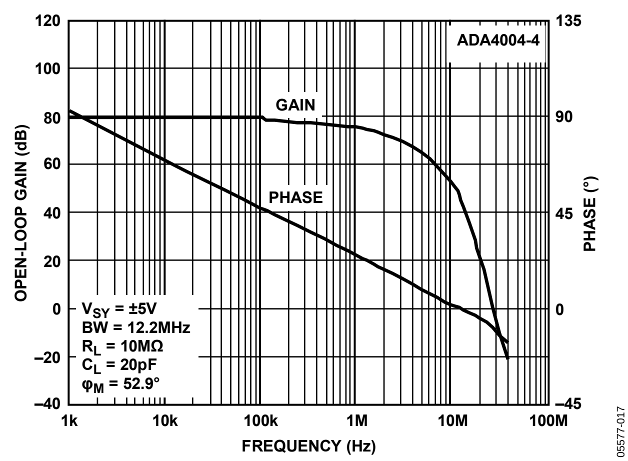


Figure 14. Open-Loop Gain and Phase vs. Frequency



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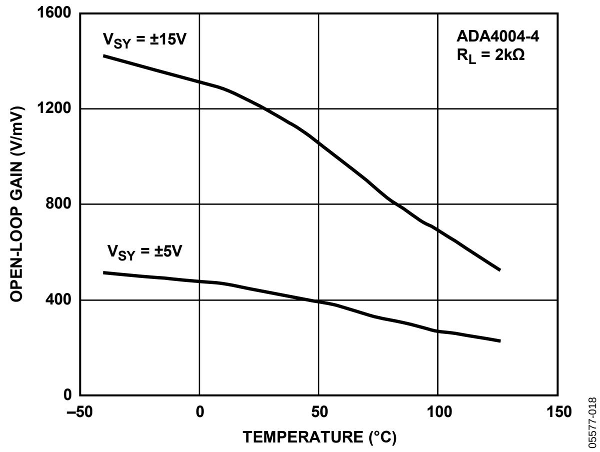


Figure 18. Open-Loop Gain vs. Temperature

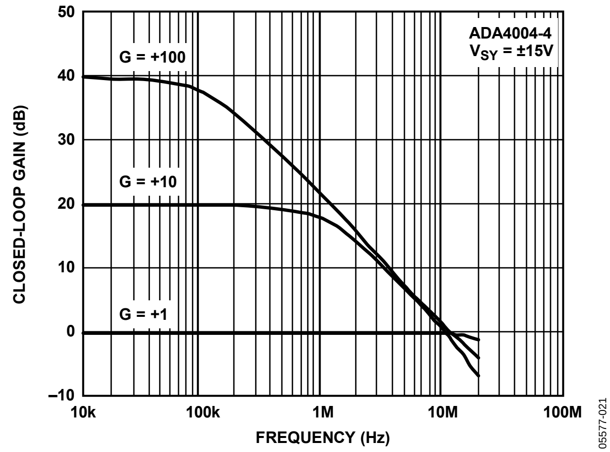
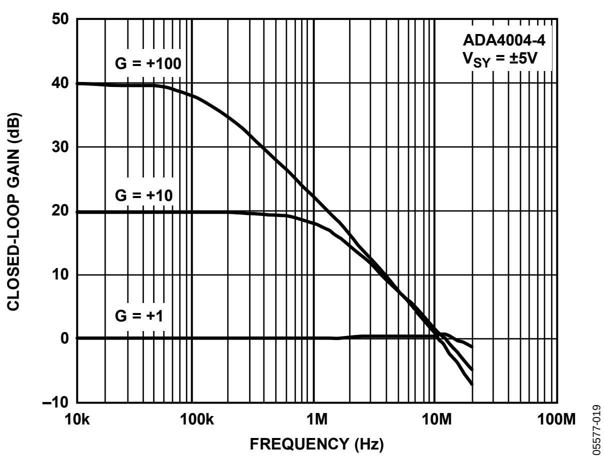


Figure 21. Closed-Loop Gain vs. Frequency



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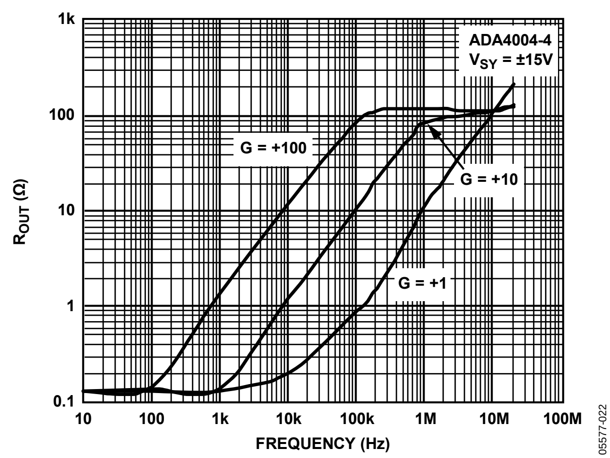

Figure 22. Output Impedance vs. Frequency

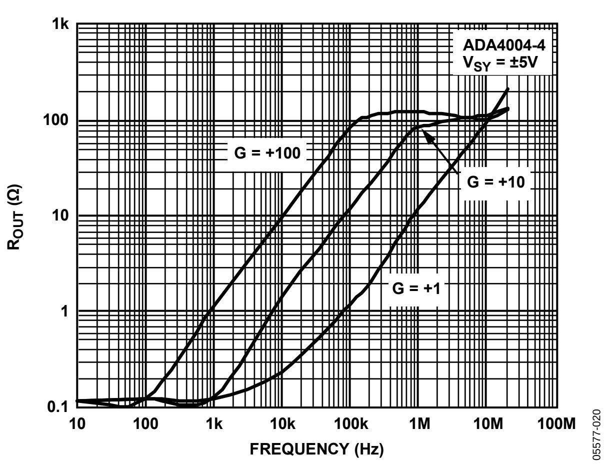

Figure 20. Output Impedance vs. Frequency

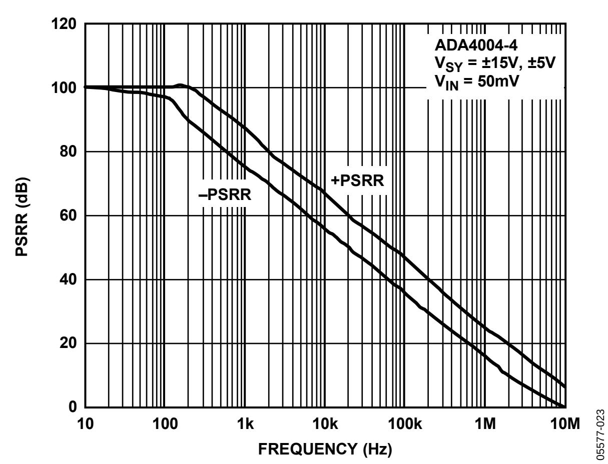

Figure 23. PSRR vs. Frequency

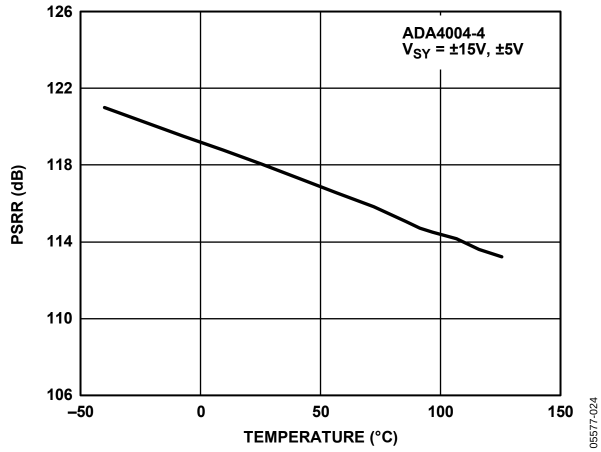

Figure 24. PSRR vs. Temperature

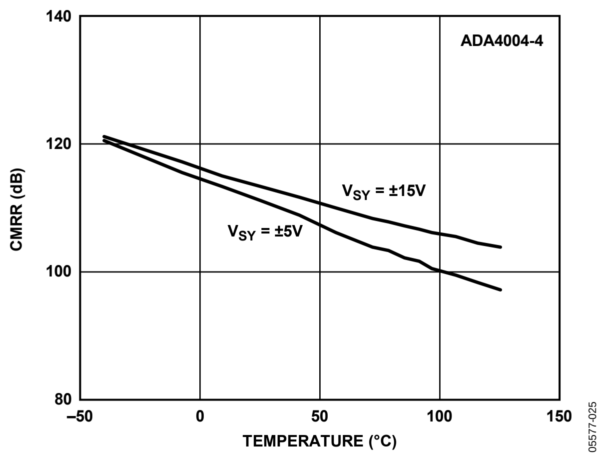

Figure 25. CMRR vs. Temperature

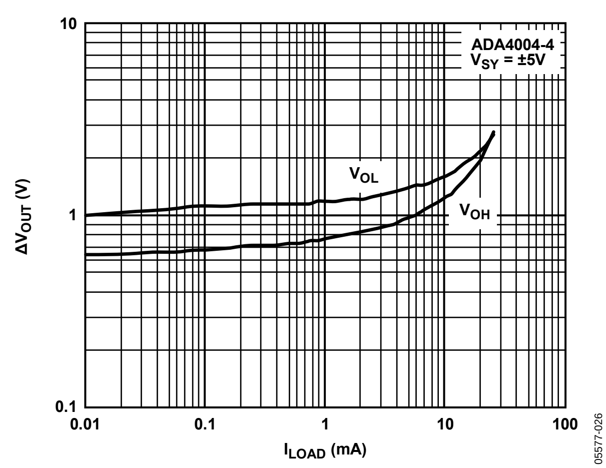

Figure 26. Output Voltage vs. Current Load

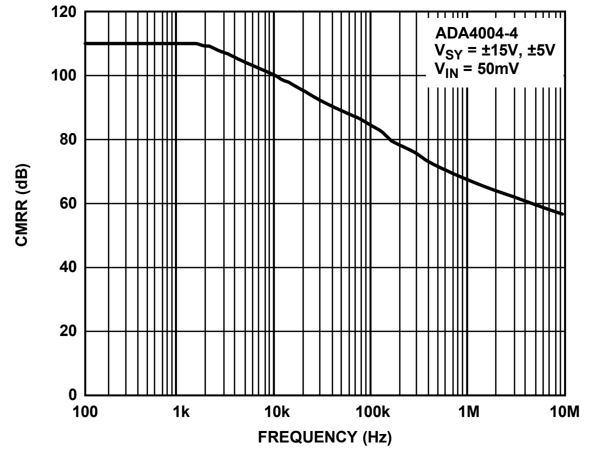

Figure 27. CMRR vs. Frequency

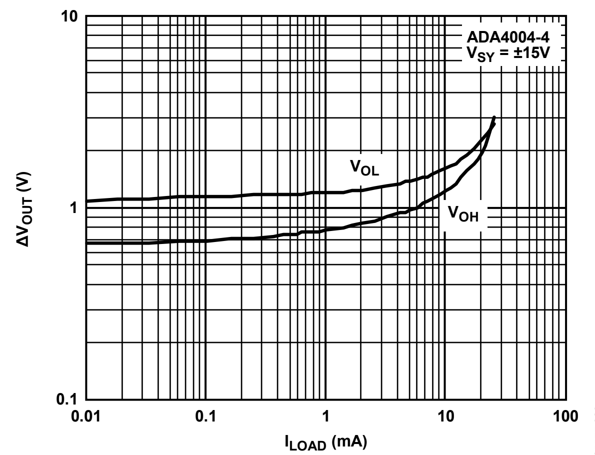

Figure 28. Output Voltage vs. Current Load

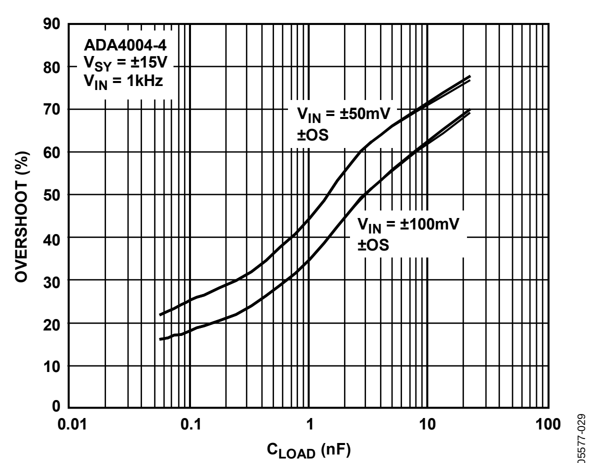

Figure 29. Small-Signal Overshoot vs. Capacitive Load

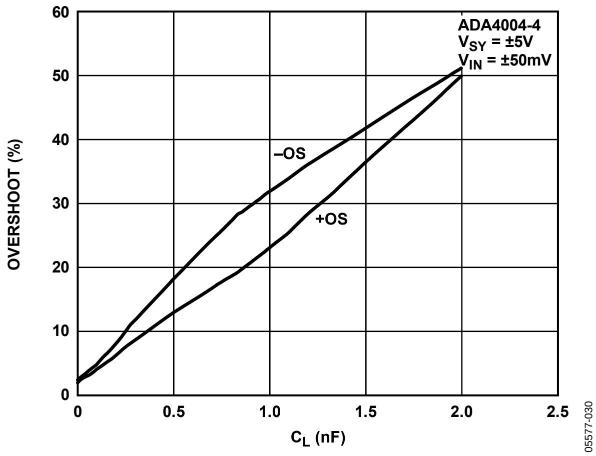

Figure 30. Small-Signal Overshoot vs. Capacitive Load

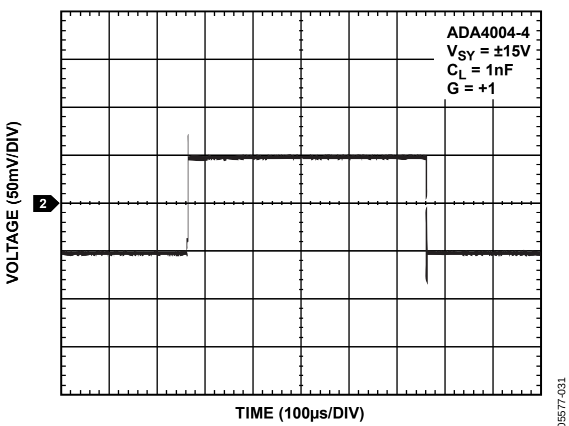

Figure 31. Small-Signal Transient Response

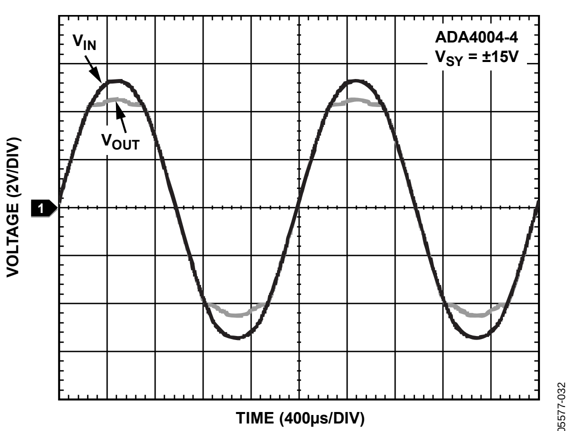

Figure 32. No Phase Reversal

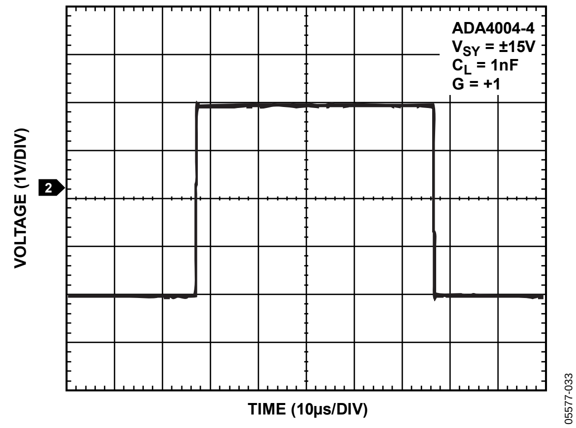

Figure 33. Large-Signal Transient Response

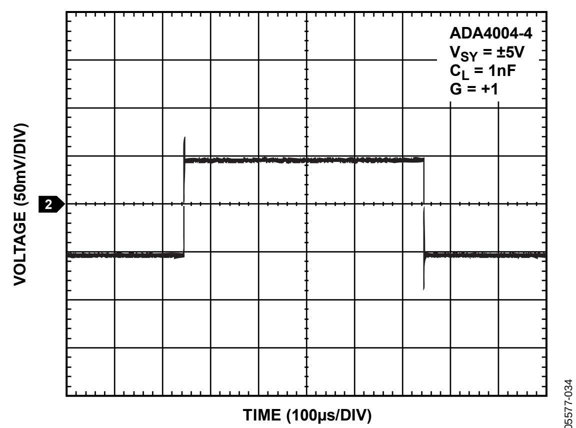

Figure 34. Small-Signal Transient Response

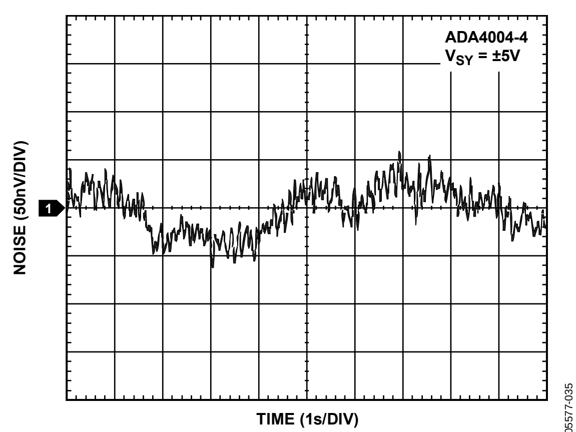

Figure 35. Voltage Noise (0.1 Hz to 10 Hz)

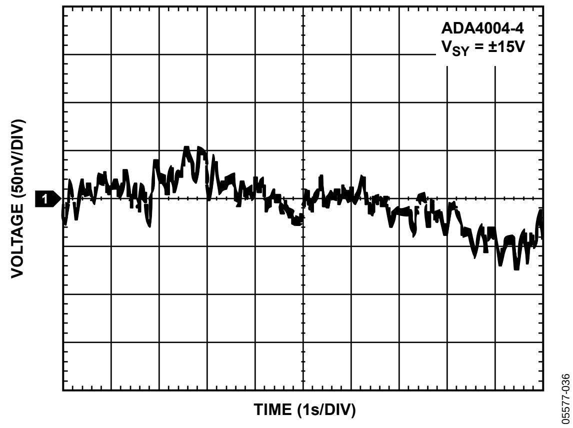

Figure 36. Voltage Noise (0.1 Hz to 10 Hz)

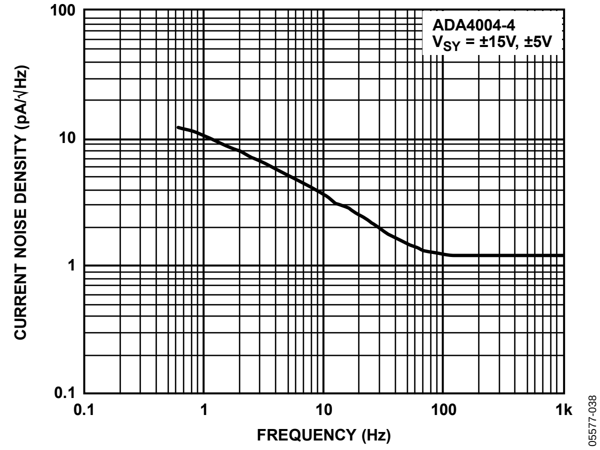

Figure 38. Current Noise Density vs. Frequency

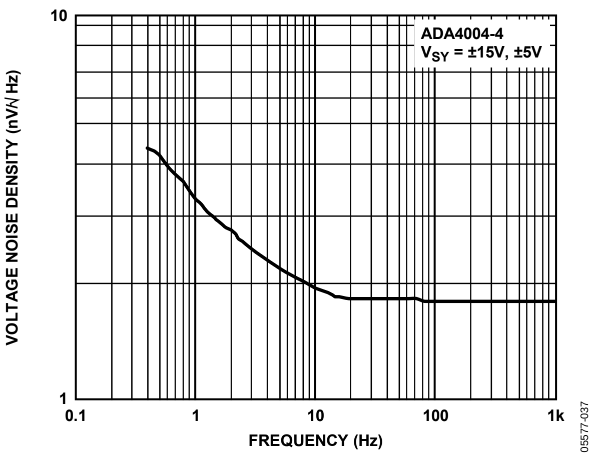

Figure 37. Voltage Noise Density vs. Frequency

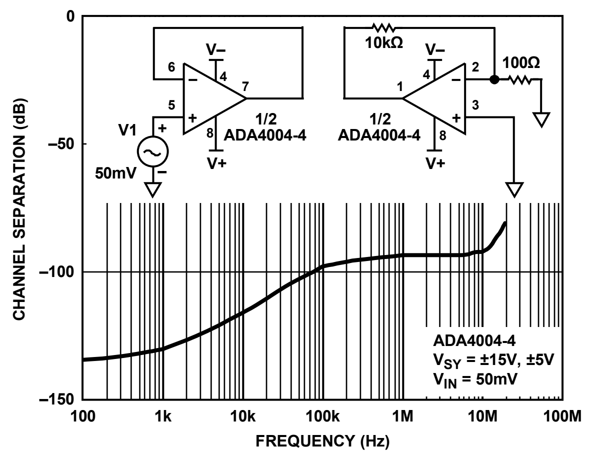

Figure 39. Channel Separation vs. Frequency

OUTLINE DIMENSIONS

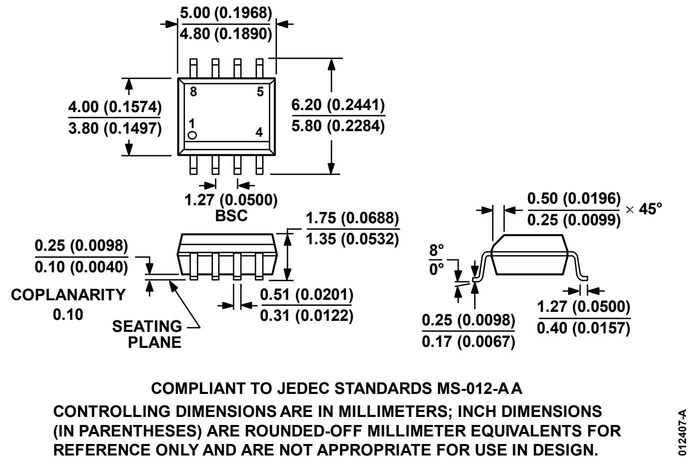

Figure 40. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

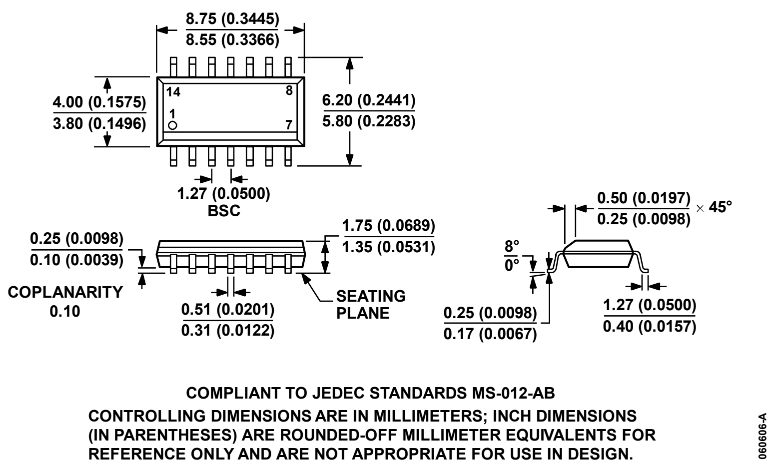

Figure 41. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

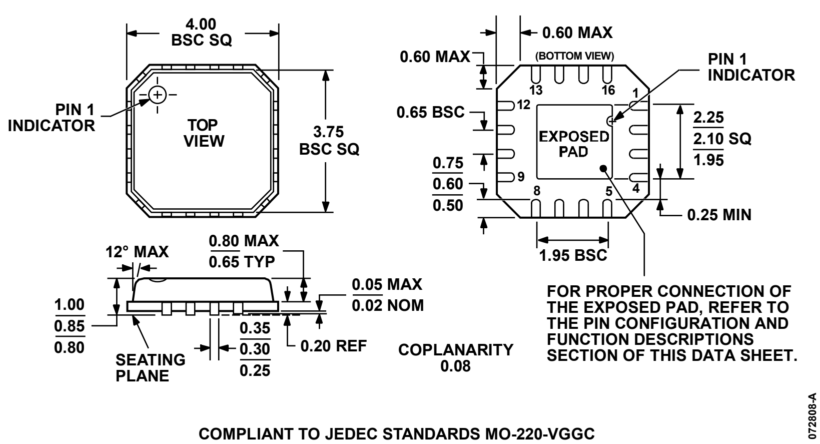

Figure 42. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

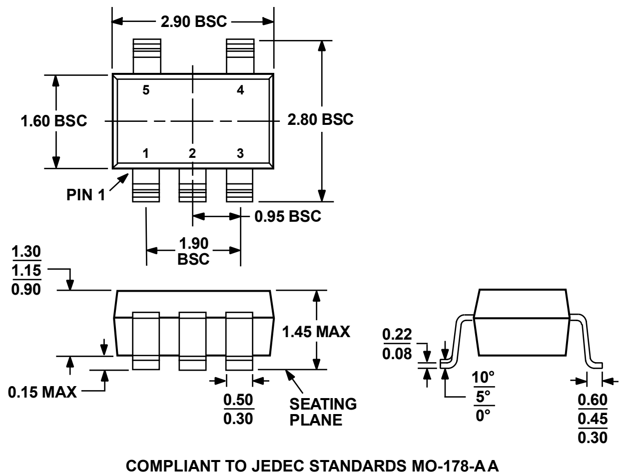

Figure 43. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

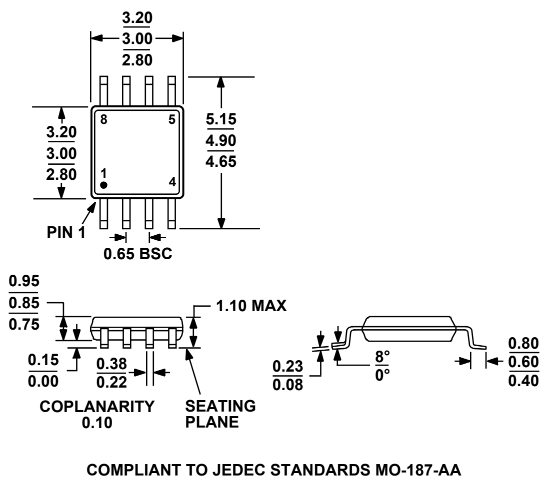

Figure 44. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADA4004-1ARJZ-R2[1]	−40°C to +125°C	5-Lead SOT-23	RJ-5	A1M
ADA4004-1ARJZ-R7[1]	−40°C to +125°C	5-Lead SOT-23	RJ-5	A1M
ADA4004-1ARJZ-RL[1]	−40°C to +125°C	5-lead SOT-23	RJ-5	A1M
ADA4004-1ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-1ARZ-R7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-1ARZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-2ARMZ[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A1N
ADA4004-2ARMZ-RL[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A1N
ADA4004-2ARMZ-R7[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A1N
ADA4004-2ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-2ARZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-2ARZ-RL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4004-4ACPZ-R2[1]	−40°C to +125°C	16-Lead LFCSP_VQ	CP-16-4	
ADA4004-4ACPZ-R7[1]	−40°C to +125°C	16-Lead LFCSP_VQ	CP-16-4	
ADA4004-4ACPZ-RL[1]	−40°C to +125°C	16-Lead LFCSP_VQ	CP-16-4	
ADA4004-4ARZ[1]	−40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4004-4ARZ-R7[1]	−40°C to +125°C	14-Lead SOIC_N	R-14	
ADA4004-4ARZ-RL[1]	−40°C to +125°C	14-Lead SOIC_N	R-14	

[1] Z = RoHS Compliant Part.

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