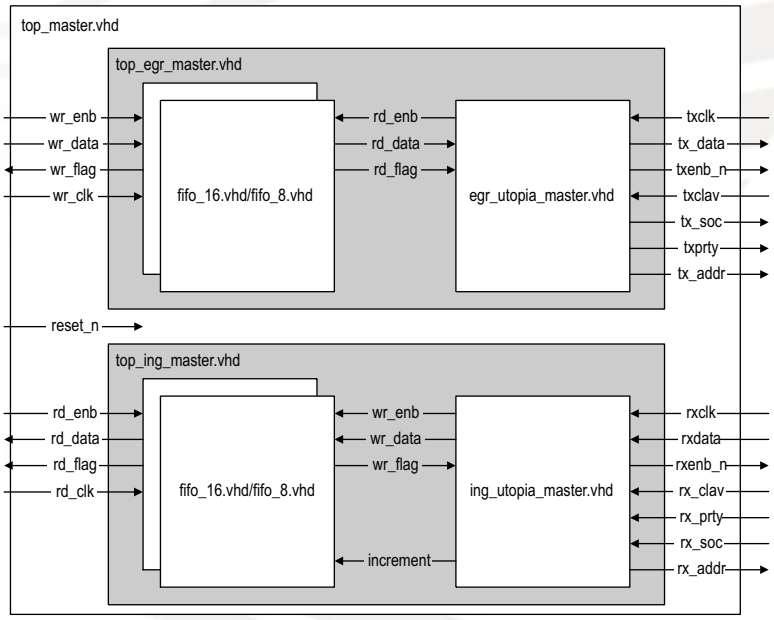
AvnetCore: Datasheet

Version 1.0, July 2006

UTOPIA Level 3 Link



Block Diagram

UTOPIA (Universal Test and Operations PHY Interface for ATM) level 3 defines the interface between the ATM or LINK layer and a Physical Layer (PHY) device. The UTOPIA level 3 standard defines a full duplex interface with a Master/Slave format. The Slave or LINK layer device responds to the requests from the PHY or Master device. The Master performs PHY arbitration and initiates data transfers to and from the Slave. The ATM forum has defined the UTOPIA Level 3 as either 8 or 32 bits in width, at up to 104 MHz, supporting an OC48 channel at 2.5 Gbps.

Intended Use:

- Cell Processors
- Switch Fabrics
- Networking
- Telecommunications

Features:

- Function compatible with ATM Forum
- Asynchronous/synchronous FIFO using RAM
- Up to 256 phys supported
- 8/16/32 bit interfaces supported
- Simple system side FIFO interface
- Flow control and polling integrated

Targeted Devices:

- Axcelerator Family

Core Deliverables:

- Netlist Version
  - > Netlist compatible with the Actel Designer place and route tool
  - > Compiled RTL simulation model, compliant with the Actel Libero® environment
- RTL Version
  - > VHDL Source Code
- All
  - > User Guide
  - > Test Bench

Synthesis and Simulation Support:

- Synthesis: Synplicity®
- Simulation: Model*Sim*®
- Other tools supported upon request

Verification:

- Test Bench
- Test Vectors

Actel CompanionCore

AVNET Memec

Functional Description

This core conforms to the appropriate standard(s). In general, standards do not define the internal user interface, only the external interfaces and protocols. Therefore, Avnet Memec has created a simple FIFO interface to this core for easy user connectivity. This document describes this Avnet Memec created interface. Please consult the appropriate standards document for all external signaling.

TOP_MASTER

This is the top level of the core. Its only purpose is to serve as a container to instantiate the Ingress and Egress modules.

Egress Master

The egress master is responsible for polling the PHYs and internal queues in order to send cells to the slave device.

Ingress/Egress FIFO

The FIFO contains the RAM FIFO and the pointer processing blocks. The FIFO operates in synchronous and asynchronous systems. The FIFO contains additional logic to implement a SOC-SOC pointer reset. There is one FIFO per PHY polled.

Ingress Master

The Ingress master is responsible for polling the PHYs and internal queues in order to accept cells from the slave device.

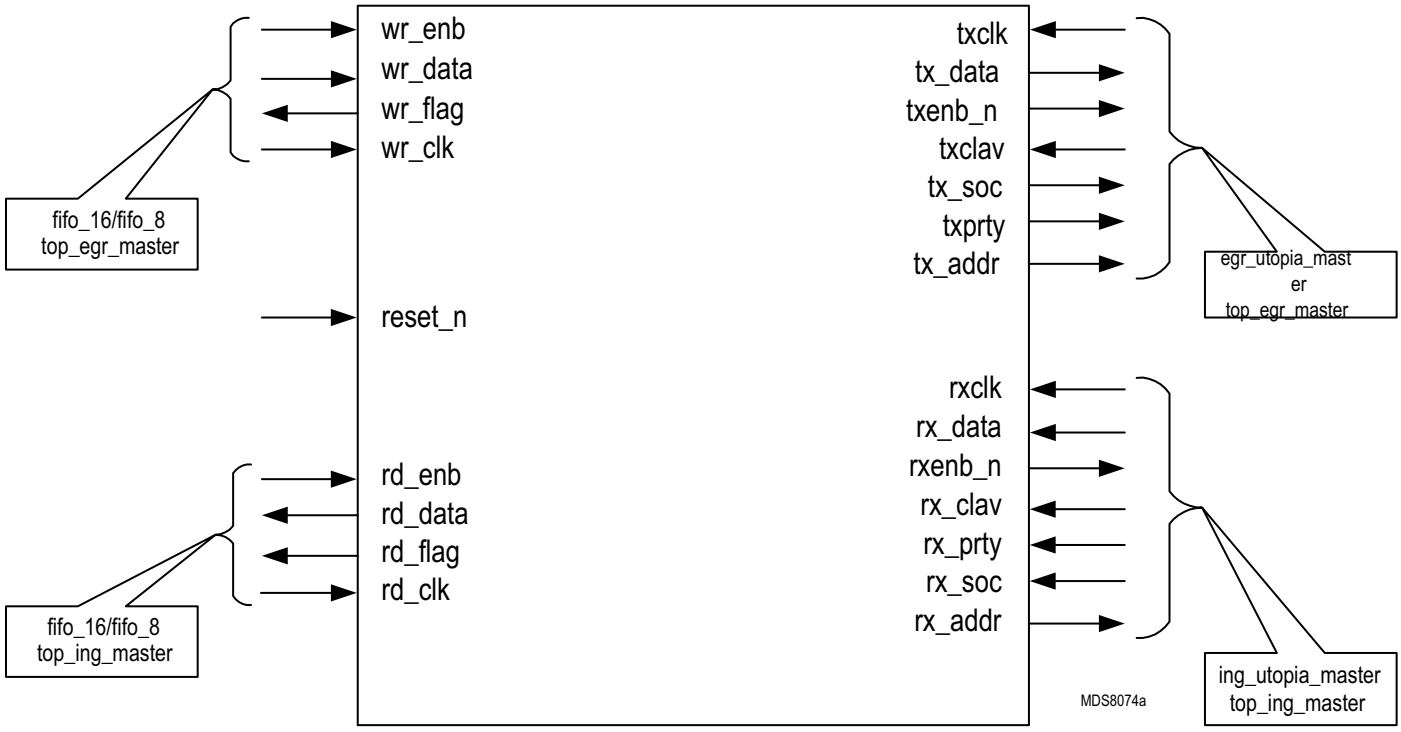


Figure 1: Logic Symbol

Device Requirements

Family	Device	Utilization			Performance
		COMB	SEQ	Tiles	
Axcelerator	AX250	38%	76%	n/a	104 MHz
ProASIC3	A3PE600	n/a	n/a	20%	97 MHz
ProASIC^{PLUS}	APA150	n/a	n/a	53%	85 MHz

Table 1: Device Utilization and Performance

Verification and Compliance

The testbench is self-checking, which means that if there is an error detected in the start word, end word, or payload the testbench will assert one or both of two error signals. The test checks for errors at two stages in the testbench: when the cells (packets) are looped back through the PHY device (SIG_LOOP_ERROR_OUT), and upon reading out of the link device (SIG_ERROR_OUT). This core has also been used successfully in customer designs.

Signal Descriptions

The following signal descriptions define the IO signals.

Signal	Width	Direction	Description
WR_ENB	N	Input	Write enable signal for FIFO
WR_DATA	N*8/16/32	Input	Write data bus for FIFO
WR_FLAG	N	Output	Write flag indicating if FIFO can accept another cell
WR_CLK	N	Input	Write clock for the FIFO
RESET_N	1	Input	Reset signal from user logic
RD_ENB	N	Input	Read enable signal for the FIFO
RD_DATA	N*8/16/32	Output	Read data bus for the FIFO
RD_FLAG	N	Output	FIFO read flag indicating that a cell is ready to be read from the ports FIFO
RD_CLK	N	Input	Read clock for the FIFO
TXCLK	1	Input	Tx utopia clock
TX_DATA	8/16/32	Output	Tx utopia data bus
TXENB_N	1	Output	Tx utopia enable signal
TXCLAV	1/N<4	Input	Tx utopia cell available signal(s)
TX_SOC	1	Output	Tx utopia start of cell signal
TXPRTY	1	Output	Tx utopia parity signal
TX_ADDR	8	Output	Tx utopia polling address bus
RXCLK	1	Input	Ingress utopia clock
RXDATA	8/16/32	Input	Ingress utopia data bus
RXENB_N	1	Output	Ingress utopia enable signal
RX_CLAV	1/ N<4	Input	Ingress utopia cell available signal(s)
RX_PRTY	1	Input	Ingress utopia parity signal
RX_SOC	1	Input	Ingress utopia start of cell signal
RX_ADDR	8	Output	Ingress utopia address bus

Table 2: Core I/O Signals

Timing

Since the ATM Forum specification fully defines the line side of the UTOPIA Level 3 interface, timing for that is not replicated here. Instead, only user (FIFO) interface timing information is presented here. The figure below shows the functional timing for FIFO reads and writes.

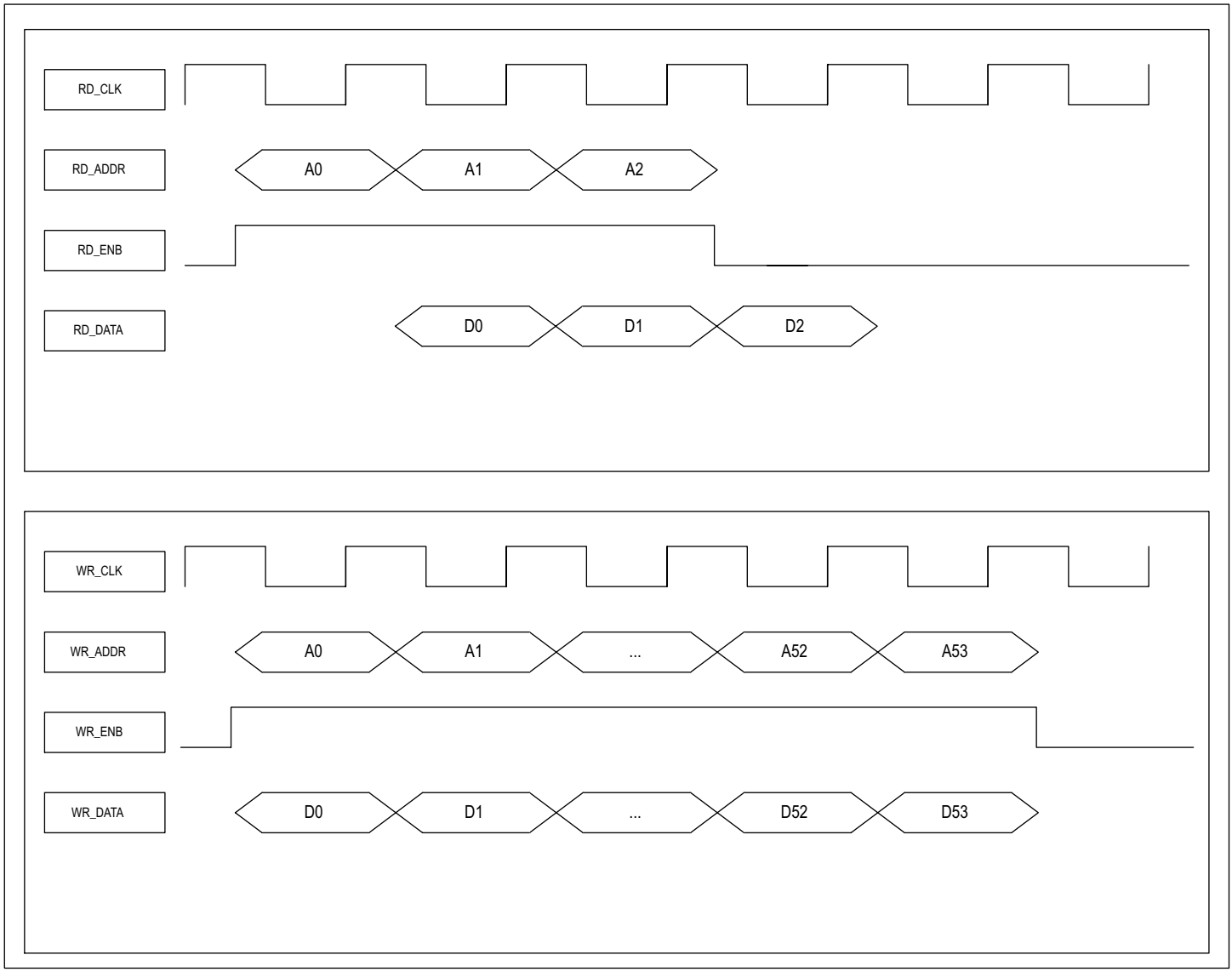


Figure 3: FIFO Timing

Recommended Design Experience

For the source version, users should be familiar with HDL entry and Actel design flows. Users should be familiar with Actel Libero Integrated Design Environment (IDE) and preferably with Synplify and Model*Sim*.

Ordering Information

The CORE is provided under license from Avnet Memec for use in Actel programmable logic devices. Please contact Avnet Memec for pricing and more information.

Contact Information:

North America
10805 Rancho Bernardo Road
Suite 100
San Diego, California 92127
United States of America
TEL: +1 858 385 7500
FAX: +1 858 385 7770

Europe, Middle East & Africa
Mattenstrasse 6a
CH-2555 Brügg BE
Switzerland
TEL: +41 0 32 374 32 00
FAX: +41 0 32 374 32 01

Ordering Information:

Part Number	Hardware	Resale
MC-ACT-UL3LINK-NET	Actel UL3LINK Netlist	Contact for pricing
MC-ACT-UL3LINK-VHDL	Actel UL3LINK VHDL	Contact for pricing

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www.em.avnet.com/actel