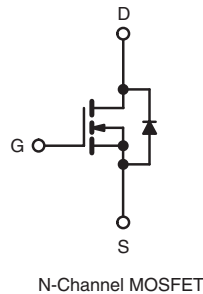
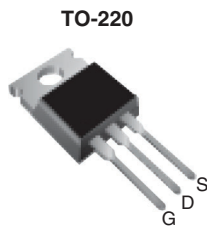


## Power MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	200	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 5.0 V	0.18
Q <sub>g</sub> (Max.) (nC)	66	
Q <sub>gs</sub> (nC)	9.0	
Q <sub>gd</sub> (nC)	38	
Configuration	Single	



### FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- R<sub>DS(on)</sub> Specified at V<sub>GS</sub> = 4 V and 5 V
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available


**RoHS\***  
COMPLIANT

### DESCRIPTION

Third generation Power MOSFETs from Vishay provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRFL640PbF
	SiHL640-E3
SnPb	IRFL640
	SiHL640

ABSOLUTE MAXIMUM RATINGS T <sub>C</sub> = 25 °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Gate-Source Voltage			V <sub>GS</sub>	± 10	V
Continuous Drain Current	V <sub>GS</sub> at 5.0 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	17	A
		T <sub>C</sub> = 100 °C		11	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	68	
Linear Derating Factor				1.0	W/°C
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	580	mJ
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	10	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	13	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	125	W
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 3.0 mH, R<sub>G</sub> = 25 Ω I<sub>AS</sub> = 17 A (see fig. 12).
- I<sub>SD</sub> ≤ 17 A, dI/dt ≤ 150 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	200	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.27	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	-	2.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 10$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 200\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 160\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$ , $I_D = 10\text{ A}^b$	-	-	0.18	$\Omega$
		$V_{GS} = 4.0\text{ V}$ , $I_D = 8.5\text{ A}^b$	-	-	0.27	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 10\text{ A}^b$	16	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ $V_{DS} = 25\text{ V}$ $f = 1.0\text{ MHz}$ , see fig. 5	-	1800	-	pF
Output Capacitance	$C_{oss}$		-	400	-	
Reverse Transfer Capacitance	$C_{rss}$		-	120	-	
Total Gate Charge	$Q_g$	$V_{GS} = 5.0\text{ V}$ , $I_D = 17\text{ A}$ , $V_{DS} = 160\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	66	nC
Gate-Source Charge	$Q_{gs}$		-	-	9.0	
Gate-Drain Charge	$Q_{gd}$		-	-	38	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\text{ V}$ , $I_D = 17\text{ A}$ $R_G = 4.6\text{ }\Omega$ , $R_D = 5.7\text{ }\Omega$ , see fig. 10 <sup>b</sup>	-	8.0	-	ns
Rise Time	$t_r$		-	83	-	
Turn-Off Delay Time	$t_{d(off)}$		-	44	-	
Fall Time	$t_f$		-	52	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact	-	4.5	-	nH
Internal Source Inductance	$L_S$		-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode	-	-	17	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	68	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 17\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	2.0	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = 17\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	310	470	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	3.2	4.8	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

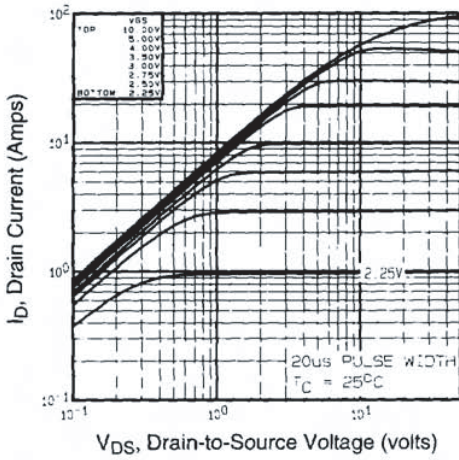


Fig. 1 - Typical Output Characteristics,  $T_C = 25^\circ\text{C}$

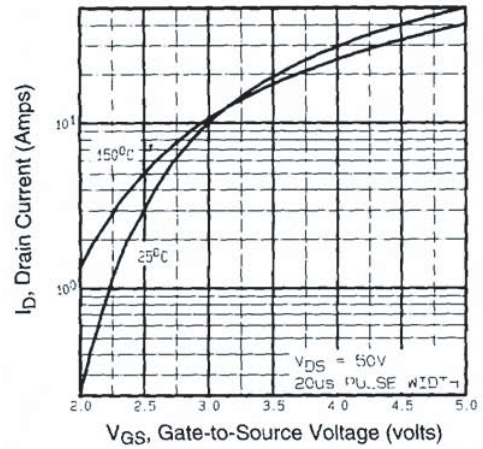


Fig. 3 - Typical Transfer Characteristics

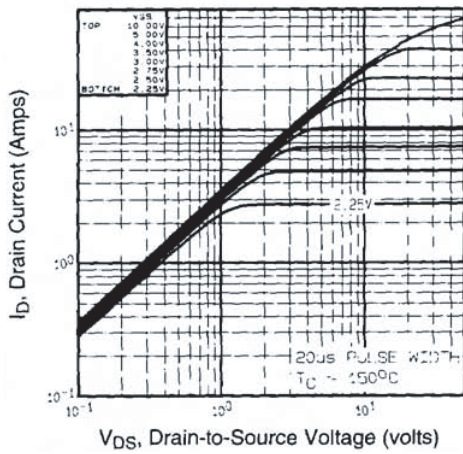


Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$

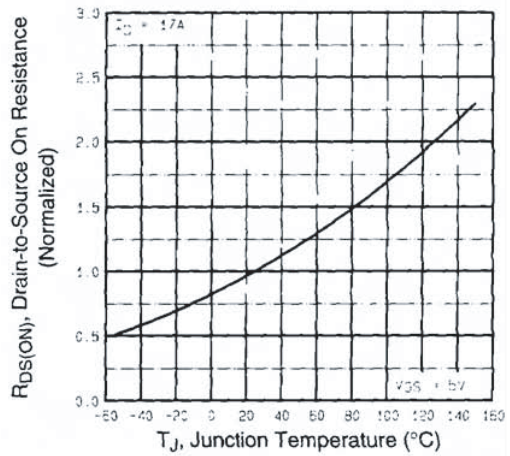


Fig. 4 - Normalized On-Resistance vs. Temperature

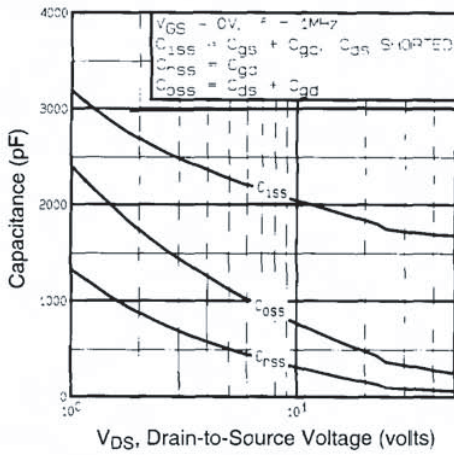


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

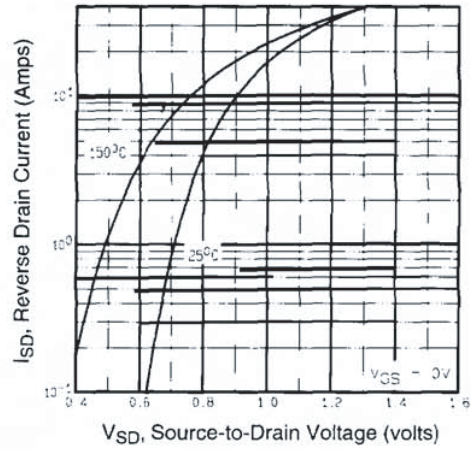


Fig. 7 - Typical Source-Drain Diode Forward Voltage

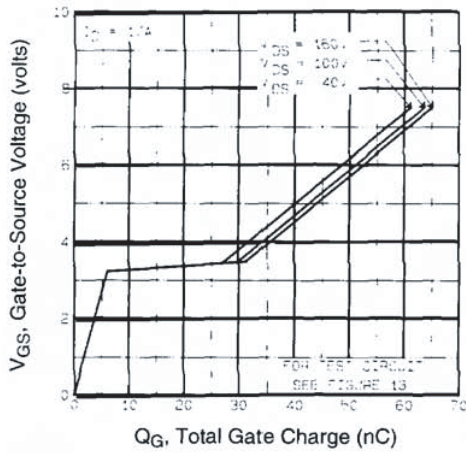


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

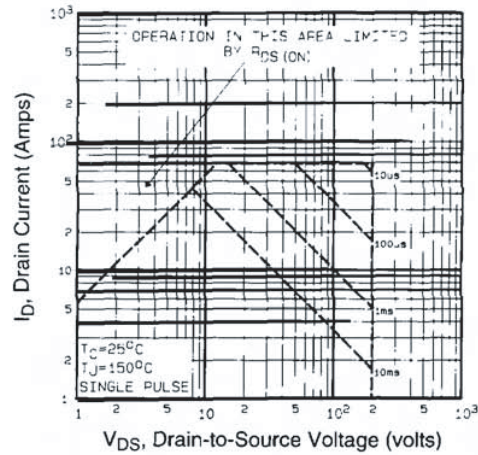


Fig. 8 - Maximum Safe Operating Area

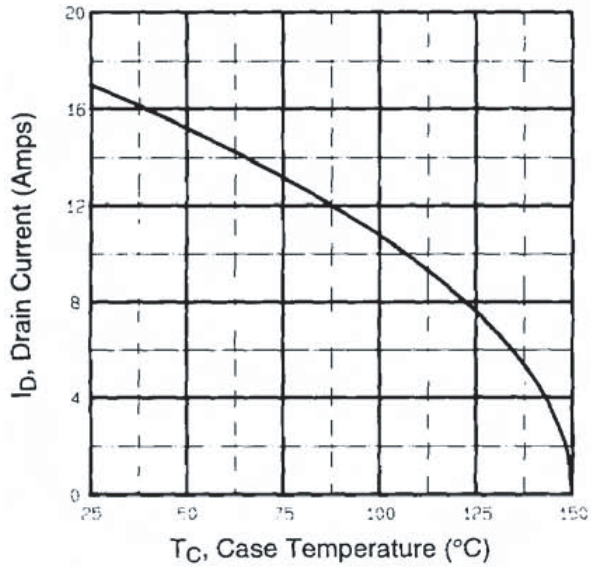


Fig. 9 - Maximum Drain Current vs. Case Temperature

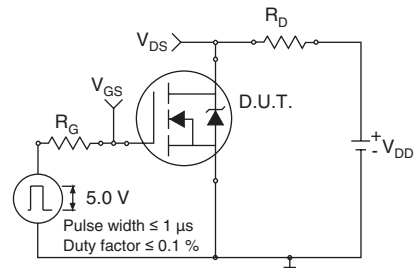


Fig. 10a - Switching Time Test Circuit

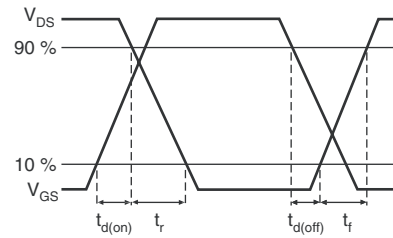


Fig. 10b - Switching Time Waveforms

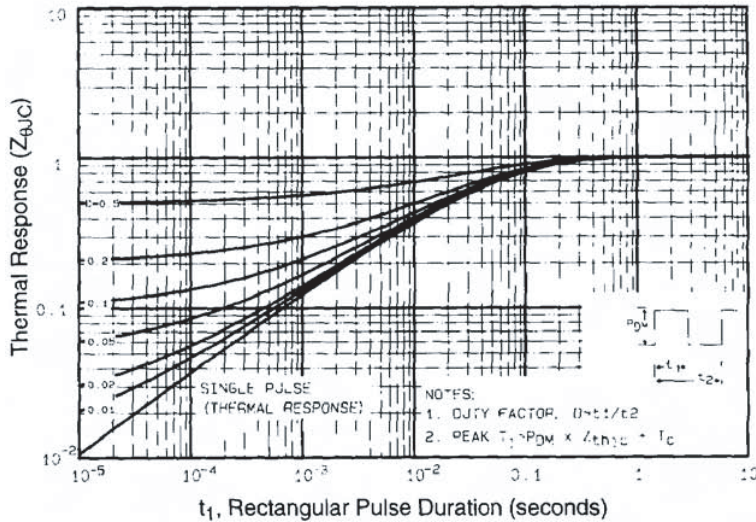


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

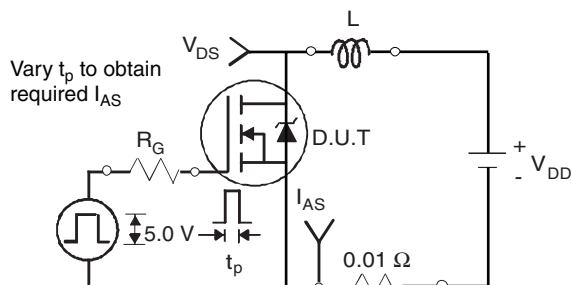


Fig. 12a - Unclamped Inductive Test Circuit

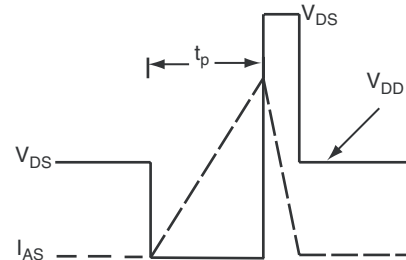


Fig. 12b - Unclamped Inductive Waveforms

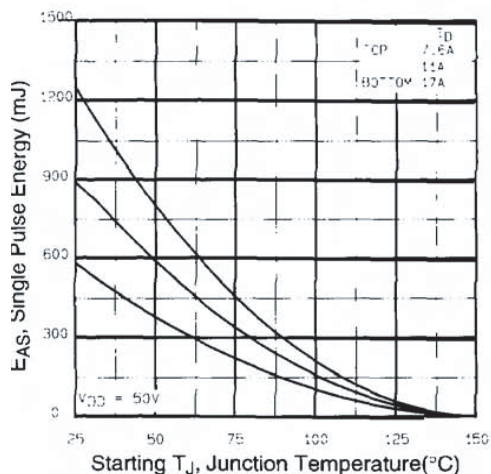


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

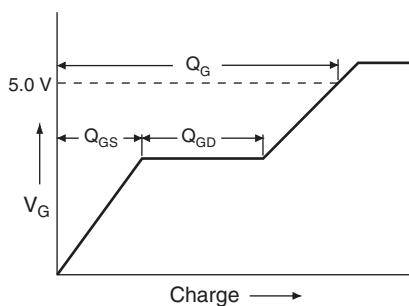


Fig. 13a - Basic Gate Charge Waveform

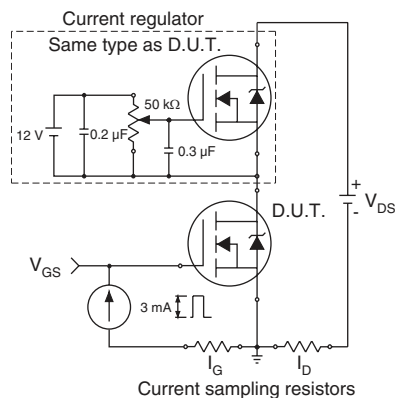
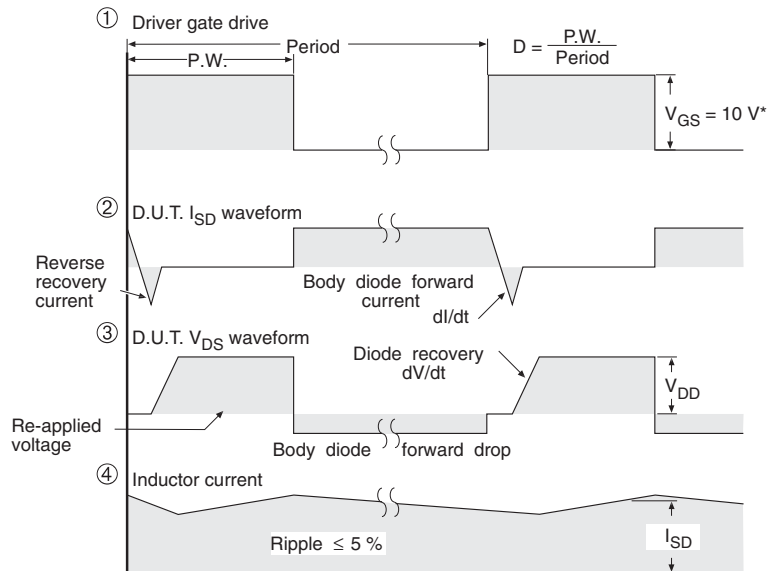
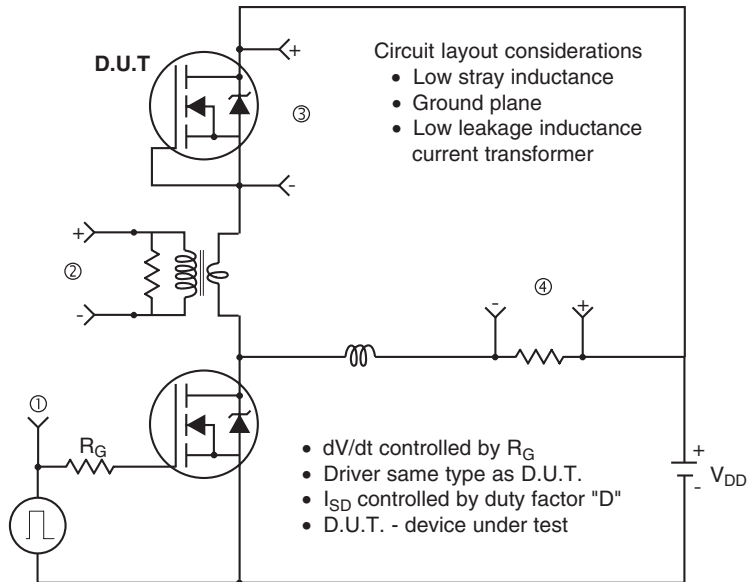


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**


\*  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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