



AON6710

N-Channel Enhancement Mode Field Effect Transistor

SRFET™



General Description

SRFET™ The AON6710/L uses advanced trench technology with a monolithically integrated Schottky diode to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a low side FET in SMPS, load switching and general purpose applications. AON6710 and AON6710L are electrically identical.

- RoHS Compliant
- AON6710L is Halogen Free

Features

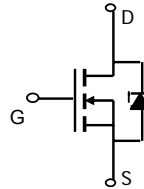
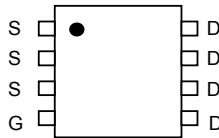
- $V_{DS} (V) = 30V$
- $I_D = 20A (V_{GS} = 10V)$
- $R_{DS(ON)} < 4.7m\Omega (V_{GS} = 10V)$
- $R_{DS(ON)} < 6.7m\Omega (V_{GS} = 4.5V)$

Fits SOIC8 footprint !



DFN5X6

Top View



SRFET™
Soft Recovery MOSFET:
Integrated Schottky Diode

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^{BJ}	I_D	$T_C=25^\circ C$	30
		$T_C=100^\circ C$	30
Pulsed Drain Current	I_{DM}	100	A
Continuous Drain Current ^H	I_{DSM}	$T_A=25^\circ C$	19
		$T_A=70^\circ C$	15
Avalanche Current ^C	I_{AR}	30	A
Repetitive avalanche energy $L=0.3mH$ ^C	E_{AR}	135	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ C$	62
		$T_C=100^\circ C$	25
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ C$	2.5
		$T_A=70^\circ C$	1.6
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10s$	14.2	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	42	$^\circ C/W$
Maximum Junction-to-Case ^C	$R_{\theta JC}$	1.2	2.0	$^\circ C/W$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=1\text{mA}, V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $T_J=125^\circ\text{C}$			0.1 20	mA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			0.1	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.3	1.5	2.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=5\text{V}$	100			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$ $T_J=125^\circ\text{C}$		3.7	4.7	m Ω
		$V_{GS}=4.5\text{V}, I_D=20\text{A}$		5.3	6.7	
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		90		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.36	0.5	V
I_S	Maximum Body-Diode Continuous Current				5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$		3760	4512	pF
C_{oss}	Output Capacitance			682		pF
C_{rss}	Reverse Transfer Capacitance			314		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		0.75	1.5	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=20\text{A}$		62	72	nC
$Q_g(4.5\text{V})$	Total Gate Charge			29		nC
Q_{gs}	Gate Source Charge			12		nC
Q_{gd}	Gate Drain Charge			12		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=0.75\Omega,$ $R_{GEN}=3\Omega$		9.5	12	ns
t_r	Turn-On Rise Time			8.5		ns
$t_{D(off)}$	Turn-Off Delay Time			34		ns
t_f	Turn-Off Fall Time			9		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=20\text{A}, di/dt=300\text{A}/\mu\text{s}$		18	27	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, di/dt=300\text{A}/\mu\text{s}$		22		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with $T_A=25^\circ\text{C}$.

B: The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsink is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.

D: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ\text{C}$.

G: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $\bar{T}_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

H: Surface mounted on a 1 in 2 FR-4 board with 2oz. Copper.

J: Maximum current is limited by bonding wire.

Prelim: :Jan 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

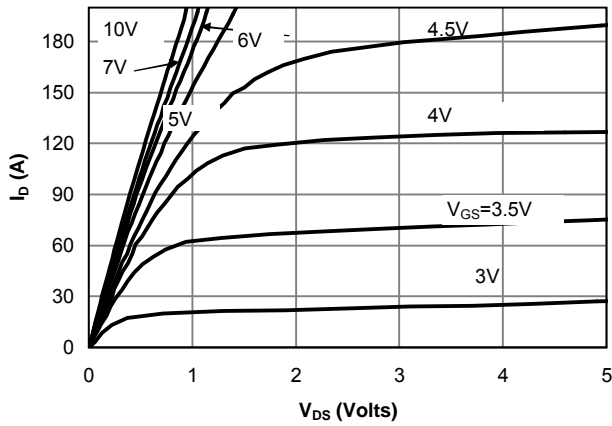


Figure 1: On-Region Characteristics

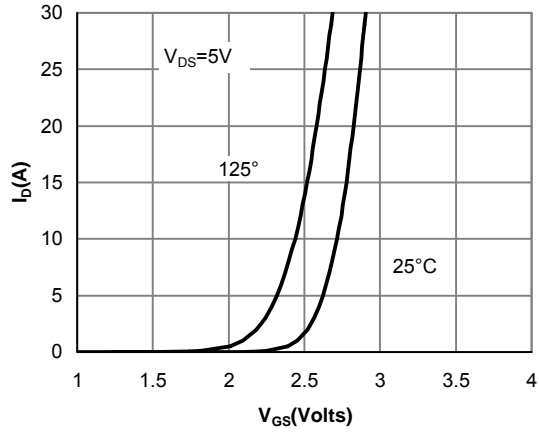


Figure 2: Transfer Characteristics

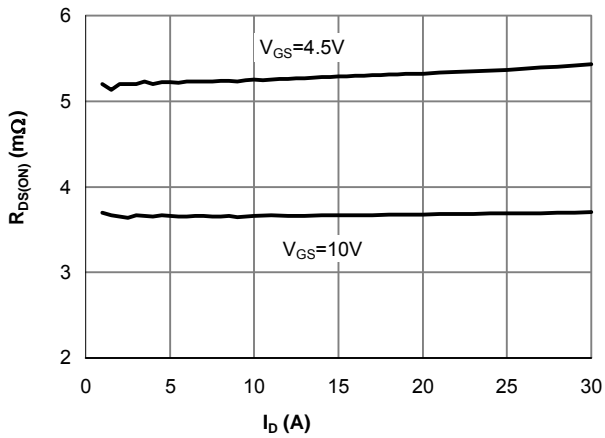


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

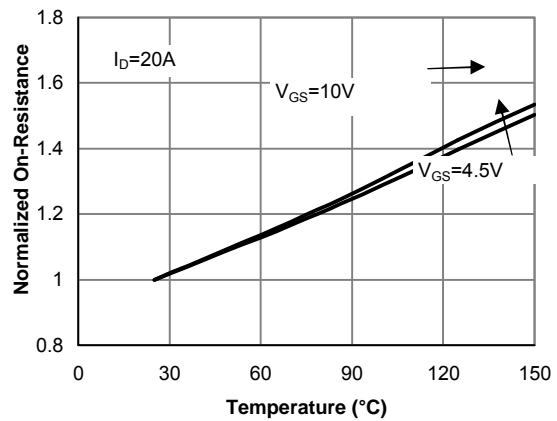


Figure 4: On-Resistance vs. Junction Temperature

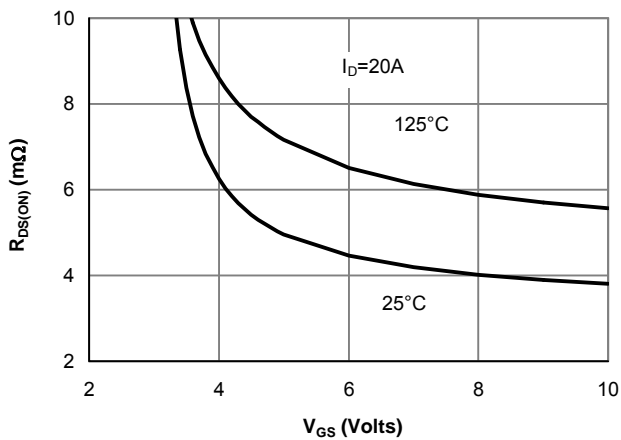


Figure 5: On-Resistance vs. Gate-Source Voltage

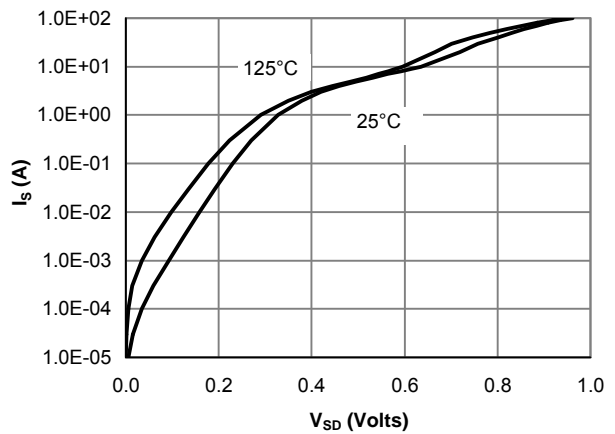


Figure 6: Body-Diode Characteristics

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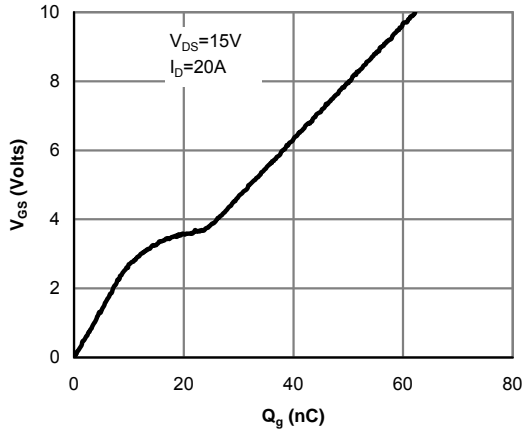


Figure 7: Gate-Charge Characteristics

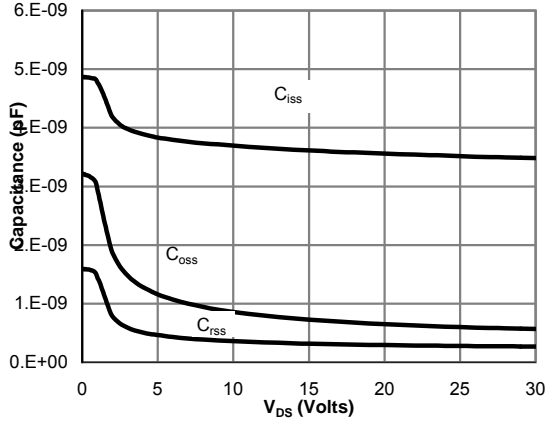


Figure 8: Capacitance Characteristics

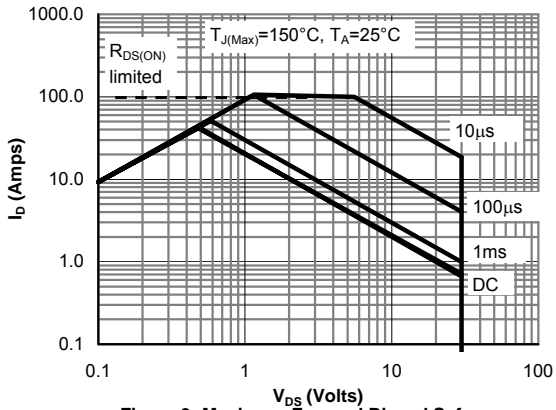


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

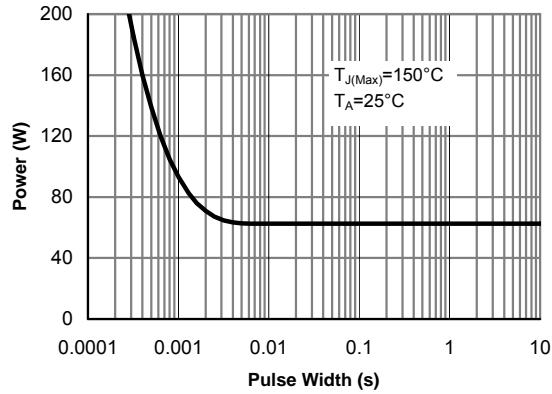


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

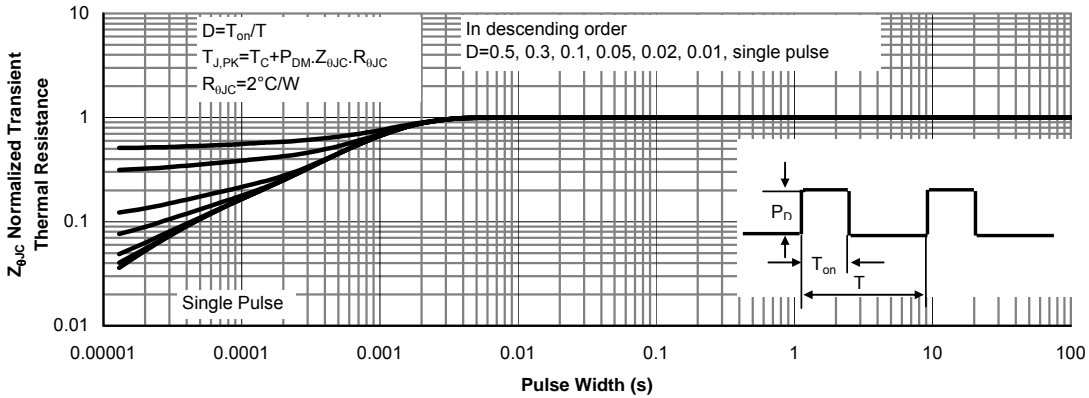


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

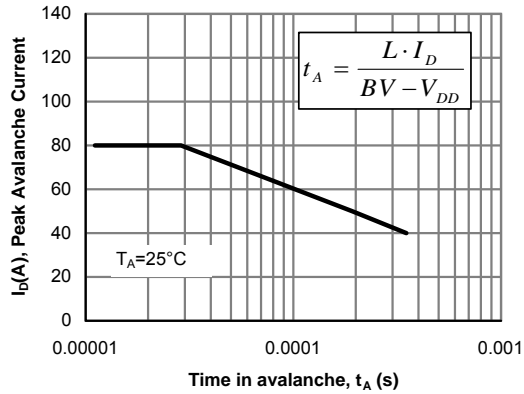


Figure 12: Single Pulse Avalanche capability

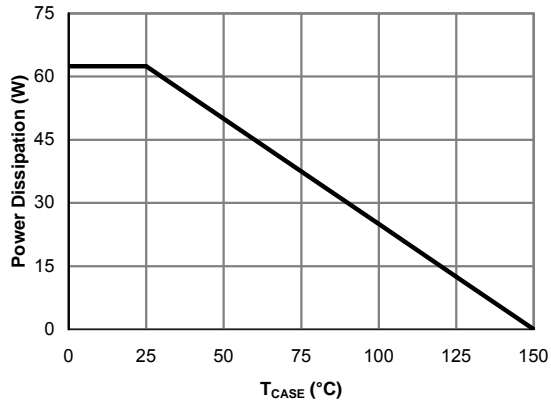


Figure 13: Power De-rating (Note B)

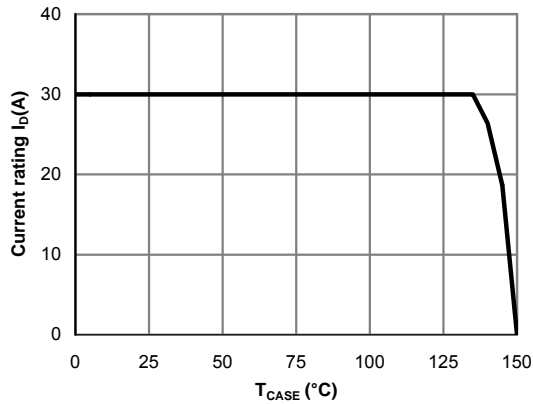


Figure 14: Current De-rating (Note B)

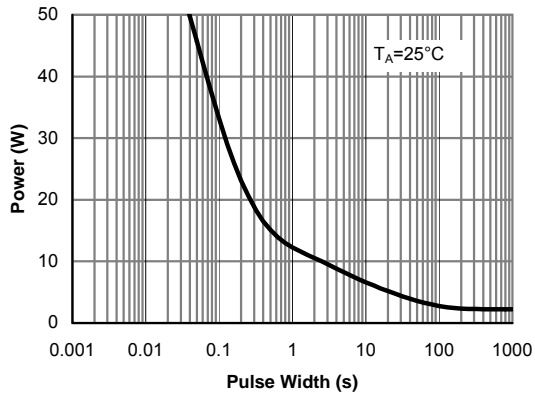


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)

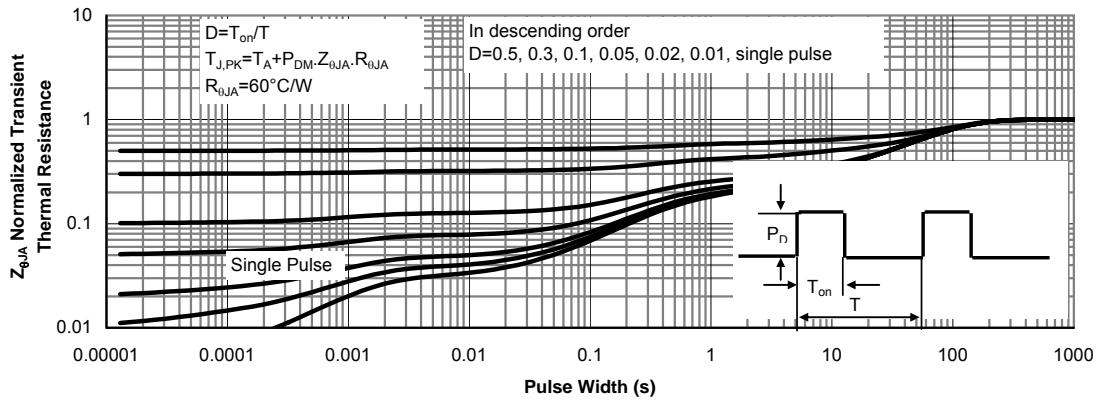


Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)