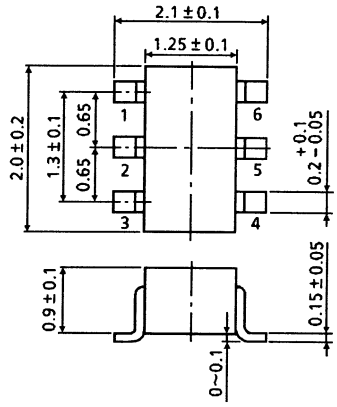
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

# SSM6K06FU

High Speed Switching Applications

- Small package
- Low on resistance : $R_{on}$ = 160 mΩ max (@$V_{GS}$ = 4 V)
  : $R_{on}$ = 210 mΩ max (@$V_{GS}$ = 2.5 V)
- Low gate threshold voltage

Unit: mm




1, 2, 5, 6 : DRAIN
3 : GATE
4 : SOURCE

US6

| | |
|---|---|
| JEDEC | — |
| JEITA | — |
| TOSHIBA | 2-2J1D |

Weight: 6.8 mg (typ.)

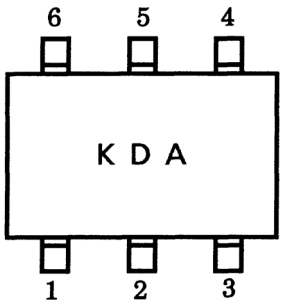
## Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DS}$ | 20 | V |
| Gate-source voltage | | $V_{GSS}$ | ±12 | V |
| Drain current | DC | $I_D$ | 1.1 | A |
| | Pulse | $I_{DP}$ | 2.2 | |
| Drain power dissipation (Ta = 25°C) | | $P_D$ (Note 1) | 300 | mW |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55~150 | °C |

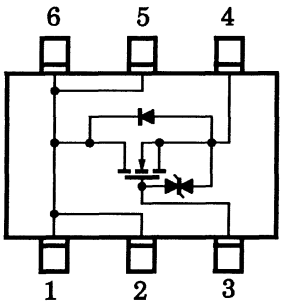
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 t, Cu pad: 0.32 $mm^2$ × 6) Figure 1.

## Marking




## Equivalent Circuit (top view)




## Handling Precaution

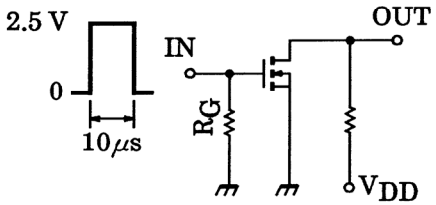
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

## Electrical Characteristics (Ta = 25°C)

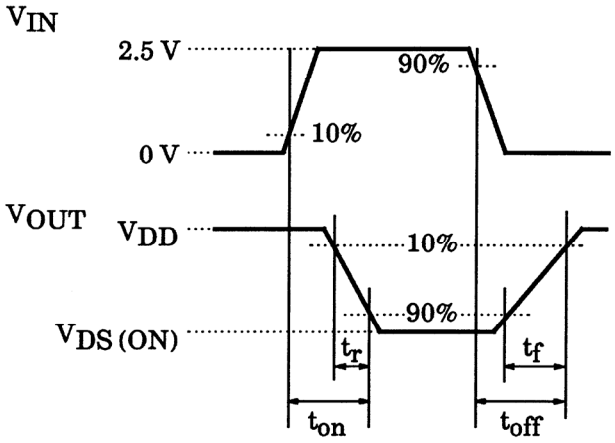
| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±12 V, $V_{DS}$ = 0 | — | — | ±1 | μA |
| Drain-source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = 1 mA, $V_{GS}$ = 0 | 20 | — | — | V |
| Drain cut-off current | | $I_{DSS}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 | — | — | 1 | μA |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = 3 V, $I_D$ = 0.1 mA | 0.6 | — | 1.1 | V |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = 3 V, $I_D$ = 0.5 A (Note 2) | 1.2 | — | — | S |
| Drain-source ON resistance | | $R_{DS\ (ON)}$ | $I_D$ = 0.5 A, $V_{GS}$ = 4 V (Note 2) | — | 120 | 160 | mΩ |
| | | | $I_D$ = 0.5 A, $V_{GS}$ = 2.5 V (Note 2) | — | 160 | 210 | |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz | — | 125 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz | — | 30 | — | pF |
| Output capacitance | | $C_{oss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz | — | 75 | — | pF |
| Switching time | Turn-on time | $t_{on}$ | $V_{DD}$ = 10 V, $I_D$ = 0.5 A, $V_{GS}$ = 0~2.5 V, $R_G$ = 4.7 Ω | — | 42 | — | ns |
| | Turn-off time | $t_{off}$ | | — | 100 | — | |

Note 2: Pulse test

## Switching Time Test Circuit




$V_{DD}$ = 10 V
$R_G$ = 4.7 Ω
D.U. ≦ 1%
$V_{IN}$ : $t_r$, $t_f$ < 5 ns
COMMON SOURCE
Ta = 25°C



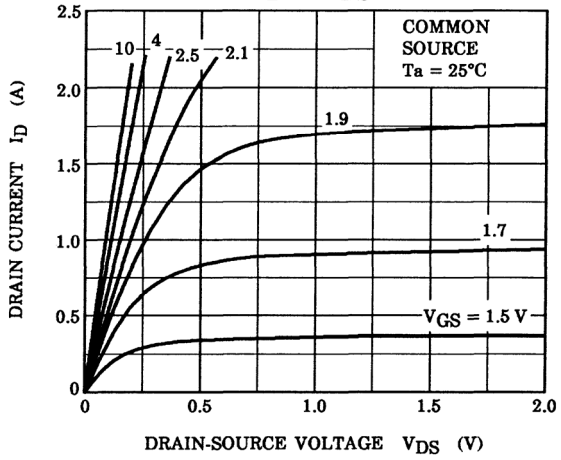

## Precaution

$V_{th}$ can be expressed as voltage between gate and source when low operating current value is $I_D$ = 100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires higher voltage than $V_{th}$ and $V_{GS\ (off)}$ requires lower voltage than $V_{th}$.

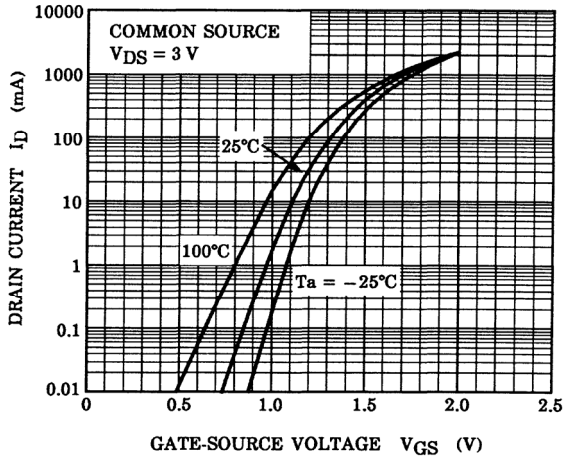
(Relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)

Please take this into consideration for using the device.

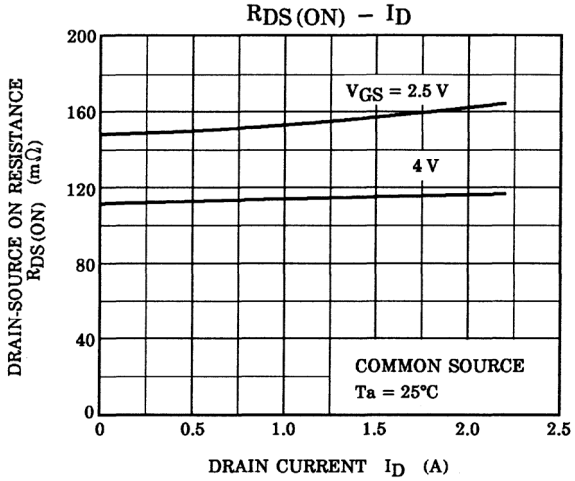
$I_D - V_{DS}$



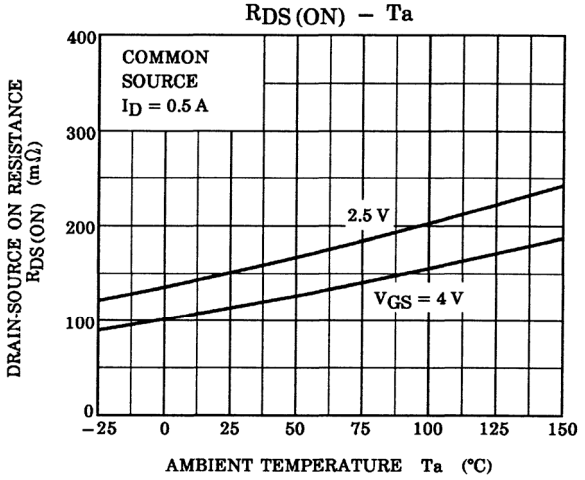

$I_D - V_{GS}$



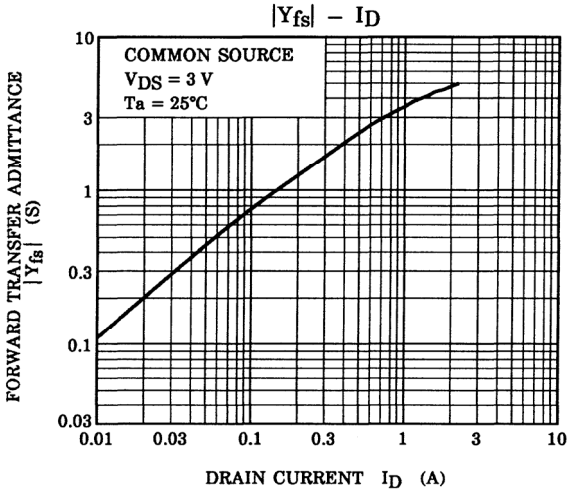

$R_{DS\,(ON)} - I_D$



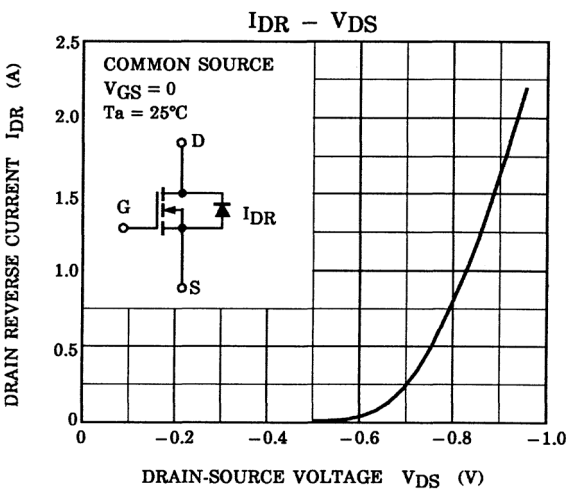

$R_{DS\,(ON)} - Ta$



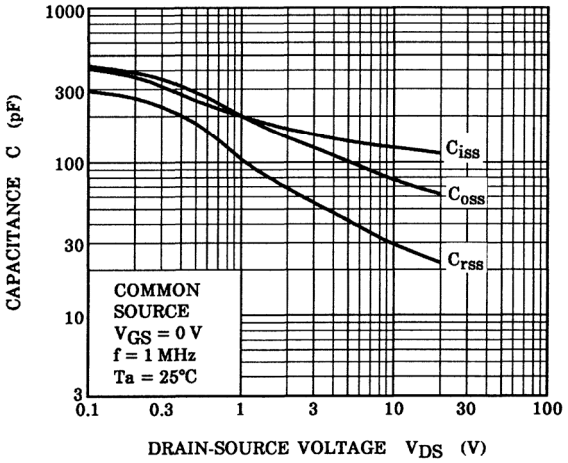

$|Y_{fs}| - I_D$



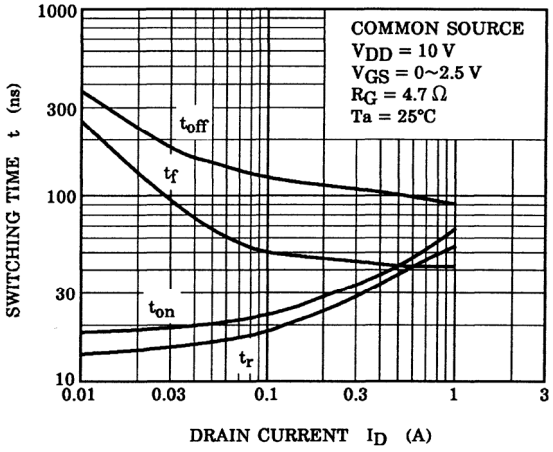

$I_{DR} - V_{DS}$



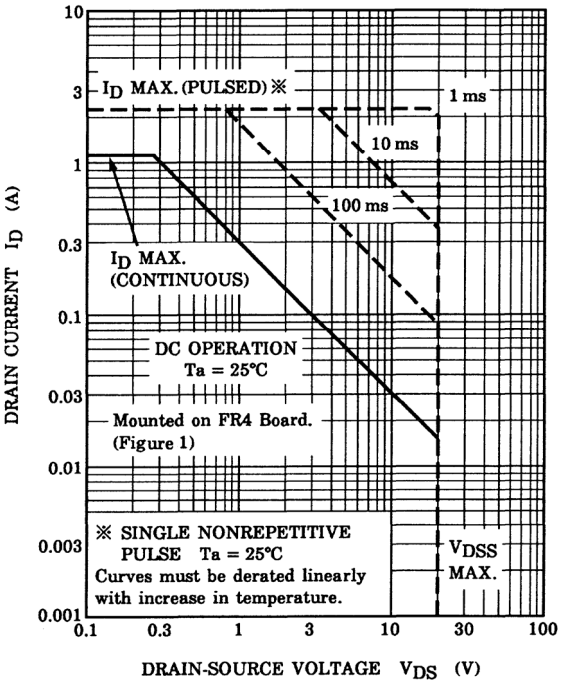
C – $V_{DS}$



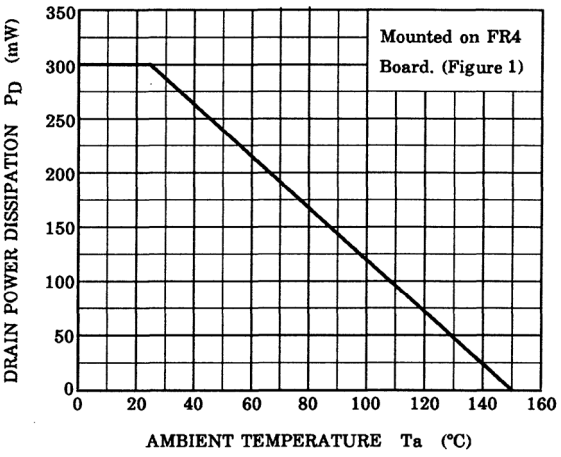

t – $I_D$




SAFE OPERATING AREA




$P_D$ – Ta



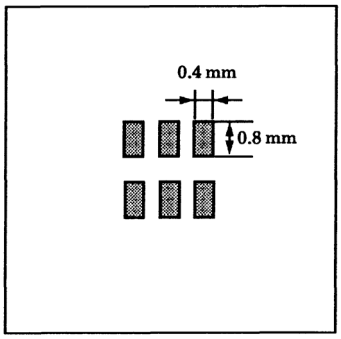



**Figure 1 25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.32 mm$^2$ × 6**

## RESTRICTIONS ON PRODUCT USE

20070701-EN GENERAL

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