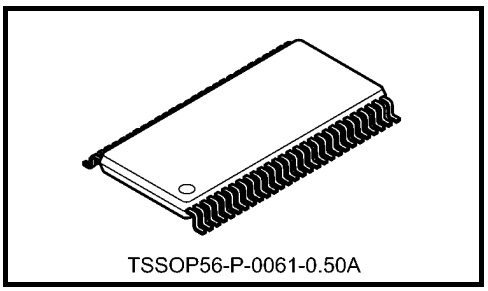
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCXH16543FT

Low-Voltage 16-Bit Registered Transceiver with Bushold



Weight: 0.25 g (typ.)

The TC74VCXH16543FT is a high-performance CMOS 16-bit registered transceiver. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The TC74VCXH16543FT can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low in order to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the Alatches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches.

Data flow from B to A is similar but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEAB}}$ inputs.

When the $\overline{\text{OE}}$ input is high, the outputs are in a high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The A, B data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

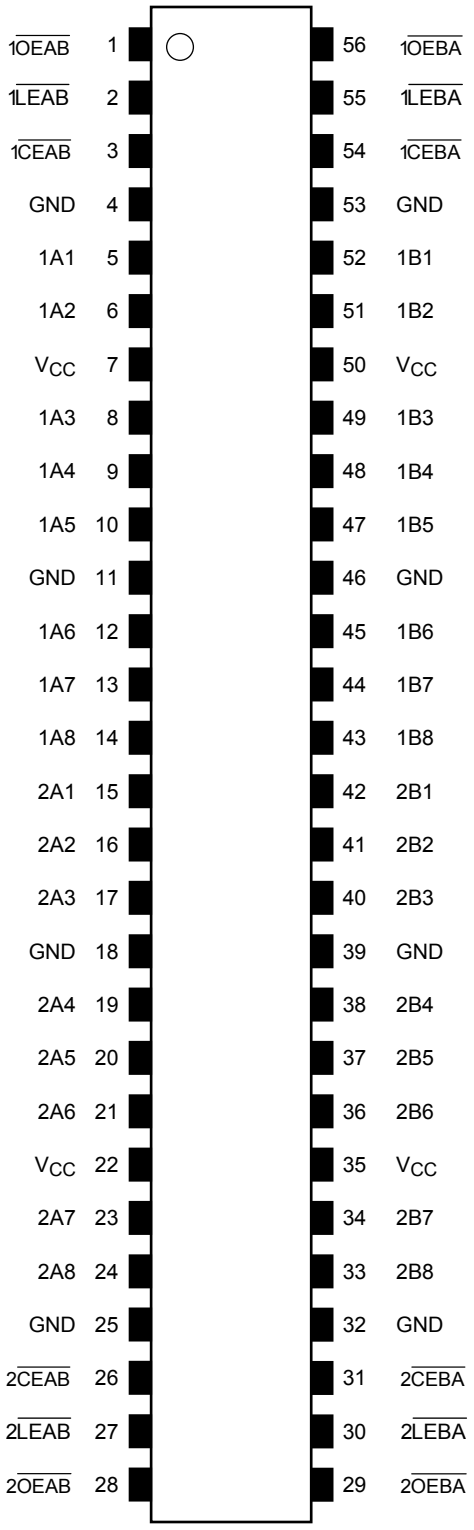
All inputs are equipped with protection circuits against static discharge.

Features (Note)

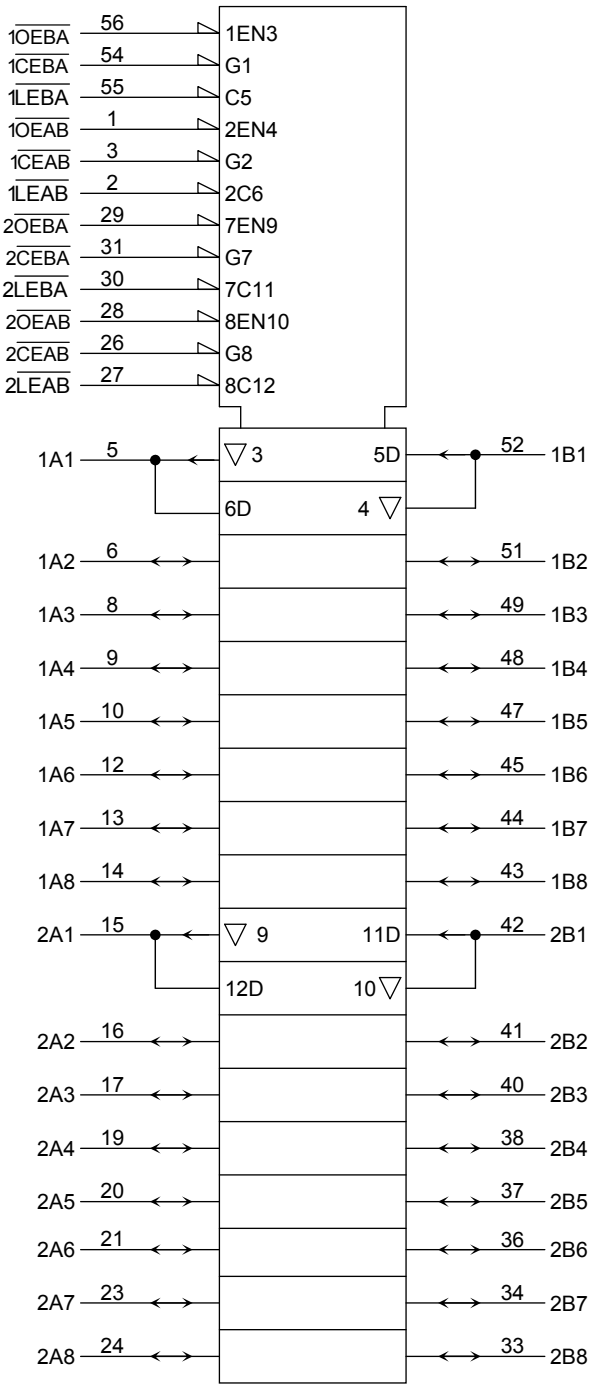
- Low-voltage operation: V_{CC} = 1.8 to 3.6 V
- Bushold on data inputs eliminating the need for external pull-up/pull-down resistors
- High-speed operation: t_{pd} = 3.5 ns (max) (V_{CC} = 3.0 to 3.6 V)
  : t_{pd} = 4.0 ns (max) (V_{CC} = 2.3 to 2.7 V)
  : t_{pd} = 8.0 ns (max) (V_{CC} = 1.8 V)
- 3.6-V tolerant control inputs
- Output current: I_{OH}/I_{OL} = ±24 mA (min) (V_{CC} = 3.0 V)
  : I_{OH}/I_{OL} = ±18 mA (min) (V_{CC} = 2.3 V)
  : I_{OH}/I_{OL} = ±6 mA (min) (V_{CC} = 1.8 V)
- Latch-up performance: −300 mA
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Package: TSSOP

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table (A bus → B bus each 8-bit latch)

Inputs				Outputs
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B0 (Note)
L	L	L	L	L
L	L	L	H	H

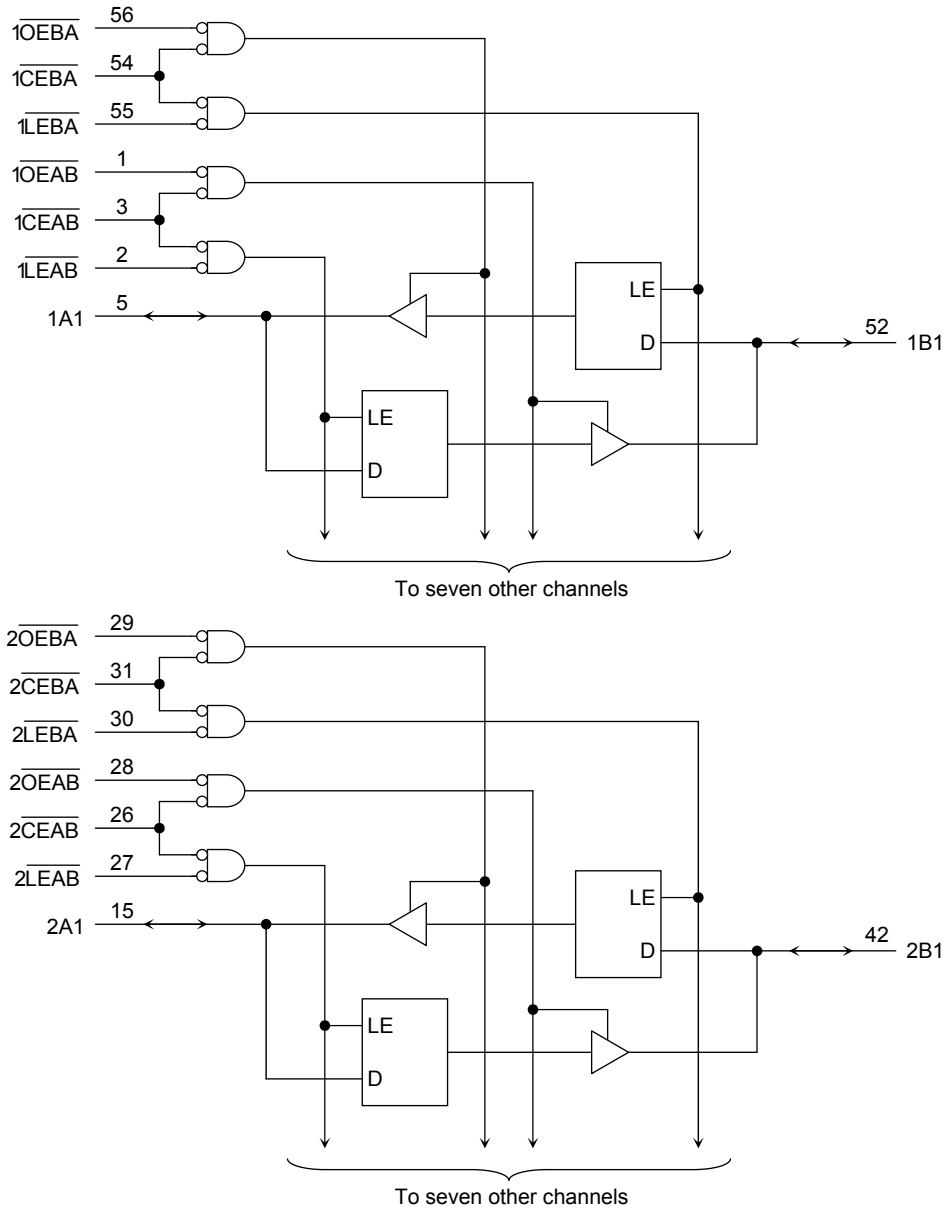
Note: Output level before the indicated steady-state input conditions were established.

Truth Table (B bus → A bus each 8-bit latch)

Inputs				Outputs
$\overline{CEBA}$	$\overline{LEBA}$	$\overline{OEBA}$	B	A
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	A0 (Note)
L	L	L	L	L
L	L	L	H	H

Note: Output level before the indicated steady-state input conditions were established.

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CC}	−0.5 to 4.6	V
DC input voltage	($\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, $\overline{LEBA}$, $\overline{CEAB}$, $\overline{CEBA}$)	V_{IN}	−0.5 to 4.6	V
	(An, Bn)		−0.5 to V_{CC} + 0.5 (Note 2)	
DC output voltage	(An, Bn)	V_{OUT}	−0.5 to V_{CC} + 0.5 (Note 3)	V
Input diode current		I_{IK}	−50	mA
Output diode current		I_{OK}	±50 (Note 4)	mA
Output current		I_{OUT}	±50	mA
Power dissipation		P_D	400	mW
DC V_{CC}/ground current per supply pin		I_{CC}/I_{GND}	±100	mA
Storage temperature		T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1) (Note 2)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CC}	1.8 to 3.6	V
			1.2 to 3.6 (Note 3)	
Input voltage	($\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, $\overline{LEBA}$, $\overline{CEAB}$, $\overline{CEBA}$)	V_{IN}	−0.3 to 3.6	V
	(An, Bn)		0 to V_{CC} (Note 4)	
Output voltage	(An, Bn)	V_{OUT}	0 to V_{CC} (Note 5)	V
Output current		I_{OH}/I_{OL}	±24 (Note 6)	mA
			±18 (Note 7)	
			±6 (Note 8)	
Operating temperature		T_{opr}	−40 to 85	°C
Input rise and fall time		dt/dv	0 to 10 (Note 9)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Note 2: Floating or unused control inputs must be held high or low.

Note 3: Data retention only

Note 4: OFF state

Note 5: High or low state

Note 6: V_{CC} = 3.0 to 3.6 V

Note 7: V_{CC} = 2.3 to 2.7 V

Note 8: V_{CC} = 1.8 V

Note 9: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = −40 to 85°C, 2.7 V < V_{CC} ≦ 3.6 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V_{IL}	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.7 to 3.6	V_{CC} − 0.2	—	V
				I_{OH} = −12 mA	2.7	2.2	—	
				I_{OH} = −18 mA	3.0	2.4	—	
				I_{OH} = −24 mA	3.0	2.2	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7 to 3.6	—	0.2	
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 18 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
Input leakage current ($\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, LEBA , CEAB , CEBA)		I_{IN}	V_{IN} = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA
Bushold input minimum drive hold current		$I_{I\ (HOLD)}$	V_{IN} = 0.8 V		3.0	75	—	μA
			V_{IN} = 2.0 V		3.0	−75	—	
Bushold input over-drive current to change state		$I_{I\ (OD)}$	(Note 1)		3.6	—	450	μA
			(Note 2)		3.6	—	−450	
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		2.7 to 3.6	—	±10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.7 to 3.6	—	20.0	μA
Increase in I_{CC} per input		ΔI_{CC}	V_{IH} = V_{CC} − 0.6 V		2.7 to 3.6	—	750	μA

Note 1: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 2: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

DC Characteristics (Ta = −40 to 85°C, 2.3 V ≦ V_{CC} ≦ 2.7 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		2.3 to 2.7	1.6	—	V
	L-level	V_{IL}	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	2.3 to 2.7	V_{CC} − 0.2	—	V
				I_{OH} = −6 mA	2.3	2.0	—	
				I_{OH} = −12 mA	2.3	1.8	—	
				I_{OH} = −18 mA	2.3	1.7	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.3 to 2.7	—	0.2	
				I_{OL} = 12 mA	2.3	—	0.4	
				I_{OL} = 18 mA	2.3	—	0.6	
Input leakage current ($\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, $\overline{LEBA}$, $\overline{CEAB}$, $\overline{CEBA}$)		I_{IN}	V_{IN} = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA
Bushold input minimum drive hold current		$I_{I\ (HOLD)}$	V_{IN} = 0.7 V		2.3	45	—	μA
			V_{IN} = 1.6 V		2.3	−45	—	
Bushold input over-drive current to change state		$I_{I\ (OD)}$	(Note 1)		2.7	—	300	μA
			(Note 2)		2.7	—	−300	
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		2.3 to 2.7	—	±10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.3 to 2.7	—	20.0	μA

Note 1: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 2: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

DC Characteristics (Ta = −40 to 85°C, 1.8 V ≦ V_{CC} < 2.3 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		1.8 to 2.3	0.7 × V_{CC}	—	V
	L-level	V_{IL}	—		1.8 to 2.3	—	0.2 × V_{CC}	
Output voltage	H-level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA	1.8	V_{CC} − 0.2	—	V
				I_{OH} = −6 mA	1.8	1.4	—	
	L-level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.8	—	0.2	
				I_{OL} = 6 mA	1.8	—	0.3	
Input leakage current ($\overline{OEAB}$, $\overline{OEBA}$, $\overline{LEAB}$, $\overline{LEBA}$, $\overline{CEAB}$, $\overline{CEBA}$)		I_{IN}	V_{IN} = 0 to 3.6 V		1.8	—	±5.0	μA
Bushold input minimum drive hold current		$I_{I\ (HOLD)}$	V_{IN} = 0.36 V		1.8	25	—	μA
			V_{IN} = 1.26 V		1.8	−25	—	
Bushold input over-drive current to change state		$I_{I\ (OD)}$	(Note 1)		1.8	—	200	μA
			(Note 2)		1.8	—	−200	
3-state output OFF state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		1.8	—	±10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		1.8	—	20.0	μA

Note 1: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 2: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

AC Characteristics (Ta = –40 to 85°C, input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500\ \Omega$) (Note 1)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay time (An, Bn-Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.8	1.5	8.0	ns
			2.5 ± 0.2	0.8	4.0	
			3.3 ± 0.3	0.6	3.5	
Propagation delay time ($\overline{LEAB}$, $\overline{LEBA}$-Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.0	
			3.3 ± 0.3	0.6	3.9	
3-state output enable time ($\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$)	t_{pZL} t_{pZH}	Figure 1, Figure 4	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	3.8	
3-state output disable time ($\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$)	t_{pLZ} t_{pHZ}	Figure 1, Figure 4	1.8	1.5	7.6	ns
			2.5 ± 0.2	0.8	4.2	
			3.3 ± 0.3	0.6	3.7	
Minimum pulse width ($\overline{LEAB}$, $\overline{LEBA}$, $\overline{CEAB}$, $\overline{CEBA}$)	$t_{W\ (L)}$	Figure 1, Figure 2, Figure 3	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum setup time (An, Bn-$\overline{LE}$, $\overline{CE}$)	t_s	Figure 1, Figure 2, Figure 3	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time (An, Bn-$\overline{LE}$, $\overline{CE}$)	t_h	Figure 1, Figure 2, Figure 3	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 2)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

Note 2: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics

(Ta = 25°C, input: $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500\ \Omega$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note)	1.8	0.25	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note)	2.5	0.6	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note)	3.3	0.8	
Quiet output minimum dynamic V_{OL}	V_{OLV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note)	1.8	−0.25	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note)	2.5	−0.6	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note)	3.3	−0.8	
Quiet output minimum dynamic V_{OH}	V_{OHV}	V_{IH} = 1.8 V, V_{IL} = 0 V (Note)	1.8	1.5	V
		V_{IH} = 2.5 V, V_{IL} = 0 V (Note)	2.5	1.9	
		V_{IH} = 3.3 V, V_{IL} = 0 V (Note)	3.3	2.2	

Note: Parameter guaranteed by design.

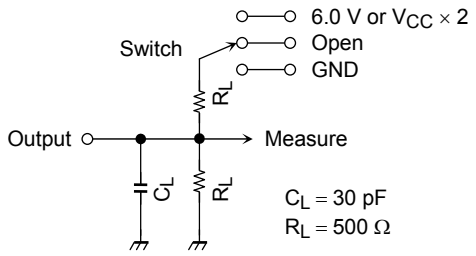
Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	1.8, 2.5, 3.3	6	pF
Bus I/O capacitance	$C_{I/O}$		1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note)	1.8, 2.5, 3.3	20	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16$ (per bit)

AC Test Circuit



Parameter	Switch	
t_{pLH}, t_{pHL}	Open	
t_{pLZ}, t_{pZL}	6.0 V $V_{CC} \times 2$	@V_{CC} = 3.3 ± 0.3 V @V_{CC} = 2.5 ± 0.2 V @V_{CC} = 1.8 V
t_{pHZ}, t_{pZH}	GND	

Figure 1

AC Waveform

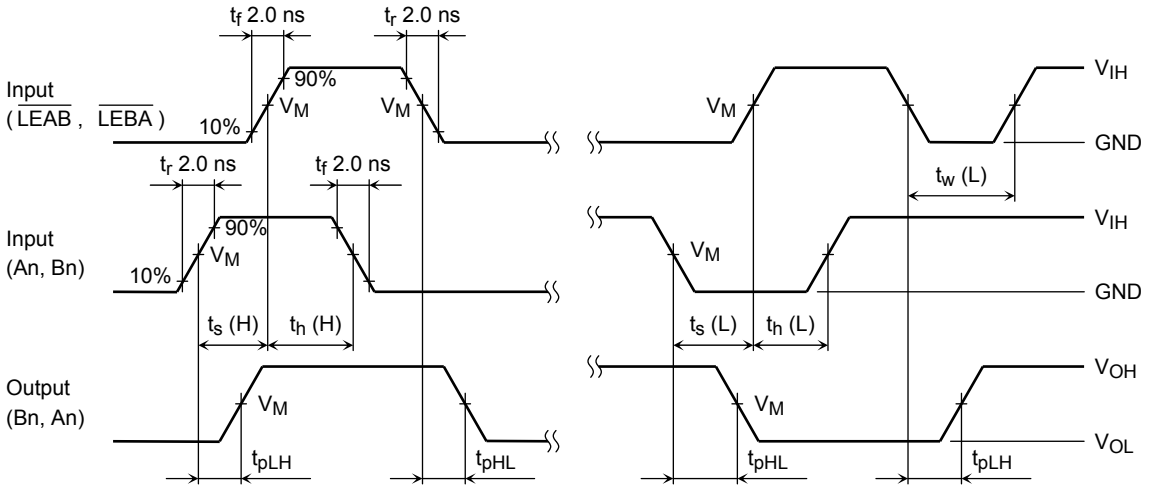


Figure 2 t_{pLH}, t_{pHL}, t_w, t_s, t_h

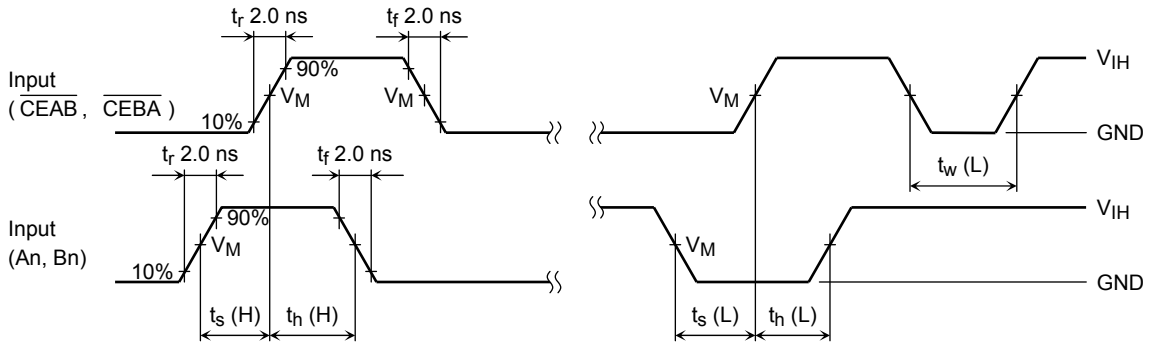


Figure 3 t_w, t_s, t_h

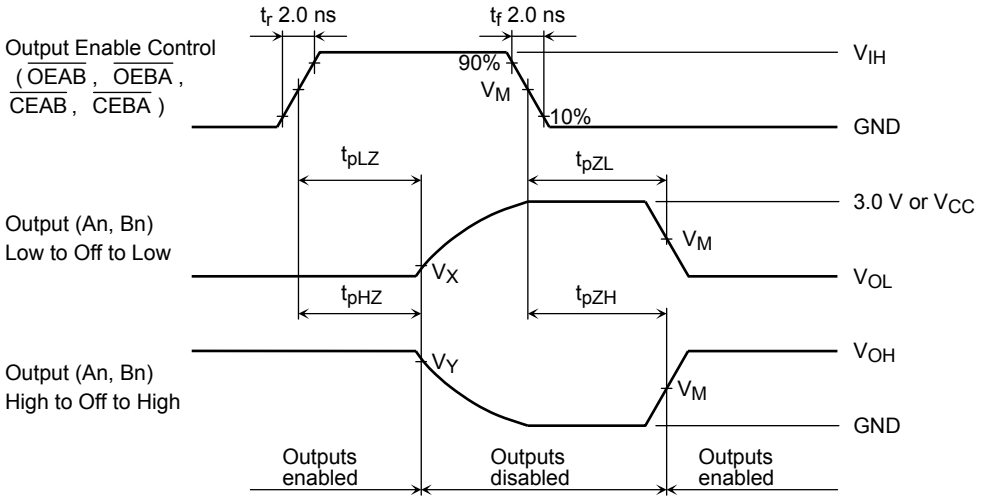
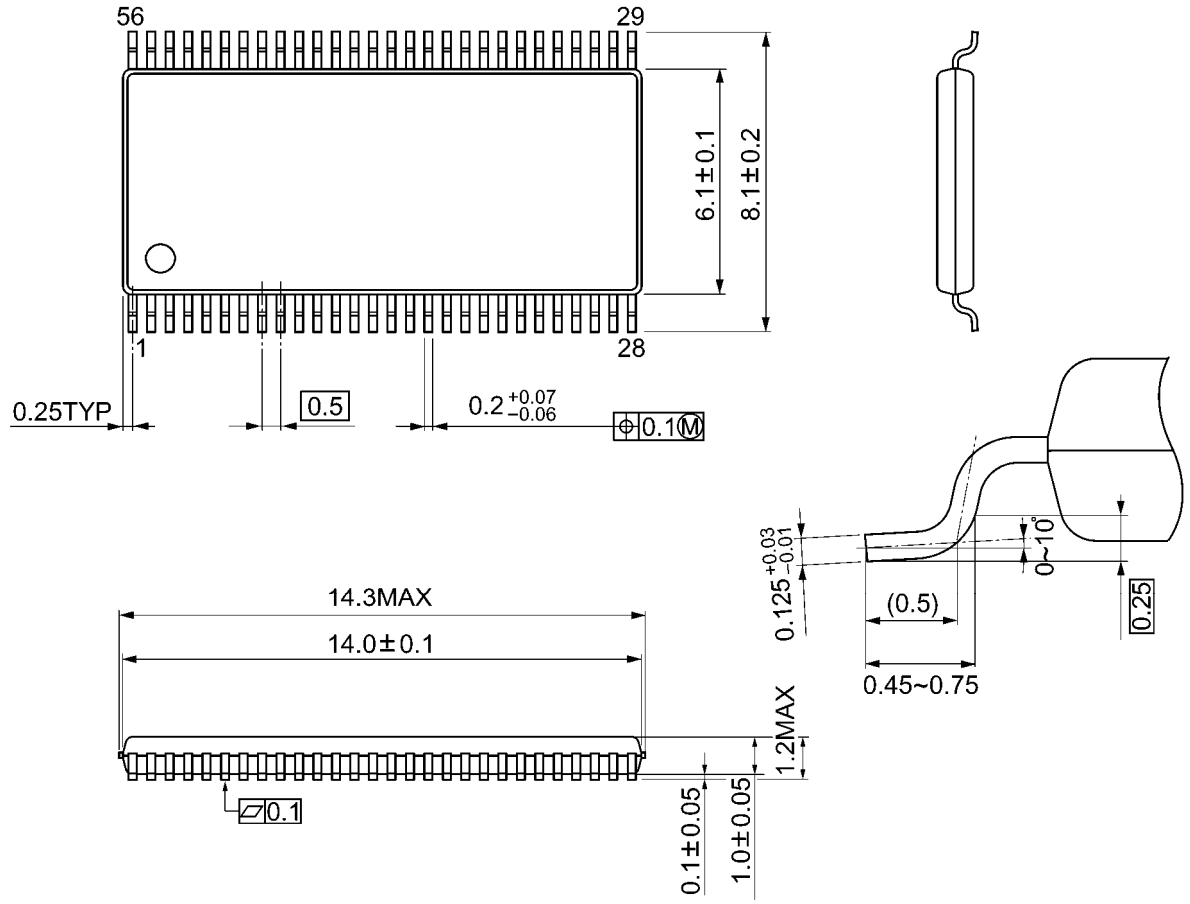


Figure 4 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V

Package Dimensions

TSSOP56-P-0061-0.50A Unit: mm



Weight: 0.25 g (typ.)

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