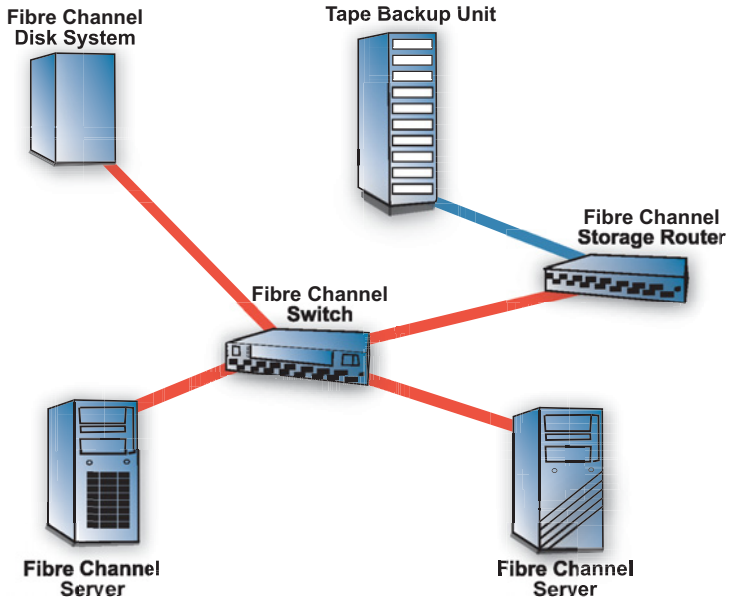
Silicon Image's SiI 2024 Quad serializer/deserializer (SerDes) is capable of transmitting and receiving four independent channels of data at 1.0625 and 2.125 gigabits-per-second (Gbps). Targeted at Fibre Channel applications, the SiI 2024 Quad SerDes is designed for power, performance and price. Making use of a robust CMOS design that significantly reduces power dissipation and jitter, the SiI 2024 provides a low-cost solution for applications that require multiple-channel, high-performance Fibre Channel SerDes. By offering four integrated, low-power SerDes in one package, the SiI 2024 reduces board space and power requirements traditionally needed for Fibre Channel SerDes.

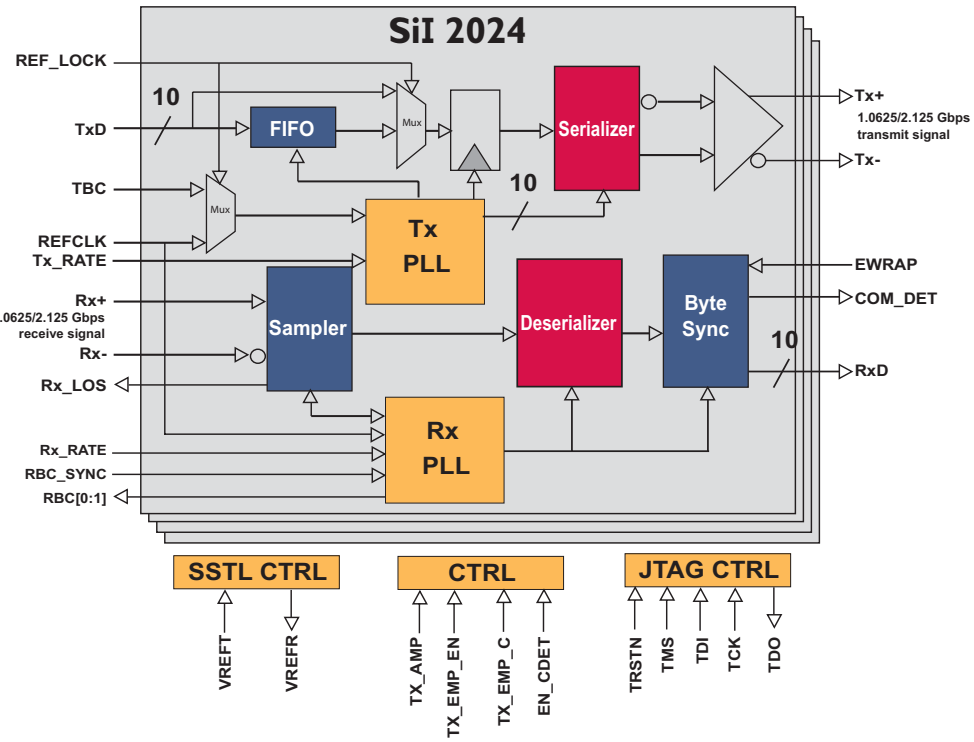
On a per-channel basis, the SiI 2024 supports selectable transmit and receive data rates for automatic speed negotiation. It also utilizes 10-bit SSTL_2-compatible interfaces for each channel's parallel data input/output. For added flexibility in some system applications, the SiI 2024 offers pre-emphasis and voltage swing control on the serial transmit ports. The SiI 2024 is available in a 324-pin, 23x23mm PBGA package and supports JTAG for improved testability.

The SiI 2024 SerDes leverages much of the circuit innovation at the physical layer of Silicon Image's proprietary, reduced overhead Multi-layer Serial Link (MSL™) architecture, pioneered and proven through the company's market-leading PanelLink® and SATALink™ products. MSL technology is a multi-layer approach to providing robust, cost-effective, multi-gigabit semiconductor solutions on a single chip for high-bandwidth applications.



Fibre Channel Applications

- Hubs and Switches
- RAID Systems
- High-Speed Backplanes



SiI 2024 Features

Fibre Channel SerDes

General

- Fibre Channel-compliant
- Multi-rate: 1.0625 Gbps and 2.125 Gbps
- Four independent channels
- Advanced-power supply filtering

Low Power

- Single 1.8V supply for core circuits and 2.5V supply for parallel I/O
- Power dissipation: 250 mW per channel

Cost Effective

- Standard CMOS technology
- Plastic 324-pin PBGA

Parallel I/O Interface

- 10-bit interface with DDR for 2.125 Gbps mode
- Flexibility of using reference clock (REFCLK) instead of transmit byte clocks (TBC) in “noisy” environments
- Separate TBC for latching parallel input data
- SSTL_2 and High-Speed Parallel Interface (HSPI)-compliant

Part Number - SiI2024CB324

Highly Reliable Serial Interface

- Individually selectable Tx and Rx data rates per channel
- Selectable pre-emphasis control
- Selectable Tx swing control
- Low-transmit jitter design
- On-chip termination resistor

Proven Technology

- MSL™-based technology proven with PanelLink® ICs for the PC and CE markets (2-5 Gbps, over 30M units shipped)
- Robust design for "noisy" environments

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