

RELIABILITY REPORT  
FOR  
**MAX1887EEE**  
PLASTIC ENCAPSULATED DEVICES

March 6, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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## Conclusion

The MAX1887 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

### A. General

The MAX1887 step-down slave controller is intended for low-voltage, high-current, multiphase DC-to-DC applications. The MAX1887 slave controller can be combined with any of Maxim's Quick-PWM™ step-down controllers to form a multiphase DC-to-DC converter. Existing Quick-PWM controllers, such as the MAX1718, function as the master controller, providing accurate output voltage regulation, fast transient response, and fault protection features. Synchronized to the master's low-side gate driver, the MAX1887 includes the Quick-PWM constant on-time controller, gate drivers for a synchronous rectifier, active current balancing, and precision current-limit circuitry.

The MAX1887 provides the same high efficiency, ultra-low duty factor capability, and excellent transient response as other Quick-PWM controllers. The MAX1887 differentially senses the inductor currents of both the master and the slave across current-sense resistors. These differential inputs and the adjustable current-limit threshold derived from an external reference allow the slave controller to accurately balance the inductor currents and provide precise current-limit protection. The MAX1887's dual-purpose current-limit input also allows the slave controller to automatically enter a low-power standby mode when the master controller shuts down.

The MAX1887 triggers on the rising edge of the master's low-side gate driver, which staggers the on-times of both master and slave, providing out-of-phase operation that can reduce the input ripple current and consequently the number of input capacitors.

### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
V+ to GND	-0.3V to +30V
VCC, VDD to GND	-0.3V to +6V
PGND to GND	±0.3V
TRIG, LIMIT to GND	-0.3V to +6V
ILIM, CM+, CM-, CS+, CS-, COMP to GND	-0.3V to (VCC + 0.3V)
DL to PGND	-0.3V to (VDD + 0.3V)
BST to GND	-0.3V to +36V
DH to LX	-0.3V to (VBST + 0.3V)
LX to BST	-6V to +0.3V
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin QSOP	667mW
Derates above +70°C	
10-Pin uMAX	8.3mW/°C

## II. Manufacturing Information

A. Description/Function:	Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies
B. Process:	S12 – Silicon Gate 1.2 micron CMOS
C. Number of Device Transistors:	1422
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Malaysia, Thailand or Philippines
F. Date of Initial Production:	October, 2001

## III. Packaging Information

A. Package Type:	<b>16-Lead QSOP</b>
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Bonding Diagram	05-3801-0006
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

## IV. Die Information

A. Dimensions:	86 x 91 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲  
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.57 \times 10^{-9} \quad \lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5881) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The PD13 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX1887EEE**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

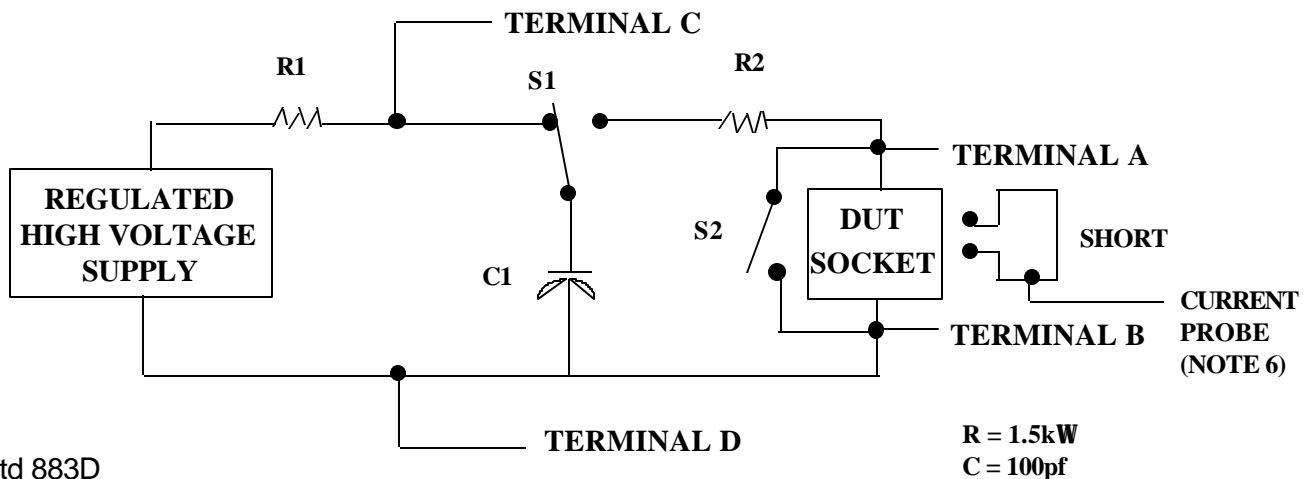
2/ No connects are not to be tested.

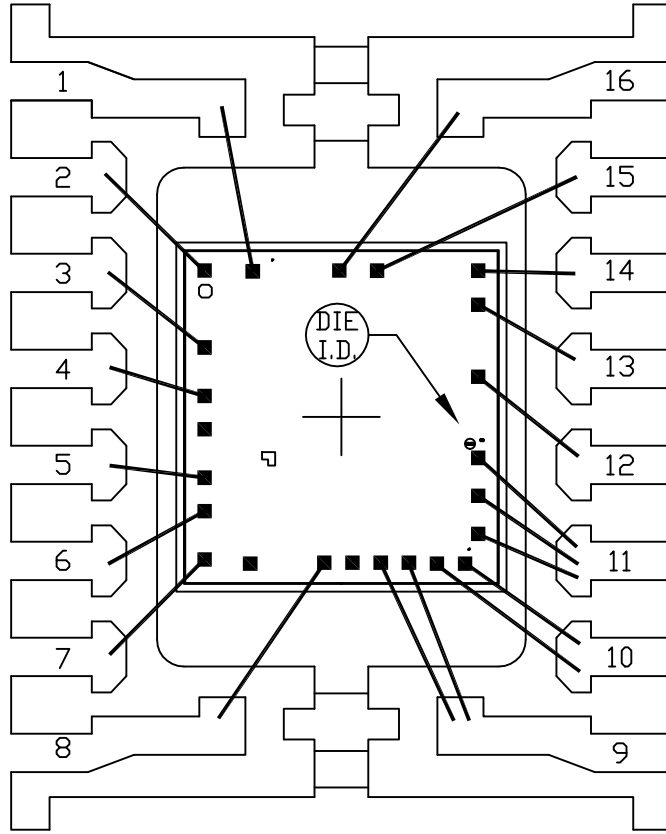
3/ Repeat pin combination 1 for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

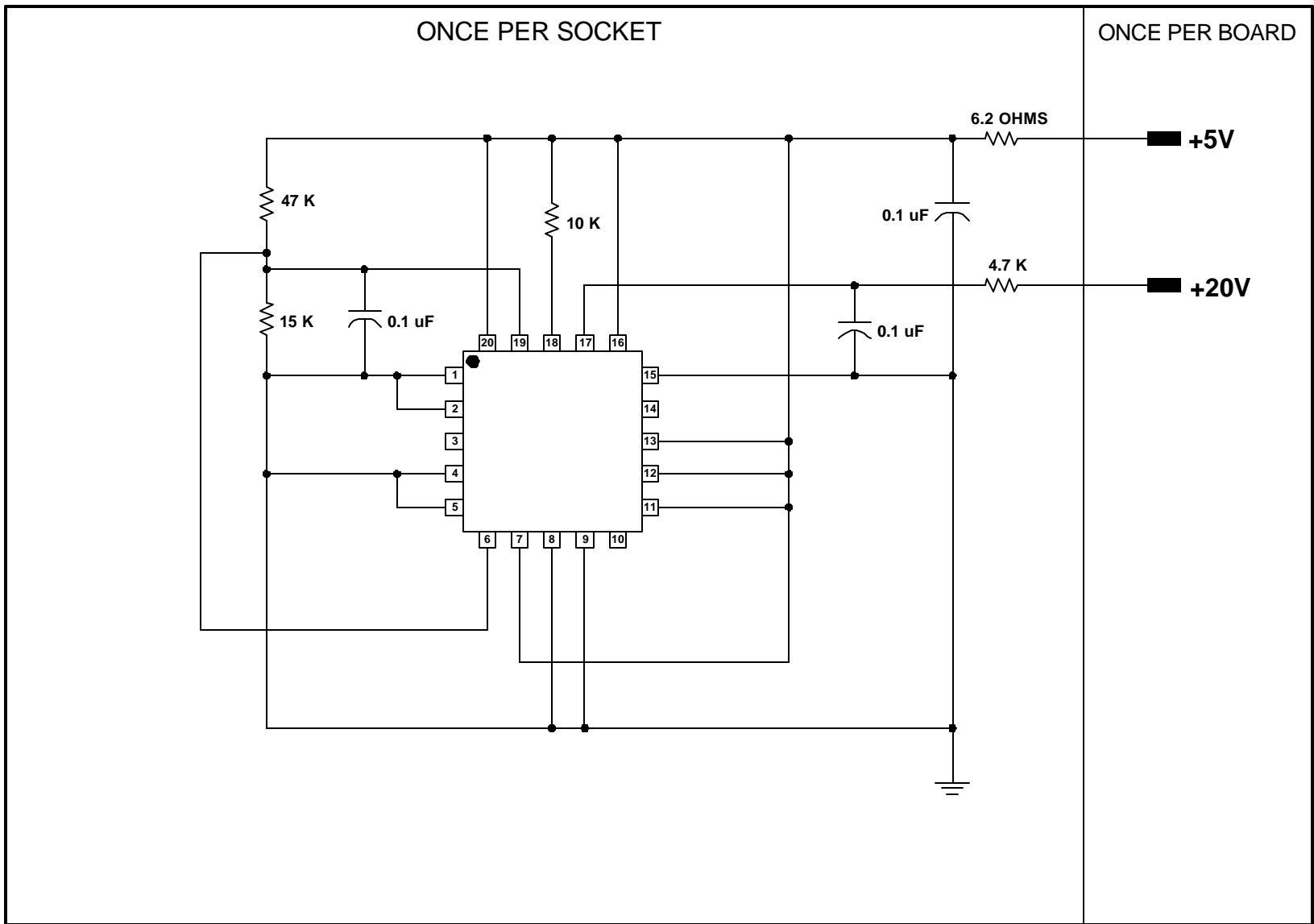
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG. CODE: E16-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X130	PKG. DESIGN			BOND DIAGRAM #: 05-3801-0006	REV: B



**DEVICES: MAX 1897**  
**PACKAGE: 20-QFN**  
**MAX. EXPECTED CURRENT = 2mA (+5V), 0.1mA (+20V)**

**DRAWN BY: TEK TAN**  
**NOTES:**