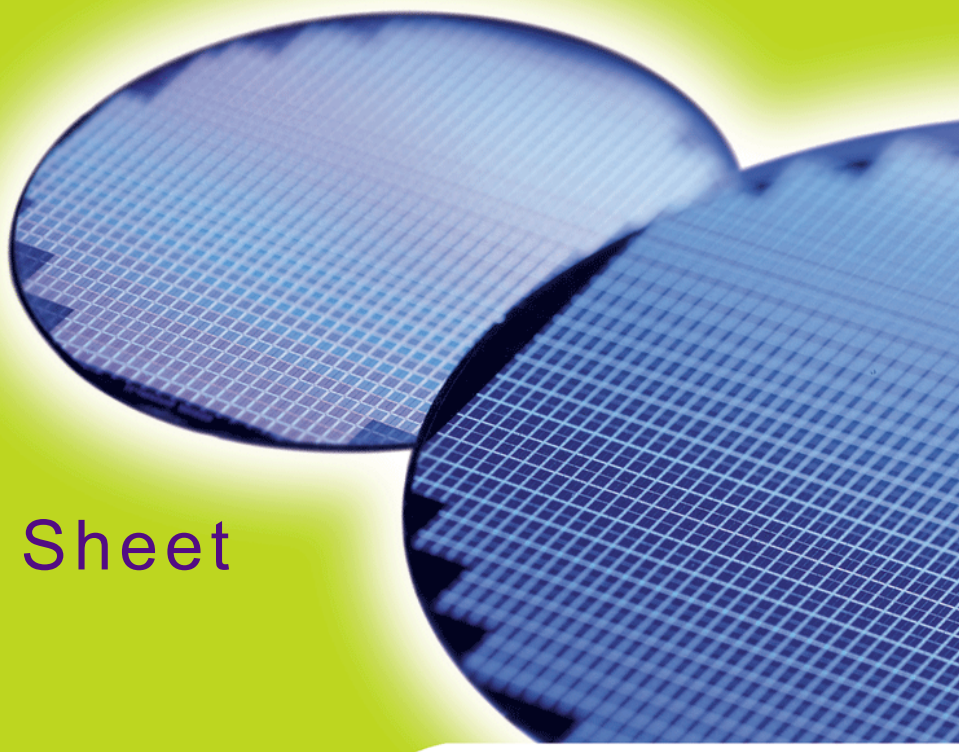
December 2006

HYS72T512341HHP–[3.7/5]–B
HYS72T512341HJP–[3.7/5]–B
HYS72T512341HKP–[3.7/5]–B

240-Pin Registered DDR2 SDRAM Modules
DDR2 SDRAM
RoHs Compliant Products



Internet Data Sheet

Rev. 1.0

www.qimonda.com

HYS72T512341HHP–[3.7/5]–B, HYS72T512341HJP–[3.7/5]–B, HYS72T512341HKP–[3.7/5]–B **Revision History: 2006-12, Rev. 1.0**	
Page	**Subjects (major changes since last revision)**
All	Qimonda update
All	Adapted internet edition
All	Added HYS672T512341HJP-[3.7/5]-B and HYS72T512341HKP-[3.7/5]-B modules
Chapter 4	SPD codes updated
Previous Revision: 2006-07, Rev. 0.5	

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1 Overview

This chapter gives an overview of the 1.8 V 240-Pin Registered DDR2 SDRAM Modules product family and describes its main characteristics.

1.1 Features

- 240-pin PC2–4200 and PC2–3200 DDR2 SDRAM memory modules.
- Four rank 512M ×72 module organization, and 512M ×4 chip organization
- Registered DIMM Parity bit for address and control bus
- 4 GB module built with 512 Mbit DDR2 SDRAMs in SG-A4FBGA-60 and PG-A4FBGA-60 chipsize packages.
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- Programmable CAS Latencies (3, 4, 5), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- Programmable self refresh rate via EMRS2 setting
- Programmable partial array refresh via EMRS2 settings
- DCC enabling via EMRS2 setting
- All inputs and outputs SSTL_18 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E^2PROM
- RDIMM Dimensions (nominal): 18,30 mm high, 133.35 mm wide
- All speed grades faster than DDR2–400 comply with DDR2–400 timing specifications.
- RoHS compliant products[1)]

TABLE 1
Performance Table

Product Type Speed Code			–3.7	–5	Unit
Speed Grade			**PC2–4200 4–4–4**	**PC2–3200 3–3–3**	**—**
Max. Clock Frequency	@CL5	f_{CK5}	266	200	MHz
	@CL4	f_{CK4}	266	200	MHz
	@CL3	f_{CK3}	200	200	MHz
Min. RAS-CAS-Delay		t_{RCD}	15	15	ns
Min. Row Precharge Time		t_{RP}	15	15	ns
Min. Row Active Time		t_{RAS}	45	40	ns
Min. Row Cycle Time		t_{RC}	60	55	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

The Qimonda HYS72T512341H[H/J/K]P–[3.7/5]–B module family are Very Low Profile Registered DIMM (with parity) modules with 18,3 mm height based on DDR2 technology. DIMMs are available as ECC modules in 512M ×72 (4 GB) organization and density, intended for mounting into 240-Ball connector sockets.

The memory array is designed with 512-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-ball I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

green Product

TABLE 2
Ordering Information for RoHS Compliant Products

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC2–4200			
HYS72T512341HHP–3.7–B	4 GB 4R×4 PC2–4200P–444–12–ZZ	4 Rank ECC	4 GB (×4)
HYS72T512341HJP–3.7–B	4 GB 4R×4 PC2–4200P–444–12–ZZ	4 Rank ECC	4 GB (×4)
HYS72T512341HKP–3.7–B	4 GB 4R×4 PC2–4200P–444–12–ZZ	4 Rank ECC	4 GB (×4)
PC2–3200			
HYS72T512341HHP–5–B	4 GB 4R×4 PC2–3200P–333–12–ZZ	4 Rank ECC	4 GB (×4)
HYS72T512341HJP–5–B	4 GB 4R×4 PC2–3200P–333–12–ZZ	4 Rank ECC	4 GB (×4)
HYS72T512341HKP–5–B	4 GB 4R×4 PC2–3200P–333–12–ZZ	4 Rank ECC	4 GB (×4)

1) All Product Type numbers end with a place code, designating the silicon die revision. Example: HYS72T512341HJP-3.7-B, indicating Rev. “B” dies are used for DDR2 SDRAM components. For all Qimonda DDR2 module and component nomenclature see **Chapter 6** of this data sheet.

2) The Compliance Code is printed on the module label and describes the speed grade, for example “PC2–4200P–444–12”, where 4200P means Registered DIMM modules (Parity bit) with 4.26 GB/sec Module Bandwidth and “444-12” means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.2.

TABLE 3
Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits
4 GB	512M ×72	4	ECC	18 ×4	14/2/11

TABLE 4
Components on Modules

Product Type	DRAM Components	DRAM Density	DRAM Organisation	Note
HYS72T512341HHP	HYB18T2G401BHF	512 Mbit	512M ×4	1)
HYS72T512341HJP				
HYS72T512341HKP				

1) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2 Pin Configuration

2.1 Pin Configuration

The pin configuration of the Registered DDR2 SDRAM DIMM is listed by function in **Table 5** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1**.

TABLE 5
Pin Configuration of RDIMM

Pin No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
185	CK0	I	SSTL	**Clock Signal CK0, Complementary Clock Signal CK0**
186	$\overline{CK0}$	I	SSTL	
52	CKE0	I	SSTL	**Clock Enables 1:0**
171	CKE1	I	SSTL	*Note: 2-Ranks module*
	NC	NC	—	**Not Connected** *Note: 1-Rank module*
Control Signals				
193	$\overline{S0}$	I	SSTL	**Chip Select Rank 3:0**
76	$\overline{S1}$	I	SSTL	
220	$\overline{S2}$	I	SSTL	
221	$\overline{S3}$	I	SSTL	
192	$\overline{RAS}$	I	SSTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
74	$\overline{CAS}$	I	SSTL	
73	$\overline{WE}$	I	SSTL	
18	$\overline{RESET}$	I	CMOS	**Register Reset**
Address Signals				
71	BA0	I	SSTL	**Bank Address Bus 1:0**
190	BA1	I	SSTL	
54	BA2	I	SSTL	**Bank Address Bus 2** Greater than 512Mb DDR2 SDRAMS
	NC	I	SSTL	**Not Connected** Less than 1Gb DDR2 SDRAMS

Pin No.	Name	Pin Type	Buffer Type	Function
188	A0	I	SSTL	**Address Bus 12:0, Address Signal 10/AutoPrecharge**
183	A1	I	SSTL	
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	
70	A10	I	SSTL	
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	**Address Signal 13**
	NC	NC	—	**Not Connected** *Note: Non CA parity modules based on 256 Mbit component*
174	A14	I	SSTL	**Not Connected**
173	A15	I	SSTL	**Not Connected**
Data Signals				
3	DQ0	I/O	SSTL	**Data Bus 63:0** Data Input/Output pins
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	

Pin No.	Name	Pin Type	Buffer Type	Function
21	DQ10	I/O	SSTL	**Data Bus 63:0** Data Input/Output pins
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
152	DQ28	I/O	SSTL	
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	
159	DQ31	I/O	SSTL	
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	
206	DQ39	I/O	SSTL	**Data Bus 63:0**
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	
98	DQ48	I/O	SSTL	
99	DQ49	I/O	SSTL	

Pin No.	Name	Pin Type	Buffer Type	Function
107	DQ50	I/O	SSTL	**Data Bus 63:0**
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	
Check Bits				
42	CB0	I/O	SSTL	**Check Bits 7:0** Check Bit Input / Output pins
43	CB1	I/O	SSTL	
48	CB2	I/O	SSTL	
49	CB3	I/O	SSTL	
161	CB4	I/O	SSTL	
162	CB5	I/O	SSTL	
167	CB6	I/O	SSTL	
168	CB7	I/O	SSTL	
Data Strobe Bus				
7	DQS0	I/O	SSTL	**Data Strobes 17:0**
6	$\overline{\text{DQS0}}$	I/O	SSTL	
16	DQS1	I/O	SSTL	
15	$\overline{\text{DQS1}}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{\text{DQS2}}$	I/O	SSTL	
37	DQS3	I/O	SSTL	
36	$\overline{\text{DQS3}}$	I/O	SSTL	
84	DQS4	I/O	SSTL	
83	$\overline{\text{DQS4}}$	I/O	SSTL	
93	DQS5	I/O	SSTL	
92	$\overline{\text{DQS5}}$	I/O	SSTL	
105	DQS6	I/O	SSTL	
104	$\overline{\text{DQS6}}$	I/O	SSTL	
114	DQS7	I/O	SSTL	
113	$\overline{\text{DQS7}}$	I/O	SSTL	

Pin No.	Name	Pin Type	Buffer Type	Function
46	DQS8	I/O	SSTL	**Data Strobes 17:0**
45	$\overline{\text{DQS8}}$	I/O	SSTL	
125	DQS9	I/O	SSTL	
126	$\overline{\text{DQS9}}$	I/O	SSTL	
134	DQS10	I/O	SSTL	
135	$\overline{\text{DQS10}}$	I/O	SSTL	
146	DQS11	I/O	SSTL	
147	$\overline{\text{DQS11}}$	I/O	SSTL	
155	DQS12	I/O	SSTL	
156	$\overline{\text{DQS12}}$	I/O	SSTL	
202	DQS13	I/O	SSTL	
203	$\overline{\text{DQS13}}$	I/O	SSTL	
211	DQS14	I/O	SSTL	
212	$\overline{\text{DQS14}}$	I/O	SSTL	
223	DQS15	I/O	SSTL	
224	$\overline{\text{DQS15}}$	I/O	SSTL	
232	DQS16	I/O	SSTL	
233	$\overline{\text{DQS16}}$	I/O	SSTL	
164	DQS17	I/O	SSTL	
165	$\overline{\text{DQS17}}$	I/O	SSTL	
Data Mask				
125	DM0	I	SSTL	**Data Masks 8:0** *Note: x8 based module*
134	DM1	I	SSTL	
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	
EEPROM				
120	SCL	I	CMOS	**Serial Bus Clock**
119	SDA	I/O	OD	**Serial Bus Data**
239	SA0	I	CMOS	**Serial Address Select Bus 2:0**
240	SA1	I	CMOS	
101	SA2	I	CMOS	
Parity				
55	$\overline{\text{ERR\_OUT}}$	O	CMOS	**Parity bits**
	PAR_IN	I	CMOS	

Pin No.	Name	Pin Type	Buffer Type	Function
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage**
238	V_{DDSPD}	PWR	—	**EEPROM Power Supply**
51, 56, 62, 72, 75, 78, 170, 175,, 181, 191, 194	V_{DDQ}	PWR	—	**I/O Driver Power Supply**
53, 59, 64, 67, 69, 172, 178, 184,, 187, 189, 197	V_{DD}	PWR	—	**Power Supply**
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97, 100, 103, 106, 109, 112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	V_{SS}	GND	—	**Ground Plane**
Other Pins				
19, 55, 68, 102, 137, 138, 173	NC	NC	—	**Not connected**
195	ODT0	I	SSTL	**On-Die Termination Control 1:0**
77	ODT1	I	SSTL	*Note: 2-Ranks module*
	NC	NC	—	*Note: 1-Rank modules*

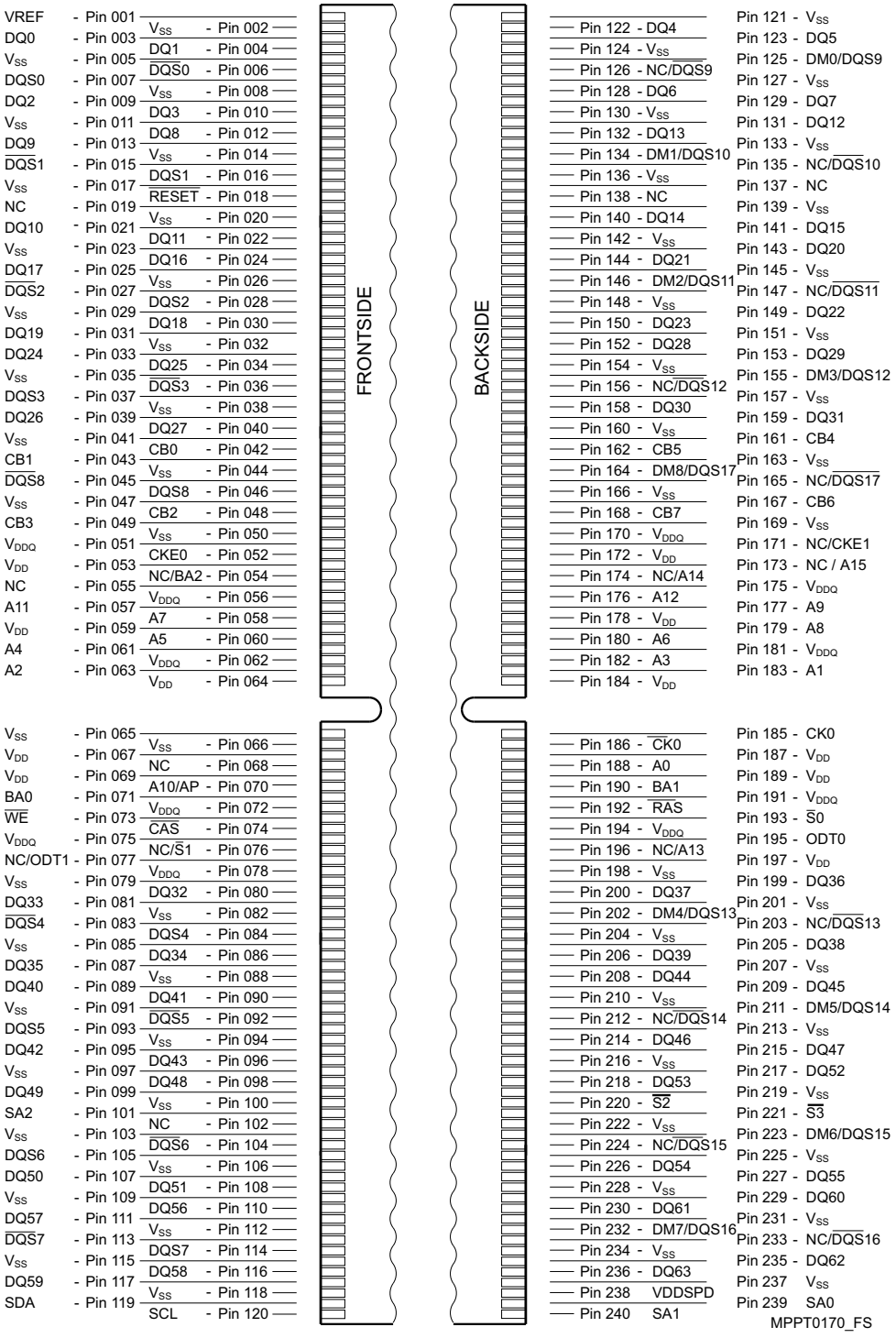
TABLE 6
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

TABLE 7
Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable
NC	Not Connected

FIGURE 1
Pin Configuration for RDIMM (240 pins)



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in **Table 8** at any time.

TABLE 8
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–1.0	+2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.5	+2.3	V	1)
T_{STG}	Storage Temperature	–55	+100	°C	1)2)

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 9
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{OPER}	Operating Temperature	0	90	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 90 °C under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 80 °C to 90 °C TCASE temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%

3.2 D.C. Characteristics

TABLE 10
Operating Conditions

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+65	°C	
DRAM Case Temperature	T_{CASE}	0	+90	°C	1)2)3)4)
Storage Temperature	T_{STG}	– 50	+100	°C	
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported
3) Above 80 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%.
5) Up to 3000 m.

TABLE 11
Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	—	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	– 5	—	5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise in V_{DDQ}.
3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

3.3 AC Characteristics

All Speed grades faster than DDR2-400B comply with DDR2-400B timing specifications(t_{CK} = 5ns with t_{RAS} = 40ns).

TABLE 12
Speed Grade Definition Speed Bins for DDR2–533C and DDR2–400B

Speed Grade			DDR2–533C		DDR2–400B		Unit	Note
QAG Sort Name			–3.7		–5			
CAS-RCD-RP latencies			4–4–4		3–3–3		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	5	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3.75	8	5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) only.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS/$\overline{DQS}$, RDQS/$\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.4 I_{DD} Specifications and Conditions

List of tables defining I_{DD} Specifications and Conditions.

TABLE 13
I_{DD} Measurement Conditions

Parameter	Symbol	Note 1)2)3)4)5)
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}	
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL_{MIN}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}	6)
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD2N}	
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}	
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}	
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$	
Operating Current - Burst Read All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CKMIN}$; $t_{RAS} = t_{RASMAX}$; $t_{RP} = t_{RPMIN}$; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; I_{OUT} = 0mA.	I_{DD4R}	6)
Operating Current - Burst Write All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}	
Burst Refresh Current $t_{CK} = t_{CK.MIN}$., Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}	

Parameter	Symbol	Note 1)2)3)4)5)
Distributed Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}	
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}	
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}	6)

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD} see **Table 14**
4) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
5) For details and notes see the relevant Qimonda component data sheet
6) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

TABLE 14
Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	Inputs are stable at a HIGH or LOW level
FLOATING	Inputs are $V_{REF} = V_{DDQ}/2$
SWITCHING	Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes

TABLE 15

I_{DD} Specification for HYS72T512341H[HJ/K]P–[3.7/5]–B

Product Type	HYS72T512341H[H/J/K]P–3.7–B	HYS72T512341H[HJ/K]P–5–B	Unit	Note[1]
Organization	4 GB	4 GB		
	4 Ranks	4 Ranks		
	×72	×72		
	–3.7	–5		
Symbol	Max.	Max.		
I_{DD0}	2780	2450	mA	2)
I_{DD1}	2960	2610	mA	2)
I_{DD2N}	3970	3420	mA	3)
I_{DD2P}	1730	1480	mA	3)
I_{DD2Q}	3750	3280	mA	3)
I_{DD3N}	4330	3780	mA	3)
$I_{DD3P(MRS=0)}$	3250	2700	mA	3)4)
$I_{DD3P(MRS=1)}$	1880	1620	mA	3)5)
I_{DD4R}	3590	3060	mA	2)
I_{DD4W}	3590	3060	mA	2)
I_{DD5B}	3950	3600	mA	2)
I_{DD5D}	1880	1620	mA	3)6)
I_{DD6}	360	504	mA	3)6)
I_{DD7}	4220	3890	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R}, and I_{DD7}, are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Current mode
3) Both ranks are in the same I_{DD}current mode
4) Fast: MRS(12)=0
5) Slow: MRS(12)=1
6) I_{DD5D} and I_{DD6} values are for 0°C ≤ T_{Case} ≤ 85°C

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

TABLE 16
SPD Codes for PC2-4200P-444

Product Type		HYS72T512341HHP–3.7–B	HYS72T512341HJP–3.7–B	HYS72T512341HKP–3.7–B
Organization		4 GByte	4 GByte	4 GByte
		×72	×72	×72
		4 Ranks (×4)	4 Ranks (×4)	4 Ranks (×4)
Label Code		PC2–4200P–444	PC2–4200P–444	PC2–4200P–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0E	0E	0E
4	Number of Column Addresses	0B	0B	0B
5	DIMM Rank and Stacking Information	03	03	03
6	Data Width	48	48	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	3D	3D	3D
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	50	50	50
11	Error Correction Support (non-ECC, ECC)	06	06	06
12	Refresh Rate and Type	81	81	81
13	Primary SDRAM Width	04	04	04

Product Type		HYS72T512341HHP–3.7–B	HYS72T512341HJP–3.7–B	HYS72T512341HKP–3.7–B
Organization		4 GByte	4 GByte	4 GByte
		×72	×72	×72
		4 Ranks (×4)	4 Ranks (×4)	4 Ranks (×4)
Label Code		PC2–4200P–444	PC2–4200P–444	PC2–4200P–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
14	Error Checking SDRAM Width	04	04	04
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	01	01	01
21	DIMM Attributes	05	05	05
22	Component Attributes	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D
31	Module Density per Rank	01	01	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37	37
34	$t_{DS.MIN}$ [ns]	10	10	10
35	$t_{DH.MIN}$ [ns]	22	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00

Product Type		**HYS72T512341HHP–3.7–B**	**HYS72T512341HJP–3.7–B**	**HYS72T512341HKP–3.7–B**
Organization		**4 GByte**	**4 GByte**	**4 GByte**
		×72	**×72**	**×72**
		4 Ranks (×4)	**4 Ranks (×4)**	**4 Ranks (×4)**
Label Code		**PC2–4200P–444**	**PC2–4200P–444**	**PC2–4200P–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	1E	1E
45	$t_{QHS.MAX}$ [ns]	28	28	28
46	PLL Relock Time	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	50	50	50
48	Psi(T-A) DRAM	7A	7A	7A
49	ΔT_0 (DT0)	43	43	43
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	29	29	29
51	ΔT_{2P} (DT2P)	36	36	36
52	ΔT_{3N} (DT3N)	21	21	21
53	$\Delta T_{3P.fast}$ (DT3P fast)	41	41	41
54	$\Delta T_{3P.slow}$ (DT3P slow)	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	40	40	40
56	ΔT_{5B} (DT5B)	1E	1E	1E
57	ΔT_7 (DT7)	22	22	22
58	Psi(ca) PLL	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	61	61	61
61	ΔT_{REG} (DTREG) / Toggle Rate	78	78	78
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	9F	9F	9F
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F

Product Type		HYS72T512341HHP–3.7–B	HYS72T512341HJP–3.7–B	HYS72T512341HKP–3.7–B
Organization		4 GByte	4 GByte	4 GByte
		×72	×72	×72
		4 Ranks (×4)	4 Ranks (×4)	4 Ranks (×4)
Label Code		PC2–4200P–444	PC2–4200P–444	PC2–4200P–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	37	37	37
74	Product Type, Char 2	32	32	32
75	Product Type, Char 3	54	54	54
76	Product Type, Char 4	35	35	35
77	Product Type, Char 5	31	31	31
78	Product Type, Char 6	32	32	32
79	Product Type, Char 7	33	33	33
80	Product Type, Char 8	34	34	34
81	Product Type, Char 9	31	31	31
82	Product Type, Char 10	48	48	48
83	Product Type, Char 11	48	4A	4B
84	Product Type, Char 12	50	50	50
85	Product Type, Char 13	33	33	33
86	Product Type, Char 14	2E	2E	2E
87	Product Type, Char 15	37	37	37
88	Product Type, Char 16	42	42	42
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	2x	0x	0x

Product Type		**HYS72T512341HHP–3.7–B**	**HYS72T512341HJP–3.7–B**	**HYS72T512341HKP–3.7–B**
Organization		**4 GByte**	**4 GByte**	**4 GByte**
		×72	**×72**	**×72**
		4 Ranks (×4)	**4 Ranks (×4)**	**4 Ranks (×4)**
Label Code		**PC2–4200P–444**	**PC2–4200P–444**	**PC2–4200P–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

TABLE 17
SPD Codes for PC2-3200P-333

Product Type		HYS72T512341HHP–5–B	HYS72T512341HJP–5–B	HYS72T512341HKP–5–B
Organization		4 GByte	4 GByte	4 GByte
		×72	×72	×72
		4 Ranks (×4)	4 Ranks (×4)	4 Ranks (×4)
Label Code		PC2–3200P–333	PC2–3200P–333	PC2–3200P–333
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80
1	Total number of Bytes in EEPROM	08	08	08
2	Memory Type (DDR2)	08	08	08
3	Number of Row Addresses	0E	0E	0E
4	Number of Column Addresses	0B	0B	0B
5	DIMM Rank and Stacking Information	03	03	03
6	Data Width	48	48	48
7	Not used	00	00	00
8	Interface Voltage Level	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	50	50	50
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	60	60	60
11	Error Correction Support (non-ECC, ECC)	06	06	06
12	Refresh Rate and Type	81	81	81
13	Primary SDRAM Width	04	04	04
14	Error Checking SDRAM Width	04	04	04
15	Not used	00	00	00
16	Burst Length Supported	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04
18	Supported CAS Latencies	38	38	38
19	DIMM Mechanical Characteristics	01	01	01
20	DIMM Type Information	01	01	01
21	DIMM Attributes	05	05	05
22	Component Attributes	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	50	50	50

Product Type		HYS72T512341HHP–5–B	HYS72T512341HJP–5–B	HYS72T512341HKP–5–B
Organization		4 GByte	4 GByte	4 GByte
		×72	×72	×72
		4 Ranks (×4)	4 Ranks (×4)	4 Ranks (×4)
Label Code		PC2–3200P–333	PC2–3200P–333	PC2–3200P–333
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	60	60	60
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	28	28	28
31	Module Density per Rank	01	01	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	35	35	35
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	47	47	47
34	$t_{DS.MIN}$ [ns]	15	15	15
35	$t_{DH.MIN}$ [ns]	27	27	27
36	$t_{WR.MIN}$ [ns]	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	28	28	28
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E
39	Analysis Characteristics	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00
41	$t_{RC.MIN}$ [ns]	37	37	37
42	$t_{RFC.MIN}$ [ns]	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	23	23	23
45	$t_{QHS.MAX}$ [ns]	2D	2D	2D
46	PLL Relock Time	0F	0F	0F
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	50	50	50
48	Psi(T-A) DRAM	7A	7A	7A
49	ΔT_0 (DT0)	3B	3B	3B

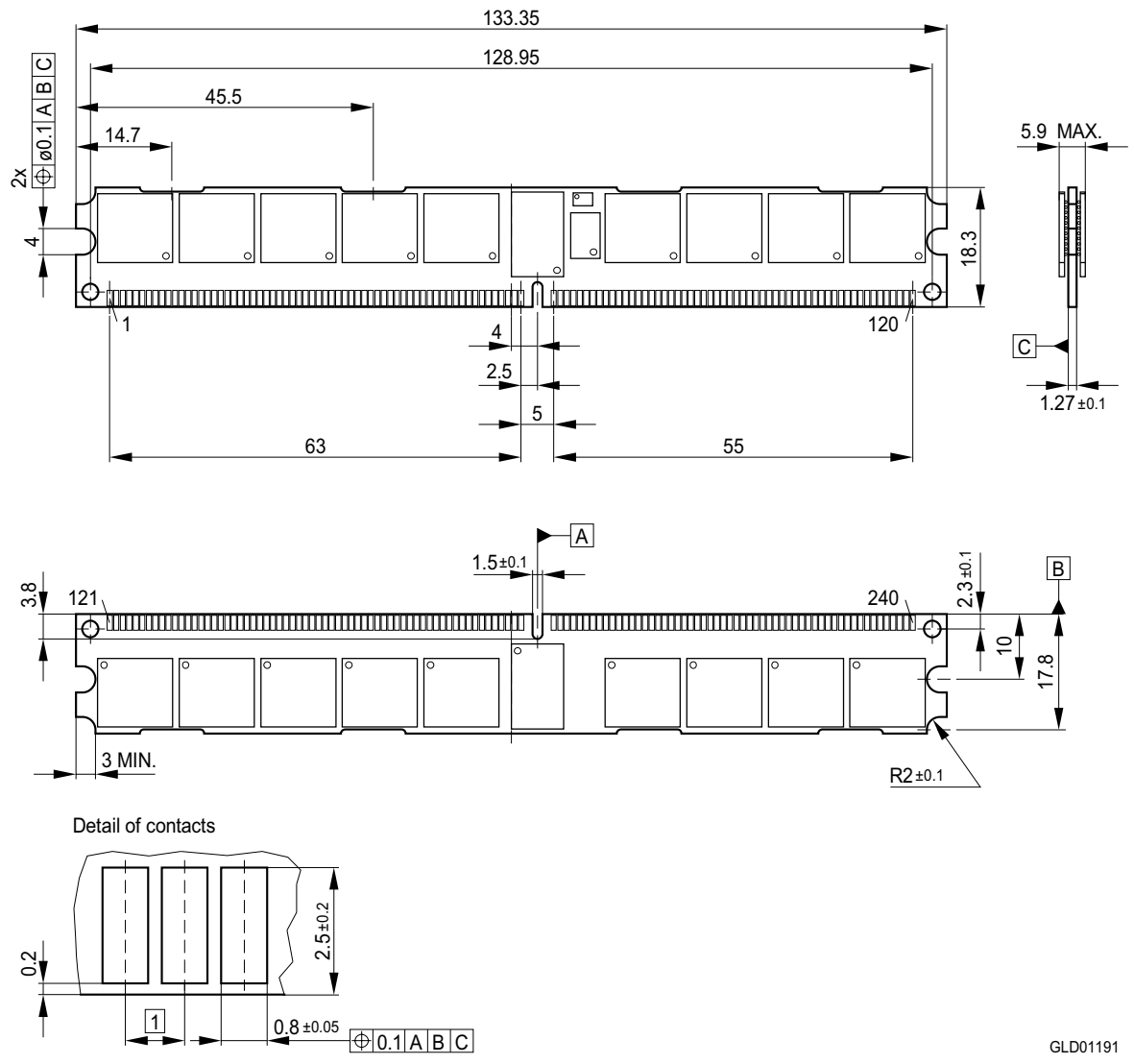
Product Type		HYS72T512341HHP–5–B	HYS72T512341HJP–5–B	HYS72T512341HKP–5–B
Organization		4 GByte	4 GByte	4 GByte
		×72	×72	×72
		4 Ranks (×4)	4 Ranks (×4)	4 Ranks (×4)
Label Code		PC2–3200P–333	PC2–3200P–333	PC2–3200P–333
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	25	25	25
51	ΔT_{2P} (DT2P)	36	36	36
52	ΔT_{3N} (DT3N)	1E	1E	1E
53	$\Delta T_{3P.fast}$ (DT3P fast)	38	38	38
54	$\Delta T_{3P.slow}$ (DT3P slow)	2A	2A	2A
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	38	38	38
56	ΔT_{5B} (DT5B)	1D	1D	1D
57	ΔT_{7} (DT7)	21	21	21
58	Psi(ca) PLL	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C
60	ΔT_{PLL} (DTPLL)	59	59	59
61	ΔT_{REG} (DTREG) / Toggle Rate	5C	5C	5C
62	SPD Revision	12	12	12
63	Checksum of Bytes 0-62	D3	D3	D3
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51
70	Manufacturer’s JEDEC ID Code (7)	00	00	00
71	Manufacturer’s JEDEC ID Code (8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Product Type, Char 1	37	37	37
74	Product Type, Char 2	32	32	32
75	Product Type, Char 3	54	54	54

Product Type		**HYS72T512341HHP–5–B**	**HYS72T512341HJP–5–B**	**HYS72T512341HKP–5–B**
Organization		**4 GByte**	**4 GByte**	**4 GByte**
		×72	**×72**	**×72**
		4 Ranks (×4)	**4 Ranks (×4)**	**4 Ranks (×4)**
Label Code		**PC2–3200P–333**	**PC2–3200P–333**	**PC2–3200P–333**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
76	Product Type, Char 4	35	35	35
77	Product Type, Char 5	31	31	31
78	Product Type, Char 6	32	32	32
79	Product Type, Char 7	33	33	33
80	Product Type, Char 8	34	34	34
81	Product Type, Char 9	31	31	31
82	Product Type, Char 10	48	48	48
83	Product Type, Char 11	48	4A	4B
84	Product Type, Char 12	50	50	50
85	Product Type, Char 13	35	35	35
86	Product Type, Char 14	42	42	42
87	Product Type, Char 15	20	20	20
88	Product Type, Char 16	20	20	20
89	Product Type, Char 17	20	20	20
90	Product Type, Char 18	20	20	20
91	Module Revision Code	2x	0x	0x
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx
99 - 127	Not used	00	00	00
128 - 255	Blank for customer use	FF	FF	FF

5 Package Outlines

In this chapter the Package Outline L-DIM-240-55 is included.

FIGURE 2
Package Outline L-DIM-240-55



Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*
4. *Heat sink is not included in the drawing. Additional width might be required.*

6 Product Type Nomenclature

Qimonda's nomenclature uses simple coding combined with some propriatory coding. **Table 18** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 19** and for components in **Table 20**.

TABLE 18
Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	64/128	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512/1G	16		0	A	C	–5	

TABLE 19
DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	Qimonda Module Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
		F	**F**ully Buffered

Field	Description	Values	Coding
10	Speed Grade	–2.5F	PC2–6400 5–5–5
		–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

TABLE 20
DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–25F	DDR2-800 5-5-5
		–2.5	DDR2-800 6-6-6
		–3	DDR2-667 4-4-4
		–3S	DDR2-667 5-5-5
		–3.7	DDR2-533 4-4-4
		–5	DDR2-400 3-3-3

Table of Contents

Edition 2006-12
Published by Qimonda AG
Gustav-Heinemann-Ring 212
D-81739 München, Germany

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