

International **IR** Rectifier

PD-95502

IRFP048RPbF

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Isolated Central Mounting Hole
- 175°C Operating Temperature
- Ease of Parallelizing
- Simple Drive Requirements
- Lead-Free

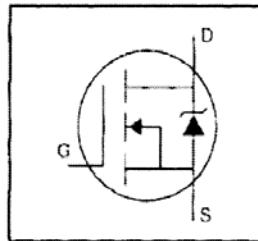
Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

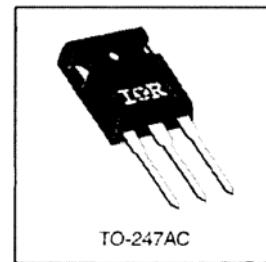
The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	70*	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	52	
I_{DM}	Pulsed Drain Current ①	290	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	190	W
	Linear Derating Factor	1.3	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	200	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10lb-in (1.1N·m)	



$V_{DSS} = 60\text{V}$
 $R_{DS(on)} = 0.018\Omega$
 $I_D = 70^*\text{A}$



Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R_{0JC}	Junction-to-Case	—	—	0.80	$^\circ\text{C/W}$
R_{0CS}	Case-to-Sink, Flat, Greased Surface	—	0.24	—	
R_{0JA}	Junction-to-Ambient			40	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.060	—	$\text{V}/^\circ\text{C}$	Reference to 25°C , $I_D=1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	—	0.018	Ω	$V_{\text{GS}}=10\text{V}$, $I_D=44\text{A}$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}}=V_{\text{GS}}$, $I_D=250\mu\text{A}$
g_{fs}	Forward Transconductance	20	—	—	S	$V_{\text{DS}}=25\text{V}$, $I_D=44\text{A}$ ④
I_{DS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{\text{DS}}=60\text{V}$, $V_{\text{GS}}=0\text{V}$
		—	—	250	μA	$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{\text{GS}}=20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{\text{GS}}=-20\text{V}$
Q_g	Total Gate Charge	—	—	110	nC	$I_D=72\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	29	nC	$V_{\text{DS}}=48\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	38	nC	$V_{\text{GS}}=10\text{V}$ See Fig. 6 and 13 ④
$t_{\text{d(on)}}$	Turn-On Delay Time	—	8.1	—	ns	$V_{\text{DD}}=30\text{V}$
t_r	Rise Time	—	250	—	ns	$I_D=72\text{A}$
$t_{\text{d(off)}}$	Turn-Off Delay Time	—	210	—	ns	$R_G=9.1\Omega$
t_f	Fall Time	—	250	—	ns	$R_D=0.34\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—	nH	
C_{iss}	Input Capacitance	—	2400	—	pF	$V_{\text{GS}}=0\text{V}$
C_{oss}	Output Capacitance	—	1300	—	pF	$V_{\text{DS}}=25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	190	—	—	$f=1.0\text{MHz}$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	70*	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	290		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J=25^\circ\text{C}$, $I_S=73\text{A}$, $V_{\text{GS}}=0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	120	180	ns	$T_J=25^\circ\text{C}$, $I_F=72\text{A}$
Q_{rr}	Reverse Recovery Charge	—	0.50	0.80	μC	$dI/dt=100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11) ③ $I_{\text{SD}} \leq 72\text{A}$, $dI/dt \leq 200\text{A}/\mu\text{s}$, $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$

② $V_{\text{DD}}=25\text{V}$, starting $T_J=25^\circ\text{C}$, $L=43\mu\text{H}$ $R_G=25\Omega$, $I_{AS}=73\text{A}$ (See Figure 12) ④ Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

* Current limited by the package, (Die Current =73A)

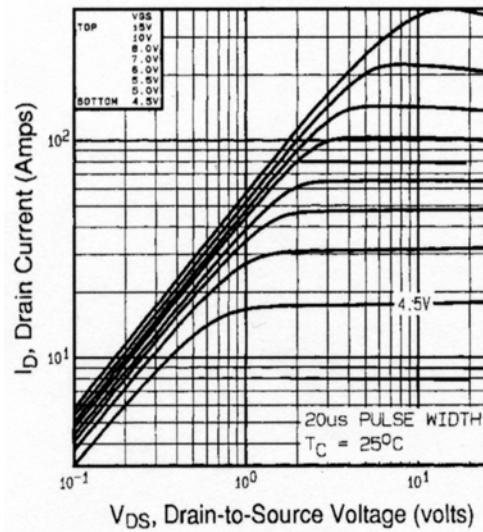


Fig 1. Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$

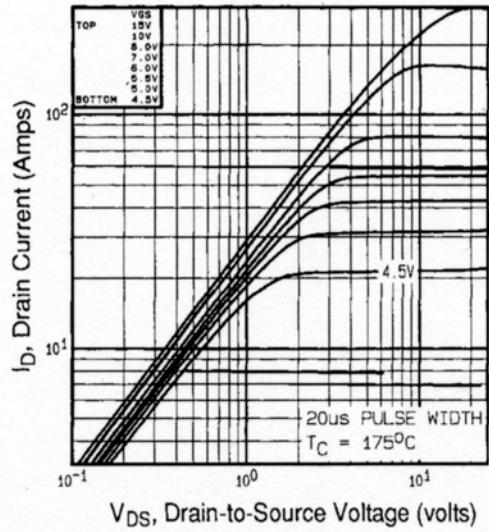


Fig 2. Typical Output Characteristics,
 $T_C = 175^\circ\text{C}$

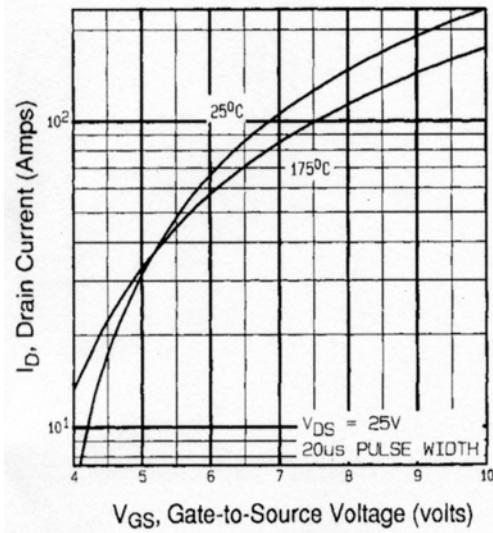


Fig 3. Typical Transfer Characteristics

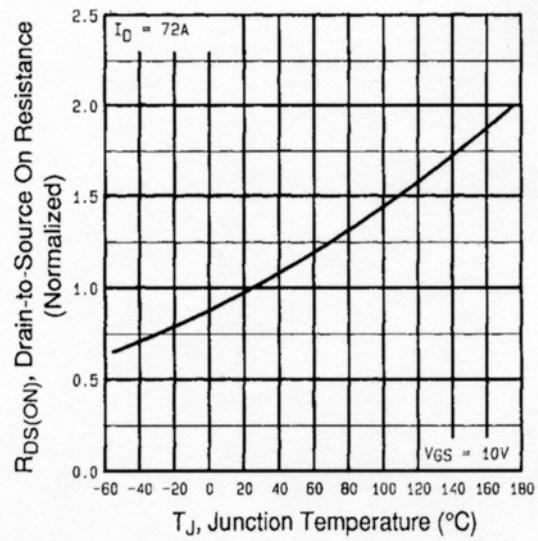


Fig 4. Normalized On-Resistance
Vs. Temperature

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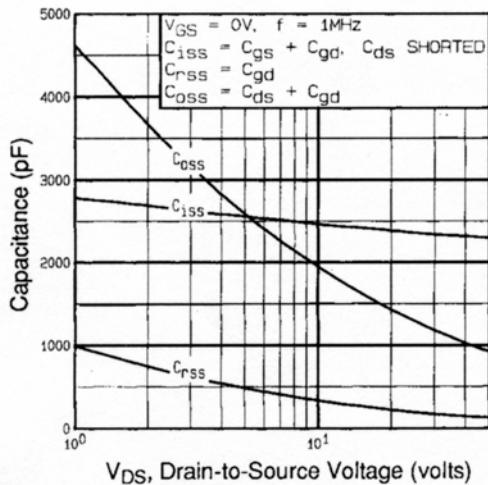


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

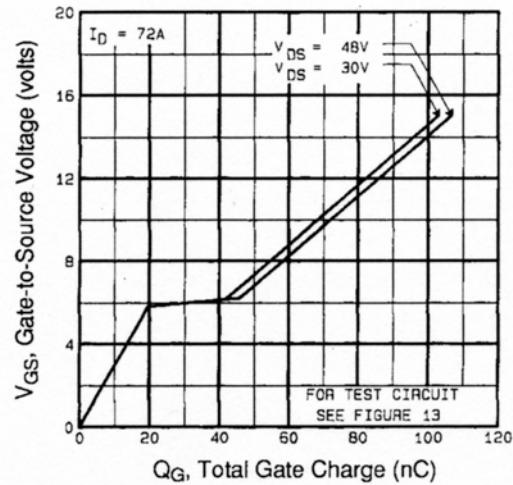


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

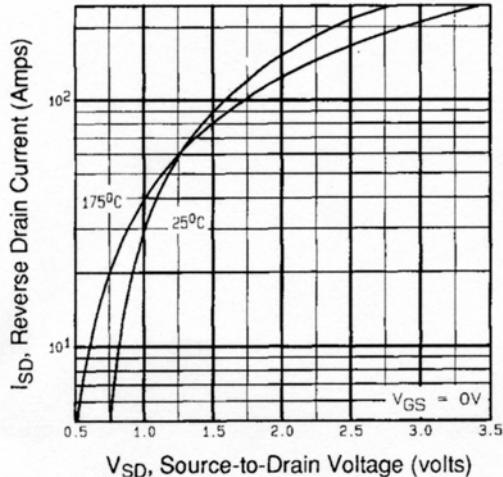


Fig 7. Typical Source-Drain Diode
Forward Voltage

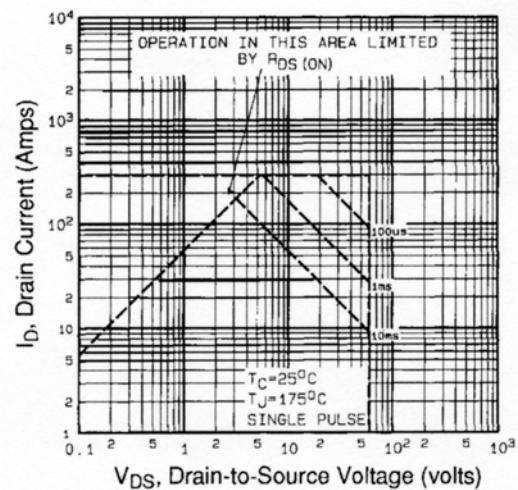


Fig 8. Maximum Safe Operating Area

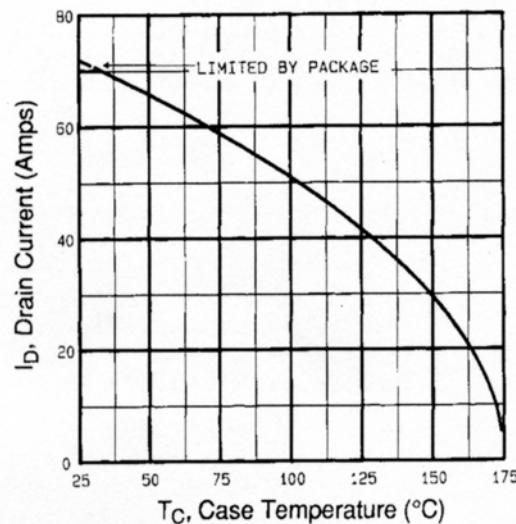


Fig 9. Maximum Drain Current Vs.
Case Temperature

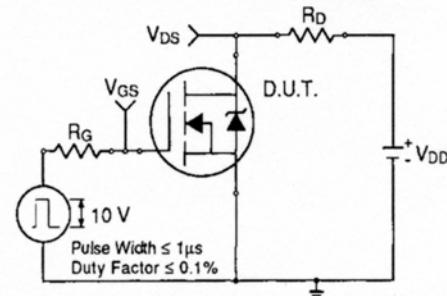


Fig 10a. Switching Time Test Circuit

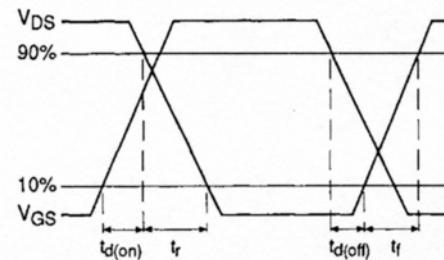


Fig 10b. Switching Time Waveforms

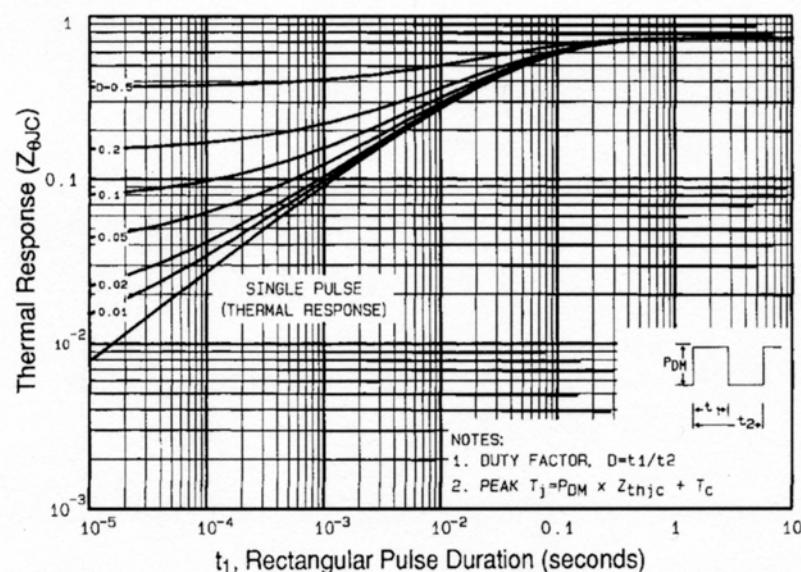


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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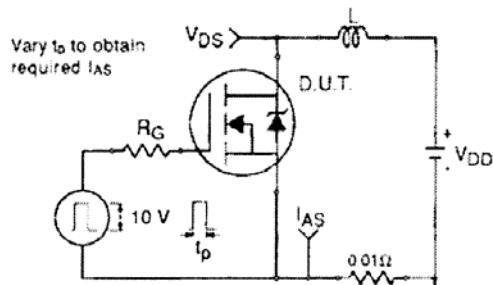


Fig 12a. Unclamped Inductive Test Circuit

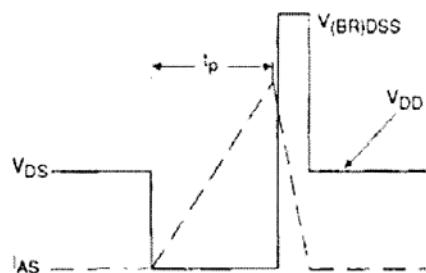


Fig 12b. Unclamped Inductive Waveforms

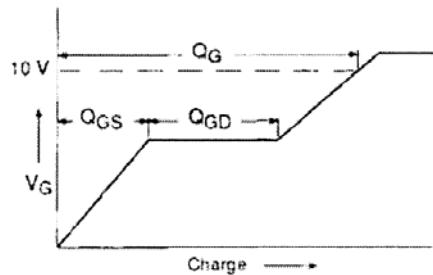


Fig 13a. Basic Gate Charge Waveform

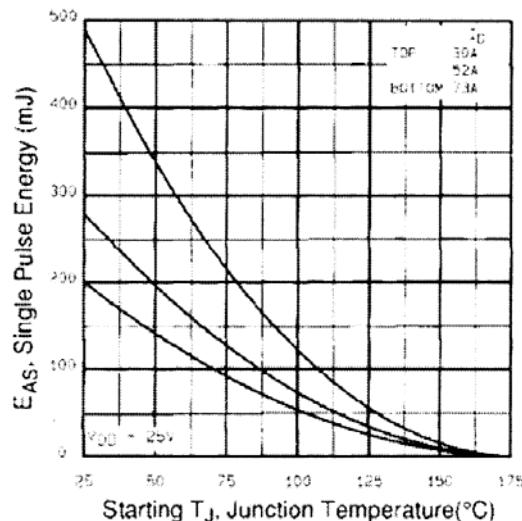


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

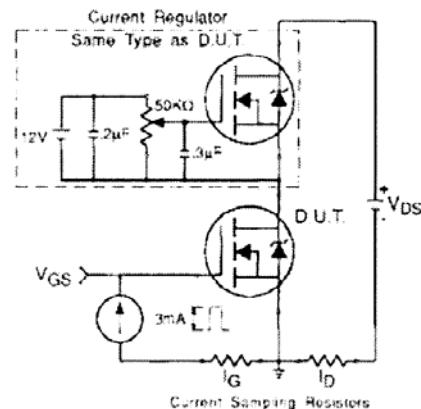
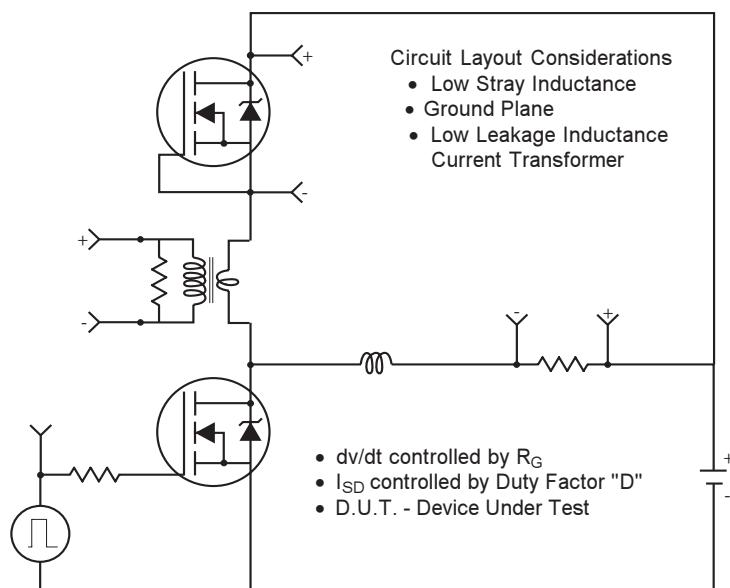


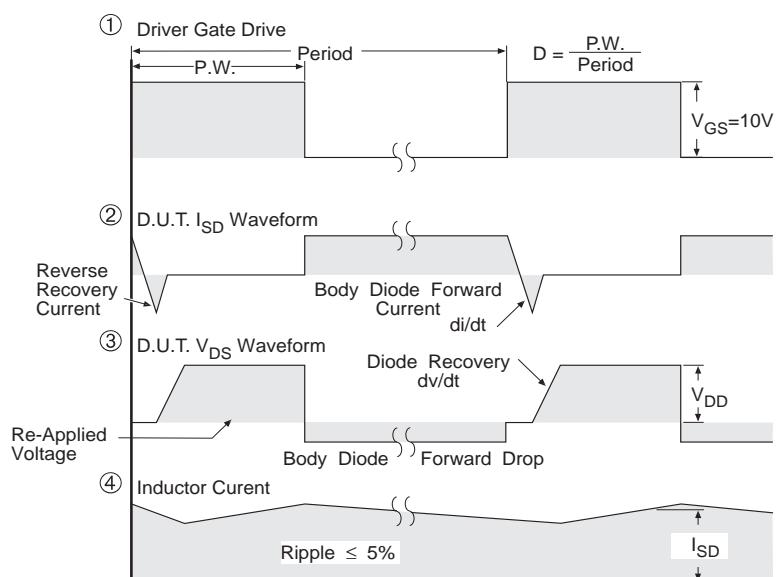
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

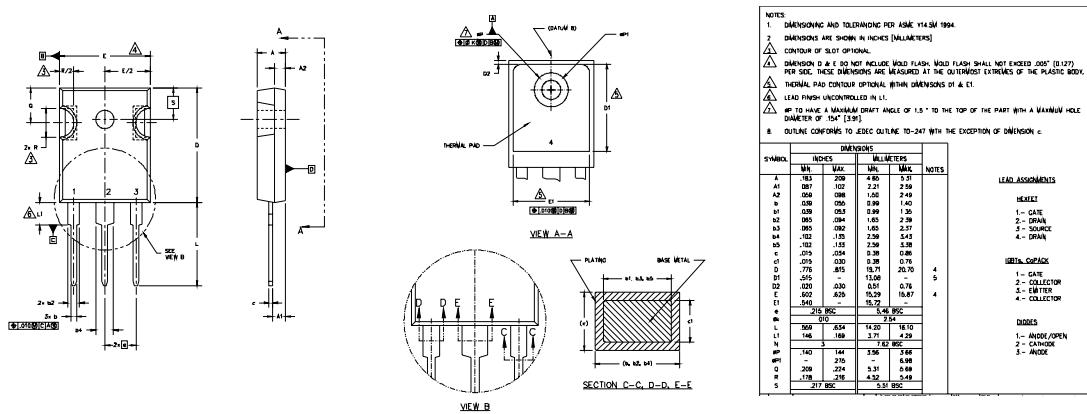
Fig 14. For N-Channel HEXFETS

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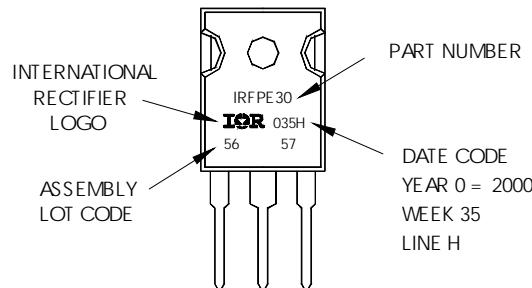
TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"
Note: "P" in assembly line
position indicates "Lead-Free"



Data and specifications subject to change without notice.

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