GENERAL DESCRIPTION

The XRT59L921 is an optimized twenty-one channel, E1, line interface unit, fabricated using low power CMOS technology. The device contains twenty-one independent E1 channels. It is primarily targeted towards the SDH multiplexers that accommodate TU12 Tributary Unit Frames. Line cards in these units multiplex 21 E1 channels into higher SDH rates. Devices with 21 E1 interfaces such as the XRT59L921 provide the most efficient method of implementing 63-channel line cards. Each channel performs the driver and receiver functions necessary to convert bipolar signals to logical levels and vice versa.

The receiver input accepts transformer coupled 1:1 signals, while the transmitter is coupled to the line using a 1:2 transformer. The same transformer configuration can be used for both balanced and unbalanced interfaces. The device offers Loss of Signal (LOS) detection, that provides an LOS output indication signal with thresholds and delay that comply with the ITU G.775 requirements.

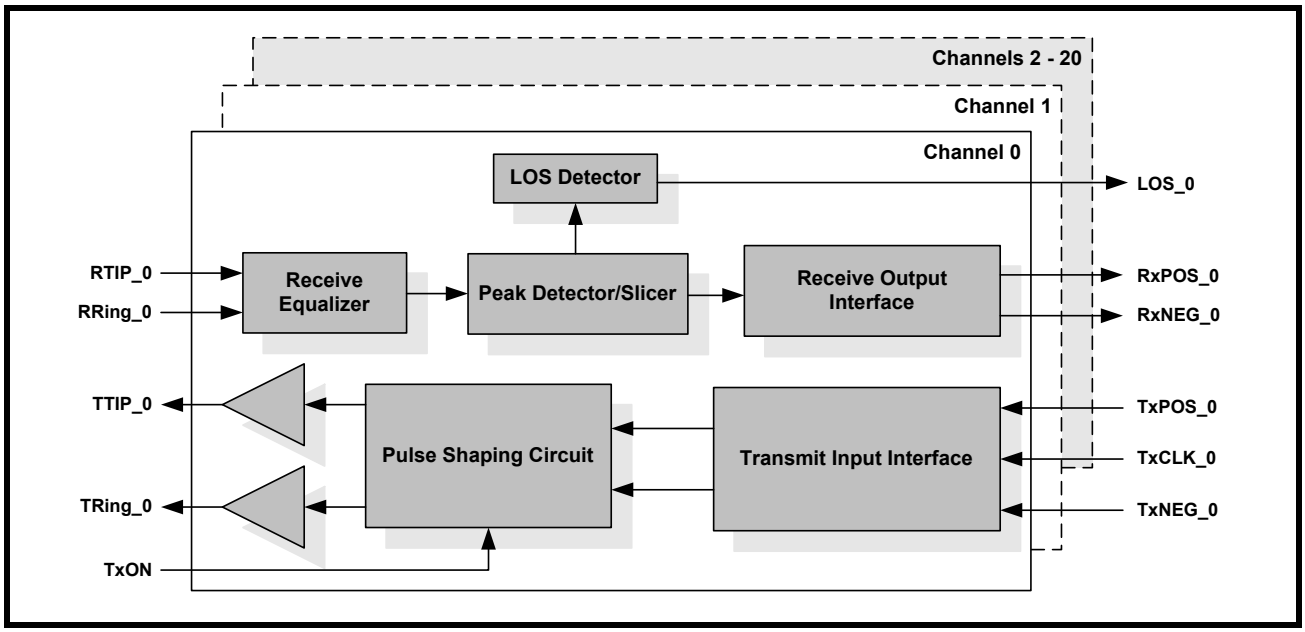
FEATURES

- Twenty-One (21) Independent E1 (CEPT) Line Interface Units (Transmitter, Receiver, and Recovery)
- Transmit Output Pulses that are Compliant with the ITU-T G.703 Pulse Template Requirement for 2.048Mbps (E1) Rates
- On-Chip Pulse Shaping for both 75Ω and 120Ω line drivers
- Detects and Clears LOS (Loss of Signal) Per ITU-T G.775
- Operates over the Industrial Temperature Range
- Ultra Low power consumption
- 3.3V operation with 5V Tolerant Input

APPLICATIONS

- PDH Multiplexers
- SDH Multiplexers
- Digital Cross-Connect Systems
- DECT (Digital European Cordless Telephone) Base Stations
- CSU/DSU Equipment

FIGURE 1. BLOCK DIAGRAM OF THE XRT59L921



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT59L921IB	316 Shrink Thin Ball Grid Array (21.0 mm x 21.0 mm, STBGA)	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRT59L921 (BOTTOM VIEW)

20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	A
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	B
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	C
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	D
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	E
O	O	O	O	O											O	O	O	O	O	F
O	O	O	O	O											O	O	O	O	O	G
O	O	O	O	O											O	O	O	O	O	H
O	O	O	O	O				O	O	O	O				O	O	O	O	O	J
O	O	O	O	O				O	O	O	O				O	O	O	O	O	K
O	O	O	O	O				O	O	O	O				O	O	O	O	O	L
O	O	O	O	O				O	O	O	O				O	O	O	O	O	M
O	O	O	O	O											O	O	O	O	O	N
O	O	O	O	O											O	O	O	O	O	P
O	O	O	O	O											O	O	O	O	O	R
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	T
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	U
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	V
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	W
O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	Y

NOTE: Refer to pin list for pin names.

TABLE OF CONTENTS

PIN DESCRIPTIONS

PIN#	SYMBOL	TYPE	DESCRIPTION
D8 C9 D9 A10 C11 A12 V10 Y9 U9 V8 U7 U14 Y14 V12 Y12 Y11 B13 D13 C14 B14 A15	RxPOS_0 RxPOS_1 RxPOS_2 RxPOS_3 RxPOS_4 RxPOS_5 RxPOS_6 RxPOS_7 RxPOS_8 RxPOS_9 RxPOS_10 RxPOS_11 RxPOS_12 RxPOS_13 RxPOS_14 RxPOS_15 RxPOS_16 RxPOS_17 RxPOS_18 RxPOS_19 RxPOS_20	O	**Receiver Positive Data Out – Channel_n: (n=0 to 20)** This output pin will pulse “High” whenever Channel_n, within the XRT59L921 has received a Positive Polarity pulse, in the incoming line signal, at RTIP_n/RRing_n inputs.
E7 C8 E9 B9 C10 B11 V9 W8 T9 U8 T7 T14 W14 V13 W12 W10 C12 E13 D14 C15 A14	RxNEG_0 RxNEG_1 RxNEG_2 RxNEG_3 RxNEG_4 RxNEG_5 RxNEG_6 RxNEG_7 RxNEG_8 RxNEG_9 RxNEG_10 RxNEG_11 RxNEG_12 RxNEG_13 RxNEG_14 RxNEG_15 RxNEG_16 RxNEG_17 RxNEG_18 RxNEG_19 RxNEG_20	O	**Receiver Negative Data Out – Channel_n:** This output pin will pulse “High” whenever Channel_n, within the XRT59L921 has received a Negative Polarity pulse, in the incoming line signal, at RTIP_n/RRing_n inputs.

PIN DESCRIPTIONS

PIN#	SYMBOL	TYPE	DESCRIPTION
D7 B8 E8 A9 B10 A11 W9 Y8 T8 V7 T6 T15 Y13 W13 W11 Y10 B12 E14 C13 B15 A13	LOS_0 LOS_1 LOS_2 LOS_3 LOS_4 LOS_5 LOS_6 LOS_7 LOS_8 LOS_9 LOS_10 LOS_11 LOS_12 LOS_13 LOS_14 LOS_15 LOS_16 LOS_17 LOS_18 LOS_19 LOS_20	O	**Receiver Loss of Signal Output Indicator – Channel_n:** This output pin toggles “High” if Channel_n, within the XRT59L921 has detected a Loss of Signal condition in the incoming line signal.
B1 D1 E1 G1 H1 K1 L1 N1 P1 T1 U1 U20 T20 P20 N20 L20 K20 H20 G20 E20 D20	RTIP_0 RTIP_1 RTIP_2 RTIP_3 RTIP_4 RTIP_5 RTIP_6 RTIP_7 RTIP_8 RTIP_9 RTIP_10 RTIP_11 RTIP_12 RTIP_13 RTIP_14 RTIP_15 RTIP_16 RTIP_17 RTIP_18 RTIP_19 RTIP_20	I	**Receiver_n Positive Bipolar Input – Channel_n:** The Receive Section of Channel_n uses this input pin, along with RRing_n to receive the bipolar line signal from the Remote E1 Terminal.

PIN DESCRIPTIONS

PIN#	SYMBOL	TYPE	DESCRIPTION
C1 D2 E2 G2 H2 K2 L2 N2 P2 T2 U2 U19 T19 P19 N19 L19 K19 H19 G19 E19 D19	RRing_0 RRing_1 RRing_2 RRing_3 RRing_4 RRing_5 RRing_6 RRing_7 RRing_8 RRing_9 RRing_10 RRing_11 RRing_12 RRing_13 RRing_14 RRing_15 RRing_16 RRing_17 RRing_18 RRing_19 RRing_20	I	**Receiver Negative Bipolar Input – Channel_n:** The Receive Section of Channel_n uses this input pin, along with RTIP_n to receive the bipolar line signal from the Remote E1 Terminal.
V11	TxON	I	**Transmit ON/OFF Input:** Upon power up, all of the transmitters are powered off. If the TxON pin is pulled "High" all 21 transmitters are powered on. Individual Channels can be powered down by connecting TxClk_n "Low" and with TPOS_n/TNEG_n data applied to that Channel_n. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

PIN DESCRIPTIONS

PIN#	SYMBOL	TYPE	DESCRIPTION
C4 D5 F4 G5 J4 K5 M4 N5 R4 T5 V4 V17 T16 R17 N16 M17 K16 J17 G16 F17 D16	TTIP_0 TTIP_1 TTIP_2 TTIP_3 TTIP_4 TTIP_5 TTIP_6 TTIP_7 TTIP_8 TTIP_9 TTIP_10 TTIP_11 TTIP_12 TTIP_13 TTIP_14- TTIP_15- TTIP_16- TTIP_17 TTIP_18 TTIP_19 TTIP_20	O	**Transmitter Positive Bipolar Output – Channel_n:** Channel_n within the XRT59L921 will use this pin, along with TRing_n, to transmit a bipolar line signal, via a 1:2 step-up transformer.
C3 D4 F3 G4 J3 K4 M3 N4 R3 T4 V3 V18 T17 R18 N17 M18 K17 J18 G17 F18 D17	TRing_0 TRing_1 TRing_2 TRing_3 TRing_4 TRing_5 TRing_6 TRing_7 TRing_8 TRing_9 TRing_10 TRing_11 TRing_12 TRing_13 TRing_14 TRing_15 TRing-16 TRing_17 TRing_18 TRing_19 TRing_20	O	**Transmitter Negative Bipolar Output – Channel_n:** Channel_n within the XRT59L921 will use this pin, along with TTIP_n, to transmit a bipolar line signal, via a 1:2 step-up transformer.

PIN DESCRIPTIONS

PIN#	SYMBOL	TYPE	DESCRIPTION
A2 A4 A6 C7 E6 A8 U6 W5 Y6 Y4 W2 Y19 Y17 Y15 V15 U15 E15 C18 B17 A18 B20	TxClk_0 TxClk_1 TxClk_2 TxClk_3 TxClk_4 TxClk_5 TxClk_6 TxClk_7 TxClk_8 TxClk-9 TxClk_10 TxClk_11 TxClk_12 TxClk_13 TxClk_14 TxClk_15 TxClk_16 TxClk_17 TxClk_18 TxClk_19 TxClk_20	I	**Transmitter Clock Input – Channel_n:** If the user operates Channel_n (within the XRT59L921) in the Clock mode, then the Transmit Section of the Channel_n will use the falling edge of this signal to sample the data at the TxPOS_n and TxNEG_n input pins. ***NOTE:*** *If the user operates the Channel_n in the clockless mode, then the Terminal Equipment should not apply a clock signal to this input pin and TxCLK should be tied "High".*
B3 B4 B6 D6 E4 B7 U4 V6 W7 W4 W3 W19 W17 W16 V14 U17 E17 C16 B16 B18 B19	TxNEG_0 TxNEG_1 TxNEG_2 TxNEG_3 TxNEG_4 TxNEG_5 TxNEG_6 TxNEG_7 TxNEG_8 TxNEG_9 TxNEG_10 TxNEG_11 TxNEG_12 TxNEG_13 TxNEG_14 TxNEG_15 TxNEG_16 TxNEG_17 TxNEG_18 TxNEG_19 TxNEG_20	I	**Transmitter - Negative Data Input – Channel_n:** The exact signal that should be applied to this input pin depends upon whether the user intends to operate the Transmit Section (of Channel_n) in the Clock or Clockless Mode **Clock Mode:** The Terminal Equipment should apply bit-wide NRZ pulses on this input pin, whenever the Terminal Equipment needs to transmit a Negative-Polarity pulse onto the line via TTIP_n and TRing_n output pins. The XRT59L921 will sample this input pin upon the falling edge of the TClk_n signal. **Clockless Mode:** The Terminal Equipment should apply RZ pulses to this input pin, anytime the Terminal Equipment needs to transmit a Negative-Polarity pulse onto the line viaTTIP_n and TRing_n output pins. ***NOTE:*** *In clockless mode, transmit output pulse width is determined by the RZ signal applied to TxNEG/TxPOS.*

PIN DESCRIPTIONS

PIN#	SYMBOL	TYPE	DESCRIPTION
A3 A5 B5 C6 E5 A7 U5 W6 Y7 Y5 Y3 Y18 W18 Y16 W15 U16 E16 C17 A16 A17 A19	TxPOS_0 TxPOS_1 TxPOS_2 TxPOS_3 TxPOS_4 TxPOS_5 TxPOS_6 TxPOS_7 TxPOS_8 TxPOS_9 TxPOS_10 TxPOS_11 TxPOS_12 TxPOS_13 TxPOS_14 TxPOS_15 TxPOS_16 TxPOS_17 TxPOS_18 TxPOS_19 TxPOS_20	I	**Transmitter - Positive Data Input – Channel_n:** The exact signal that should be applied to this input pin depends upon whether the user intends to operate the Transmit Section (of Channel_n) in the Clock or Clock-less Mode. **Clock Mode:** The Terminal Equipment should apply bit-wide NRZ pulses on this input whenever the Terminal Equipment needs to transmit a Positive-Polarity pulse onto the line via TTIP_n and TRing_n output pins. The XRT59L921 will sample this input pin upon the falling edge of the TClk_n signal. **Clockless Mode:** The Terminal Equipment should apply RZ pulses to this input pin, anytime the Terminal Equipment needs to transmit a Positive-Polarity pulse onto the line via TTIP_n and TRing_n output pins.
L5	TCK	I	**JTAG Test Clock input, Boundary Scan Clock input:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation. internally pulled "High" with a 50kΩ resistor.*
H4	TDI	I	**JTAG Test Data input, Boundary Scan Test Data Input:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation. internally pulled "High" with a 50kΩ resistor.*
L4	TDO	O	**JTAG Test Data output:** Boundary Scan Test Data Output:
H5	TMS	I	**JTAG Test Mode Select, Boundary Scan Test Mode Select input pin:**
P4	TRST	I	**JTAG Test Mode Reset, Boundary Scan Mode Reset Input pin:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation. internally pulled "High" with a 50kΩ resistor.*
H17 T13 U13	FACTORY TEST PINS		**FACTORY TEST PINS:** The customer must tie these pins to ground for normal operation.
E10 E12 T10 T12 L16	AGND AGND AGND AGND AGND	-	**Analog Ground -** Receivers

PIN DESCRIPTIONS

PIN#	SYMBOL	TYPE	DESCRIPTION
D10 D12 U10 U12 L17	AVDD AVDD AVDD AVDD AVDD	-	**Positive Supply** - (+3.3V ± 5%). Receivers
A1 A20 Y1 Y2 Y20 U11 W20 C20 D11	DVDD DVDD DVDD DVDD DVDD DVDD	-	**Positive Supply** (+3.3V ± 5%). Digital Circuitry.
F1 F20 J1 J20 M1 M20 R1 R20 W1 T11 V1 V20 C19 E11 B2	DGND DGND DGND DGND DGND DGND	-	**Digital Ground:** Digital Circuitry.

PIN DESCRIPTIONS

PIN#	SYMBOL	TYPE	DESCRIPTION
H16 J9 J10 J11 J12 K9 K10 K11 K12 L9 L10 L11 L12 M9 M10 M11 M12 P5 P16 P17	AGND	-	**Ground Pins**
D15	N/C	-	**No Connect**

PIN DESCRIPTIONS

PIN#	SYMBOL	TYPE	DESCRIPTION
C2 D3 F2 G3 J2 K3 M2 N3 R2 T3 V2 V19 T18 R19 N18 M19 K18 J19 G18 F19 D18	TGND_0 TGND_1 TGND_2 TGND_3 TGND_4 TGND_5 TGND_6 TGND_7 TGND_8 TGND_9 TGND_10 TGND_11 TGND_12 TGND_13 TGND_14 TGND_15 TGND_16 TGND_17 TGND_18 TGND_19 TGND_20	-	**Digital Ground.** Transmitter_n
C5 E3 F5 H3 J5 L3 M5 P3 R5 U3 V5 V16 U18 R16 P18 M16 L18 J16 H18 F16 E18	TVDD_0 TVDD_1 TVDD_2 TVDD_3 TVDD_4 TVDD_5 TVDD_6 TVDD_7 TVDD_8 TVDD_9 TVDD_10 TVDD_11 TVDD_12 TVDD_13 TVDD_14 TVDD_15 TVDD_16 TVDD_17 TVDD_18 TVDD_19 TVDD_20	-	**Positive Supply** (+3.3V ± 5%), Transmitter_n

RECEIVER ELECTRICAL CHARACTERISTICS

T_A=-40 to 85°C, V_{DD}=3.3V±5%, unless otherwise specified.

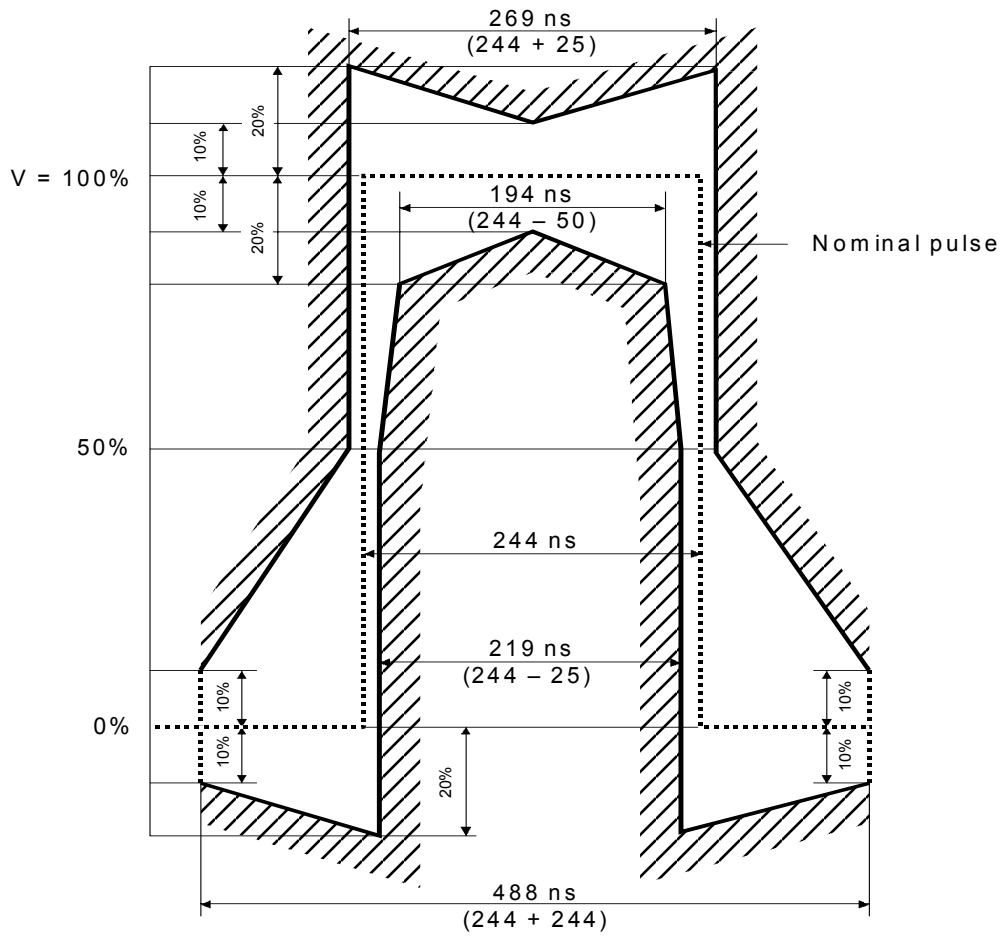
Parameter	Min	Typ	Max	Unit	Test Conditions
Receiver Loss of Signal:					
Threshold to Assert	-	20	-	dB	Cable attenuation @ 1024KHz
Threshold to Clear	-	15	-	dB	
Time Delay	10	-	255	bit	Per ITU-G.775
Hysteresis	-	5	-	dB	
Receiver Sensitivity	9	11	-	dB	Below nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω applications.
Interference Margin	-18	-14	-	dB	With 6dB cable loss.
Input Impedance	5	-	-	KΩ	
Jitter Tolerance:					
20Hz	10			UIpp	
700Hz	5	-	-	UIpp	
10KHz —100KHz	0.3			UIpp	
Return Loss:					
51KHz —102KHz	14	-	-	dB	Per ITU-G.703
102KHz—2048KHz	20	-	-	dB	
2048KHz—3072KHz	16	-	-	dB	

TRANSMITTER ELECTRICAL CHARACTERISTICS

TA=-40 to 85°C, VDD=3.3V±5%, unless otherwise specified

Parameter	Min	Typ	Max	Unit	Test Conditions
AMI Output Pulse Amplitude:					
75Ω Application	2.13	2.37	2.60	V	Use transformer with 1:2 ratio and 9.1Ω resistor in series with each end of primary
120Ω Application	2.70	3.0	3.30	V	
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	–	1.05	–	Per ITU-G.703
Output Pulse Amplitude Ratio	0.95	–	1.05	–	Per ITU-G.703
Output Return Loss:					
51KHz —102KHz	8	-	-	dB	Per ETSI 300 166 and G.703
102KHz—2048KHz	8	-	-	dB	
2048KHz—3072KHz	8	-	-	dB	

FIGURE 3. E1. ITU G.703 PULSE TEMPLATE FOR TRANSMITTER OUTPUT



Note – V corresponds to the nominal peak value.

DC ELECTRICAL CHARACTERISTICS

TA=-25°C, VDD=3.3V±5%, unless otherwise specified

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage	VDD	3.13	3.3	3.46	V
Input High Voltage	VIH	2.0	-	5.0	V
Input Low Voltage	VIL	-0.5	-	0.8	V
Output High Voltage @ IOH=-5mA	VOH	2.4	-	-	V
Output Low Voltage @ IOL=5mA	VOL	-		- 0.4	V
Input Leakage Current (except Input pins w/ pull-up resistor.)	IL	-	-	± 10	µA
Input Capacitance	CI		5.0		pF
Output Load Capacitance	CL	-	-	25	pF

AC ELECTRICAL CHARACTERISTICS

TA=-25°C, VDD=3.3V±5%, unless otherwise specified

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
TCLK Clock Period	T_1	-	488	-	ns
TCLK Duty Cycle	T_2	47	50	53	%
Transmit Data Setup Time	T_{su}	50	-	-	ns
Transmit Data Hold Time	T_{ho}	30	-	-	ns
Transmit Data Prop. Delay Time - RZ data Mode - NRZ data Mode (clock mode)	T_3	 - -	 30 30	 - -	 ns ns
TCLK Rise Time(10%/90%)	T_r	-	-	40	ns
TCLK Fall Time(90%/10%)	T_f	-	-	40	ns
Receive Data Rise Time	R_{tr}	-	-	40	ns
Receive Data Fall Time	R_{tf}	-	-	40	ns
Receive Data Prop. Delay	R_{pd}	-	75	-	ns
Receive Data Pulse Width	R_{xpw}	200	244	350	ns

PER CHANNEL POWER CONSUMPTION INCLUDING THE LINE POWER DISSIPATION, TRANMISSION AND RECEIVE PATHS ALL ACTIVE:

TA=-40 to 85°C, VDD=3.3V±5%, unless otherwise specified

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Power Consumption	PC	-	510		mW	75Ω load, operating at 50% Mark Density.
Power Consumption	PC	-	650		mW	120Ω load, operating at 50% Mark Density.
Power Consumption	PC	-	1000		mW	75Ω load, operating at 100% Mark Density.
Power Consumption	PC	-	900		mW	120Ω load, operating at 100% Mark Density.
Power Consumption	PC	-	170		mW	Transmitter in Powered-down mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to + 150°C	
Operating Temperature	-40°C to + 85°C	
ESD Rating	>2000V on all pins	***NOTE:*** *Human Body Model, 100pF capacitor discharged through a 1.5KΩ resistor.*
Supply Voltage	-0.5V to + 6.0V	

SYSTEM DESCRIPTION

The XRT59L921 is a Twenty-One (21) channel E1 transceiver that provides an electrical interface for 2.048Mbps applications. Each of the twenty-one channels includes a receive circuit that converts an ITU-T G.703 compliant bipolar signal into a TTL compatible logic levels. Each receiver also includes an LOS (Loss of Signal) detection circuit. Similarly, in the Transmit Direction, each Transmitter converts TTL compatible logic levels into a G.703 compatible bipolar signal. The Transmitter may be operated in either a Clock or Clockless Mode.

Each channel within the XRT59L921 LIU consists of both a Transmit Section and a Receive Section, each of these sections will be discussed in detail below.

1.0 THE TRANSMIT SECTION

In general, the purpose of the Transmit Section (within each channel of the XRT59L921) is to accept TTL/CMOS level digital data (from the Terminal Equipment), and to encode it into a format such that it can:

1. Be efficiently transmitted over coaxial- or twistedpair cable at the E1 data rate and
2. Be reliably received by the Remote Terminal Equipment at the other end of the E1 data link.
3. Comply with the ITU-T G.703 pulse template requirements, for E1 applications.

The circuitry that the Transmit Section (within the XRT59L921) uses to accomplish this goal is discussed below. The Transmit Section of the XRT59L921 consists of the following blocks:

- Transmit Input Interface
- Pulse Shaping Block

1.1 The Transmit Input Interface

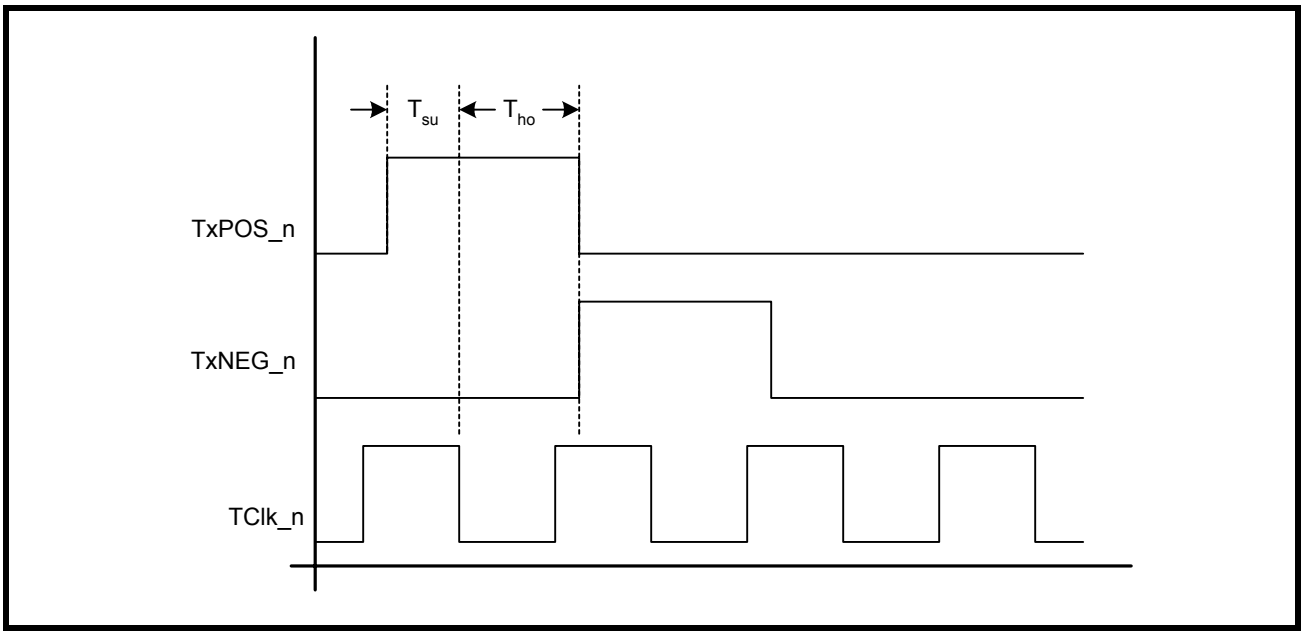
The Transmit Input Interface accepts either Clock or clockless data from the Terminal Equipment. The manner in how the Terminal Equipment should apply data to a given channel within the XRT59L921 depends upon whether the channel is being operated in the Clock or clockless mode.

1.2 Operating the Transmitter in the Clock Mode

The user can configure a given channel (within the XRT59L921) to operate in the Clock mode by simply applying a 2.048MHz clock signal to the TxClk_n input pin (where x denotes a given channel within the XRT59L921). The XRT59L921 contains circuitry that senses activity on the TxClk_n line. If this circuit senses activity on the TxClk_n line, then the corresponding channel will automatically be operating in the Clock Mode.

In the Clock Mode, the Terminal Equipment is expected to apply a 2.048MHz clock signal at the TxClk_n input pin and NRZ data at the TxPOS_n and TxNEG_n input pins. The Transmit Input Interface circuit will sample the data, at the TxPOS_n and TxNEG_n input pins, upon the falling edge of TxClk_n, as illustrated in **Figure 4**.

FIGURE 4. ILLUSTRATION ON HOW THE XRT59L921 SAMPLES THE DATA ON THE TXPOS_N AND TXNEG_N INPUT PINS



In general, if the XRT59L921 samples a “1” on the TxPOS_n input pin, then the Transmit Section of the device will ultimately generate a positive polarity pulse via the TTIP_n and TRing_n output pins (across a 1:2 transformer). Conversely, if the XRT59L921 samples a “1” on the TxNEG_n input pin, then the Transmit Section of the device will ultimately generate a negative polarity pulse via the TTIP_n and TRing_n output pins (across a 1:2 transformer).

1.2.1 Operating the Transmitter in the Clockless Mode

The user can configure a given channel (within theXRT59L921) to operate in the Clockless mode by doing the following:

- Not applying a clock signal to the TxClk_n input, and pulling this pin to VDD.
- By applying RZ (Return to Zero) data to the TxPOS_n and TxNEG_n input pins, as illustrated below.
- If TxClk_n is grounded and RZ data is applied to TPOS and TNEG, the transmitter will be powered down and tri-stated.

1.2.2 Shutting off the Transmiter

The Transmit Driver for each Channel_n (within the XRT59L921) can be shut off. To activate this feature, Connect the TxCLK_n input pin to a logic "0" (e.g. GND) and continue to apply data via the TxPOS_n and TxNEG_n input pins.

FIGURE 5. ILLUSTRATION ON HOW THE TERMINAL EQUIPMENT SHOULD APPLY DATA TO THE TRANSMIT SECTION OF A GIVEN CHANNEL (WITHIN THE XRT59L921), WHEN OPERATING IN THE CLOCKLESS MODE

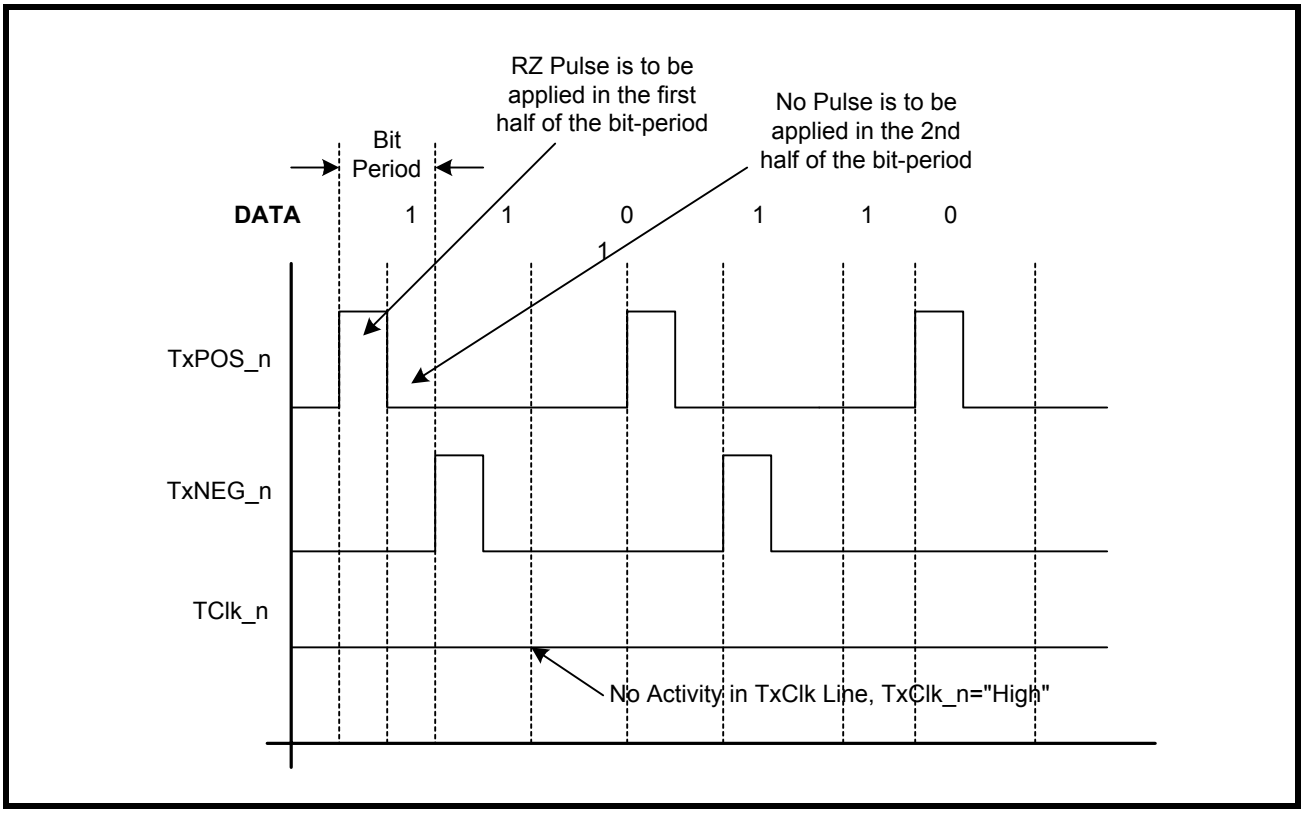


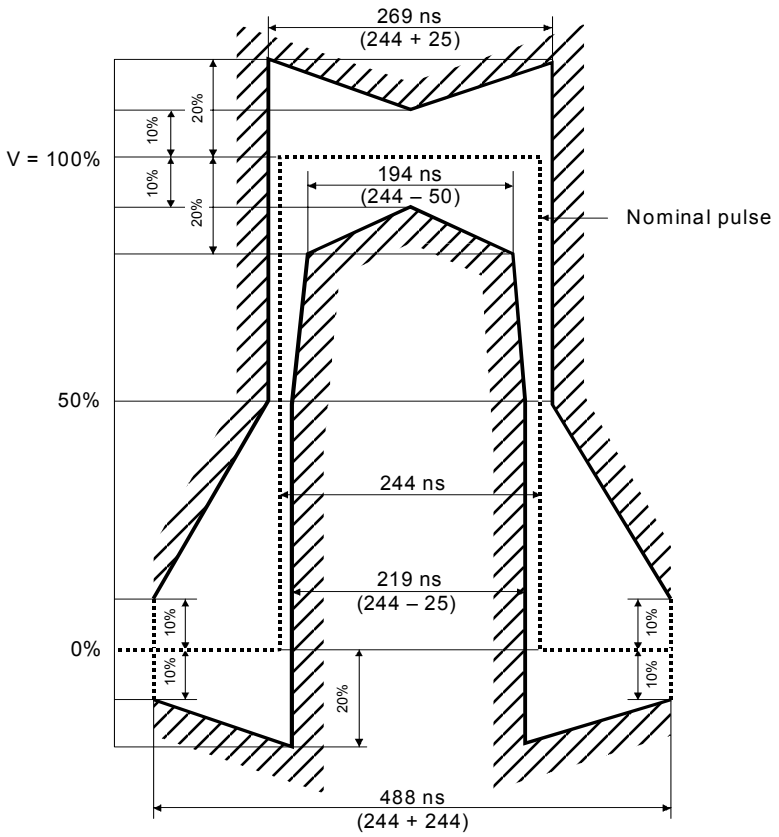
Figure 5, indicates that when the user is operating a channel in the Clockless Mode, then the corresponding Terminal Equipment must do the following:

- Not apply a signal on the TxClk_n line and connect TxClk to "High"
- When applying a pulse (to either the TxPOS_n or TxNEG_n input pin), apply an RZ pulse to the appropriate input pin. This RZ pulse should only have a width of one-half the bit-period.

1.3 The Pulse Shaping Circuit

The purpose of the Transmit Pulse Shaping circuit is to generate Transmit Output pulses that comply with the ITU-T G.703 Pulse Template Requirements for E1 Applications.

FIGURE 6. ILLUSTRATION OF THE ITU-T G.703 PULSE TEMPLATE FOR E1 APPLICATIONS



Note – V corresponds to the nominal peak value.

Each channel (within the XRT59L921) will take each mark (which is provided to it via the Transmit Input Interface block, and will generate a pulse that complies with the pulse template, presented in **Figure 6**, (when measured on the secondary-side of the Transmit Output Transformer).

1.4 Interfacing the Transmit Sections of the XRT59L921 to the Line

ITU-T G.703 specifies that the E1 line signal can be transmitted over coaxial cable and terminated with 75Ω or transmitted over twisted-pair and terminated with 120Ω. However, in both applications (e.g., 75Ω or 120Ω), the user is advised to interface the Transmitter to the Line, in the manner as depicted in **Figure 7** and **Figure 8**, respectively.

FIGURE 7. ILLUSTRATION OF HOW TO INTERFACE THE TRANSMIT SECTIONS OF THE XRT59L921 TO THE LINE (FOR 75Ω APPLICATIONS)

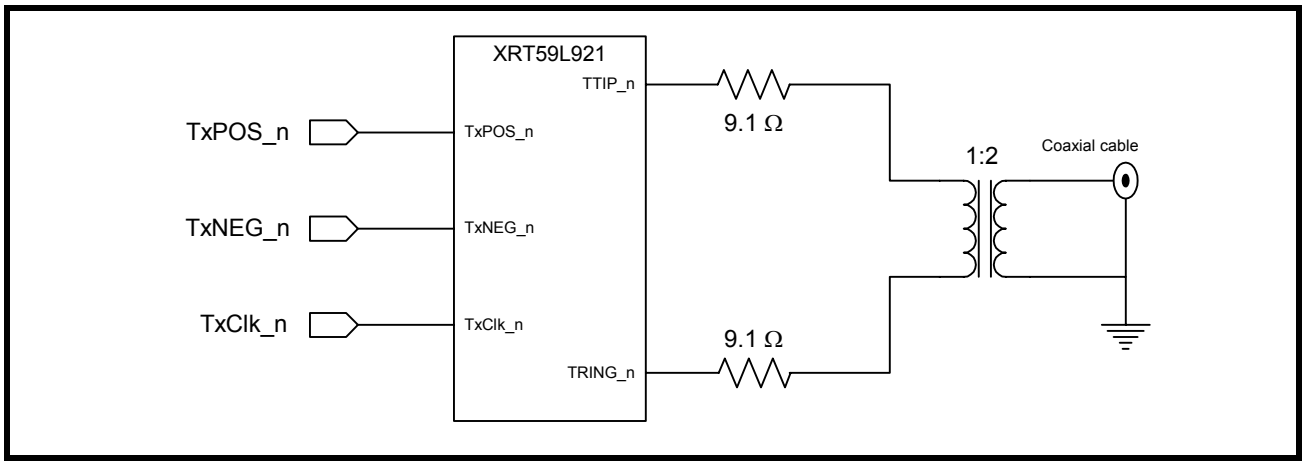
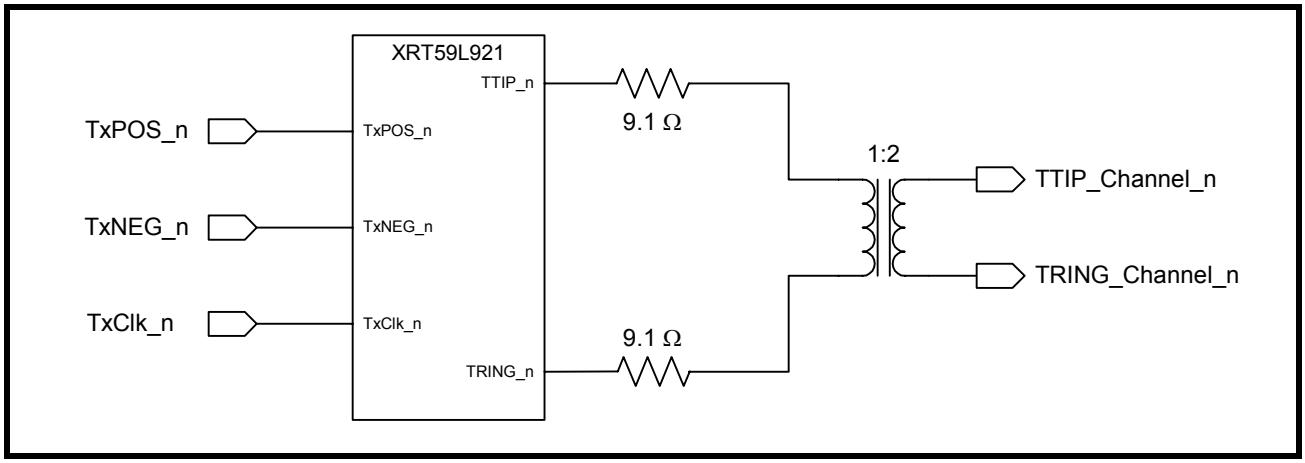


FIGURE 8. ILLUSTRATION OF HOW TO INTERFACE THE TRANSMIT SECTIONS THE XRT59L921 TO THE LINE (FOR 120Ω APPLICATIONS)



NOTES:

1. *Figure 7 and Figure 8, indicate that for both 75Ω and 120Ω applications, the user should connect a 9.1Ω resistor, in series, between the TTIP/TRing outputs and the transformers.*
2. *Figure 5 and 6, indicate that the user should use a 1:2 STEP-UP Transformer.*

TRANSMIT TRANSFORMER RECOMMENDATIONS

PARAMETER	VALUE
Turns Ratio	1:2
Primary Inductance	
Isolation Voltage	
Leakage Inductance	

THE FOLLOWING TRANSFORMERS ARE RECOMMENDED FOR USE

PART NUMBER	VENDOR	ISOLATION	PACKAGE TYPE
PE-65835	Pulse		
TTI 7154-R	Transpower Technologies, Inc.		
TG26-1205	HALO		

NOTE: More transformers will be added to this list as they are evaluated .

MAGNETIC SUPPLIER INFORMATION

Pulse

Corporate Office

12220 World Trade Drive

San Diego, CA 92128

Tel: (619)-674-8100

FAX: (619)-674-8262

Europe

1 & 2 Huxley Road

The Surrey Research Park

Guildford, Surrey GU2 5RE

United Kingdom

Tel: 44-1483-401700

FAX: 44-1483-401701

Asia

150 Kampong Ampat

#07-01/02

KA Centre

Singapore 368324

Tel: 65-287-8998

FAX: 65-280-0080

Transpower Technologies

Corporate Office

9410 Prototype Drive, Ste #1

Reno, NV 89511

Tel: (800)511-7308 or

(775)852-0140

Fax: (775)852-0145

www.trans-power.com

HALO Electronics

P.O. Box 5826

Redwood City, CA 94063

Tel: (650)568-5800

FAX: (650)568-6161

2.0 THE RECEIVE SECTION

The Receive Sections of the XRT59L921 consists of the following blocks:

- The Receive Equalizer block
- The Peak Detector and Slicer block
- The LOS Detector block
- The Receive Output Interface block

2.1 Interfacing the Receive Sections to the Line (Transformer Coupling)

The design of each channel (within the XRT59L921) permits the user to transformer-couple the Receive Section to the line. Additionally, as mentioned earlier, the specification documents for E1 specify 75Ω termination loads, when transmitting over coaxial cable, and 120Ω loads, when transmitting over twisted-pair. Figure 9, and Figure 10 present the two methods that the user can employ in order to interface the Receivers (of the XRT59L921) to the line.

FIGURE 9. RECOMMENDED SCHEMATIC FOR INTERFACING THE RECEIVE SECTIONS OF THE XRT59L921 TO THE LINE FOR 75Ω APPLICATIONS (TRANSFORMER-COUPLING)

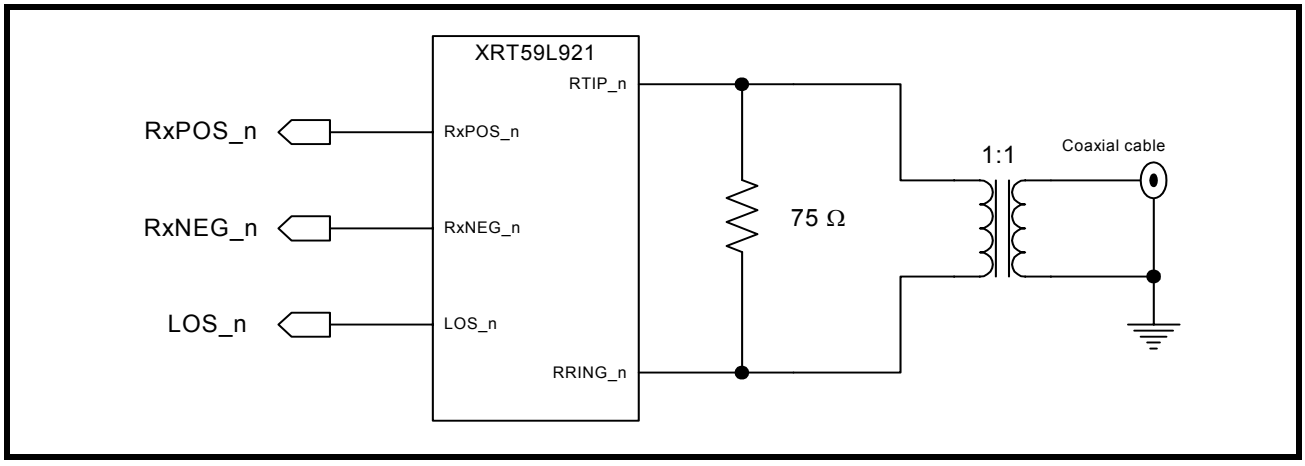
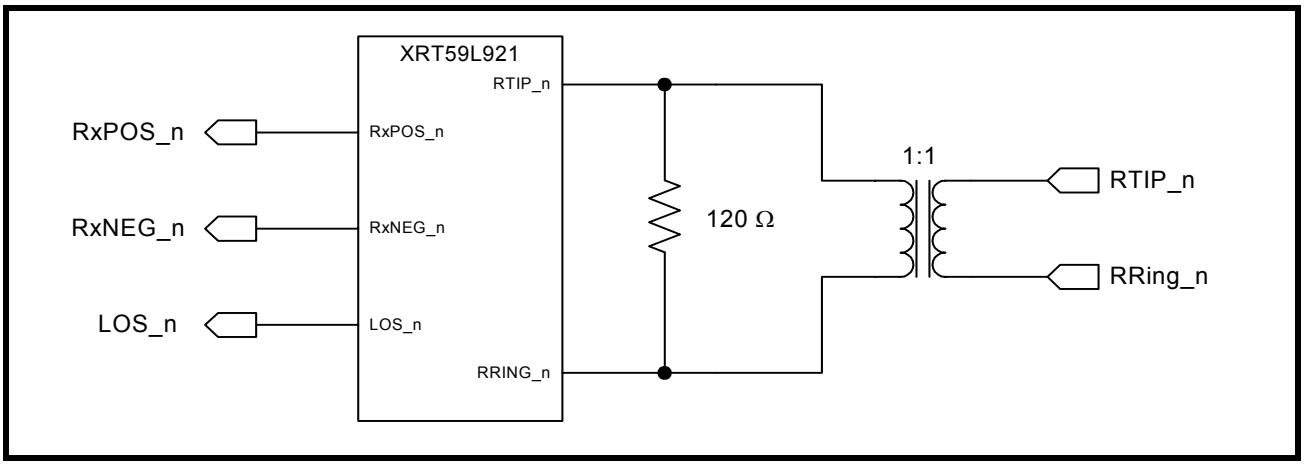


FIGURE 10. RECOMMENDED SCHEMATIC FOR INTERFACING THE RECEIVE SECTIONS OF THE XRT59L921 TO THE LINE FOR 120Ω APPLICATIONS (TRANSFORMER-COUPLING)



NOTE: ***Figure 9*** *and* ***Figure 10*** *indicate that the user should use a 1:1 transformer, when interfacing the receiver to the line.*

TRANSFORMER RECOMENDATION

RECEIVE TRANSFORMER RECOMMENDATIONS

PARAMETER	VALUE
Turns Ratio	1:1
Primary Inductance	
Isolation Voltage	
Leakage Inductance	

2.2 Interfacing the XRT59L921 Receive Section to the Line (Capacitive Coupling)

Figure 11 and Figure 12 are recommended methods to Interface the the receive sections of the XRT59L921to the line.

FIGURE 11. RECOMMENDED 75Ω CAPACITIVE COUPLING APPLICATION

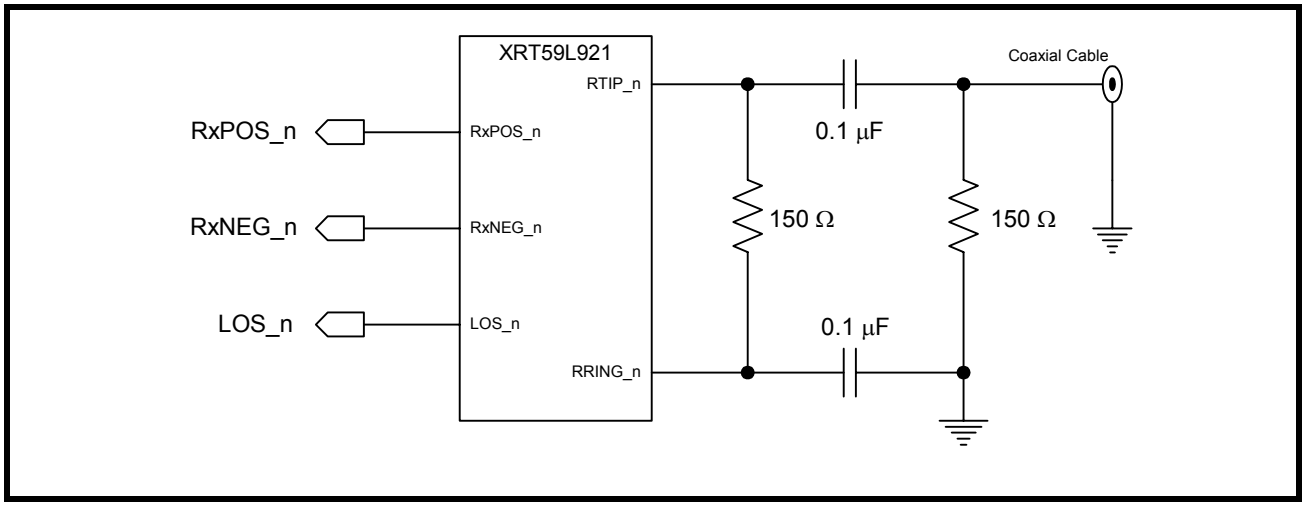
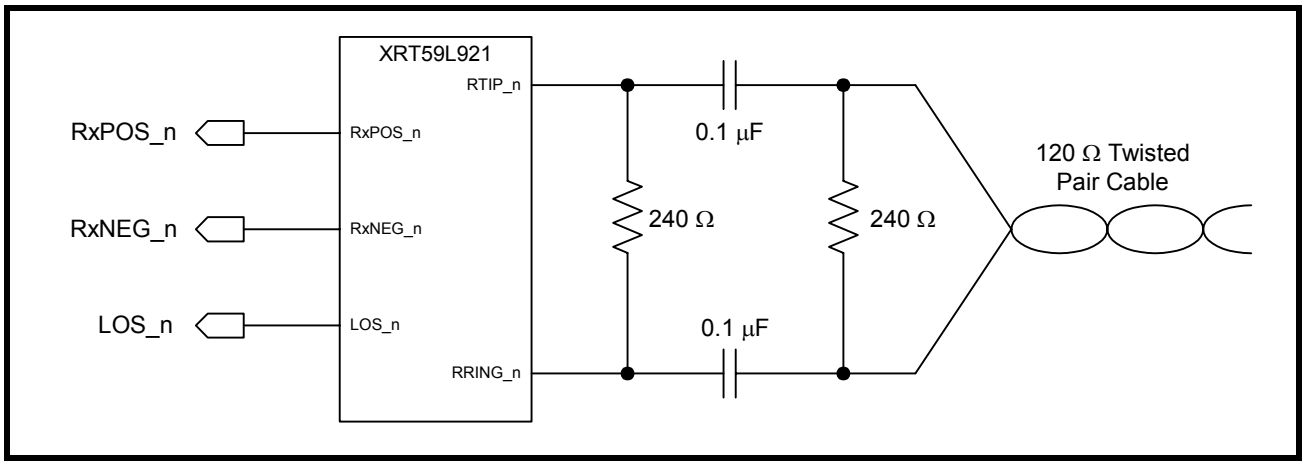


FIGURE 12. RECOMMENDED 120Ω TWISTED PAIR CAPACITIVE COUPLING APPLICATION



2.3 The Receive Equalizer Bock

After a given Channel (within the XRT59L921) has received the incoming line signal, via the RTIP_n and RRing_n input pins, the first block that this signal will pass through is the Receive Equalizer block.

As the line signal is transmitted from a given Transmitting terminal, the pulse shapes (at that location) are basically square. Hence, these pulses consist of a combination of low and high frequency Fourier components. As this line signal travels from the transmitting terminal (via the coaxial cable or twisted pair) to the receiving terminal, it will be subjected to frequency-dependent loss. In other words, the higher frequency components of the signal will be subjected to a greater amount of attenuation than the lower frequency components. If this line signal travels over reasonably long cable lengths, then the shape of the pulses (which were originally square) will be distorted and with inter-symbol interference increases.

The purpose of this block is to equalize the incoming distorted signal, due to cable loss. In essence, the Receive Equalizer block accomplishes this by subjecting the received line signal to frequency-dependent amplification (which attempts to counter the frequency-dependent loss that the line signal has experienced). By doing this, the Receive Equalizer is attempting to restore the shape of the line signal so that the received data can be recovered reliably.

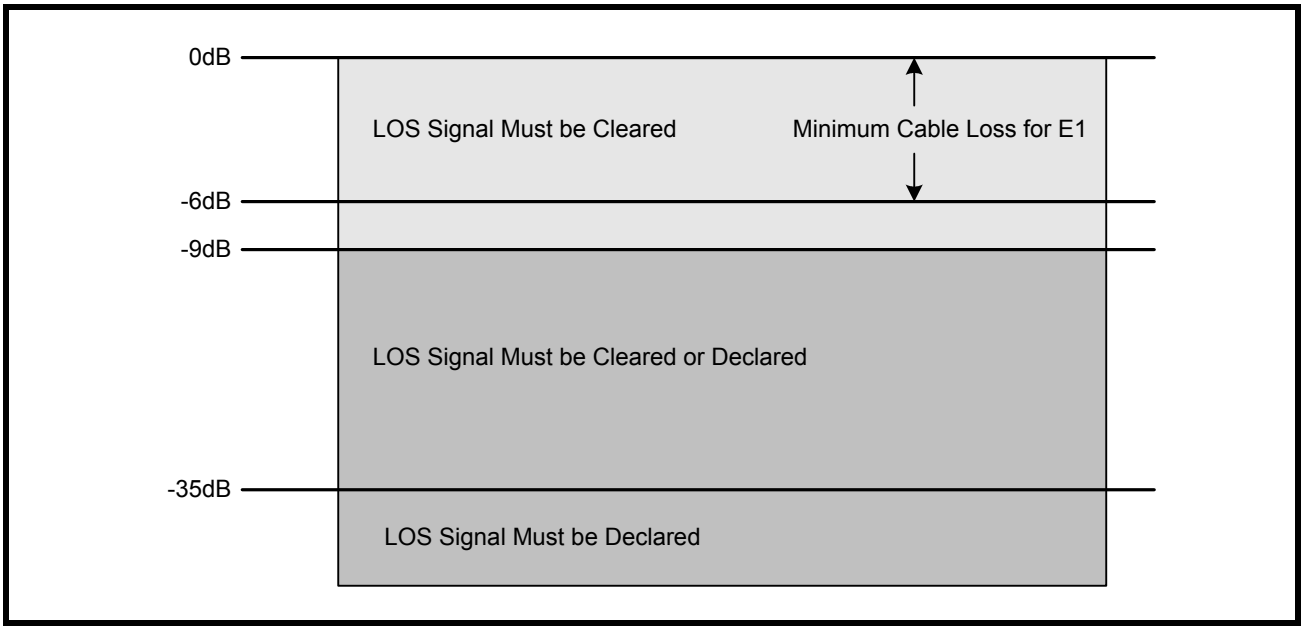
2.4 The Peak Detector and Slicer Block

After the incoming line signal has passed through the Receive Equalizer block, it will next be routed to the Slicer block. The purpose of the Slicer block is to quantify a given bit-period (or symbol) within the incoming line signal as either a “1” or a “0”.

2.5 The LOS Detector block

The LOS Detector block, within each channel (of the XRT59L921) was specifically designed to comply with the LOS Declaration/Clearance requirements per ITU-T G.775. As a consequence, the channel will declare a LOS Condition, (by driving the RxLOS output pin “High”) if the received line signal amplitude drops to –20dB or below. Further, the channel will clear the LOS Condition if the signal amplitude rises back up to –15dB or above. Figure 13 presents an illustration that depicts the signal levels at which a given channel (within the XRT59L921) will assert and clear LOS.

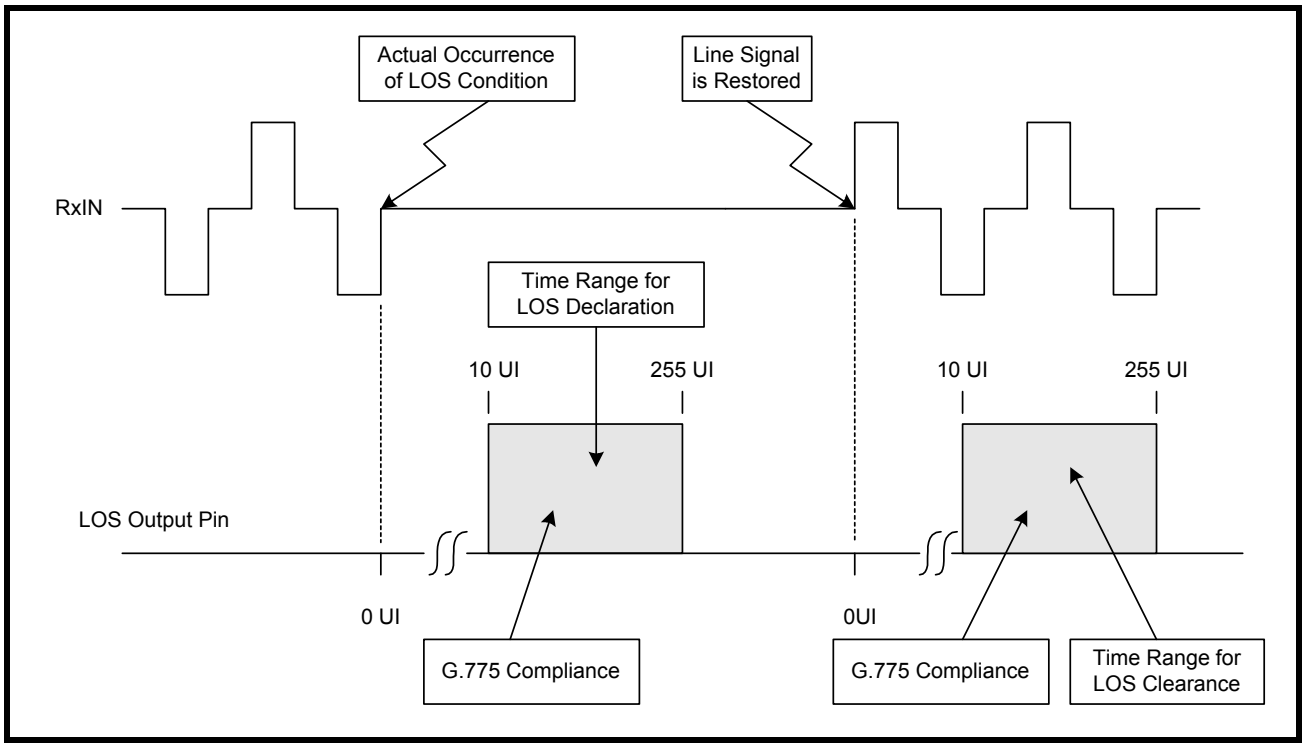
FIGURE 13. ILLUSTRATION OF THE SIGNAL LEVELS THAT THE RECEIVER SECTIONS (WITHIN XRT59L921) WILL DECLARE AND CLEAR LOS



Timing Requirements associated with Declaring and Clearing the LOS Indicator. The XRT59L921 was designed to meet the ITU-T G.775 specification timing requirements for declaring and clearing the LOS

indicator. In particular, the XRT59L921 will declare a LOS, between 10 and 255 UI (or E1 bit-periods) after the actual time the LOS condition occurred. Further, the XRT59L921 will clear the LOS indicator within 10 to 255 UI after restoration of the incoming line signal. Figure 14 illustrates the LOS Declaration and Clearance behavior, in response to first, the Loss of Signal event and then afterwards, the restoration of the signal.

FIGURE 14. THE BEHAVIOR OF THE LOS OUTPUT INDICATOR, IN RESPONSE TO THE LOSS OF SIGNAL, AND THE RESTORATION OF THE SIGNAL



2.6 LOS Mute Description

The LOSMute feature is included in the XRT59L921 such that when the input signal to a receiver is too low or is lost. The LOS_n pin will toggle "High" and at the same time the RPOS_n and RNEG_n outputs are muted to a "Zero" state to prevent output data chattering.

2.7 The Receive Output Interface block

The purpose of the Receive Output Interface block is to interface directly with the Receiving Terminal Equipment. The Receive Output Interface block outputs the data (which has been recovered from the incoming line signal) to the Receive Terminal Equipment via the RxPOS_n and RxNEG_n output pins.

If the Receive Sections of the XRT59L921 has received a Positive-Polarity pulse, via the RTIP_n and RRing_n input pins, then the Receive Output Interface will output a pulse via the RxPOS_n output pins.

Similarly, if the Receive Sections of the XRT59L921 has received a Negative-Polarity pulse, via the RTIP_n and RRing_n input pins, then the Receive Output Interface will output a pulse via the RxNEG_n output pins.

NOTE: *The Receive Output Interface block does not supply a recovered clock. This device is intended to be used in those applications, where the Clock Recovery circuit is realized in an ASIC solution.*

3.0 SHUTTING OFF THE TRANSMITTER

Each channel (within the XRT59L921) permits the user to shut off the Transmit Driver within their respective Transmit Section. This feature can come in handy for system redundancy design considerations or during diagnostic testing. The user can activate this feature by connecting the TxClk_n input pin to a logic “0” (e.g., GND) and continue to apply data via the TxPOS_n and TxNEG_n input pins.

FIGURE 15. TRANSMIT TIMING DIAGRAM

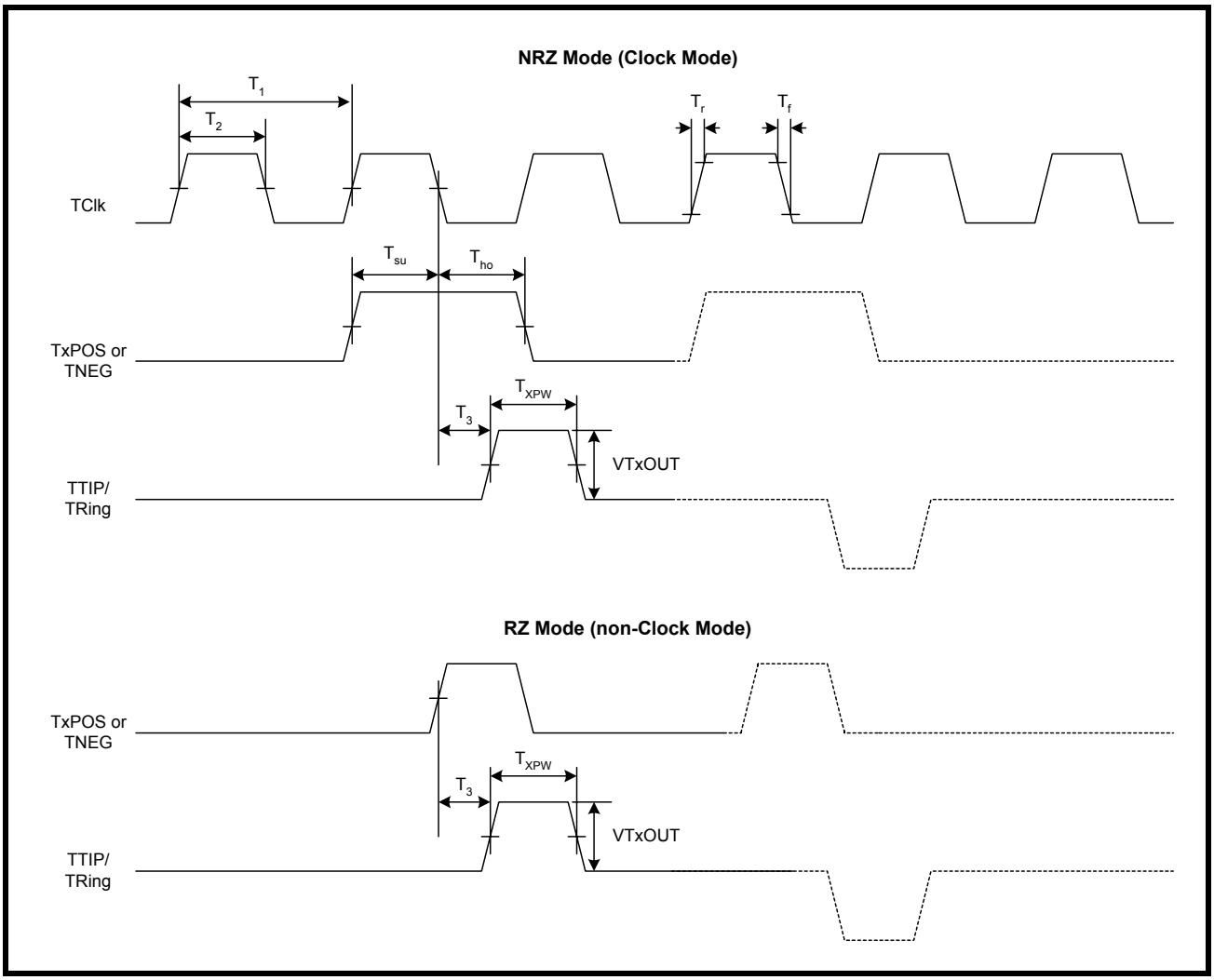
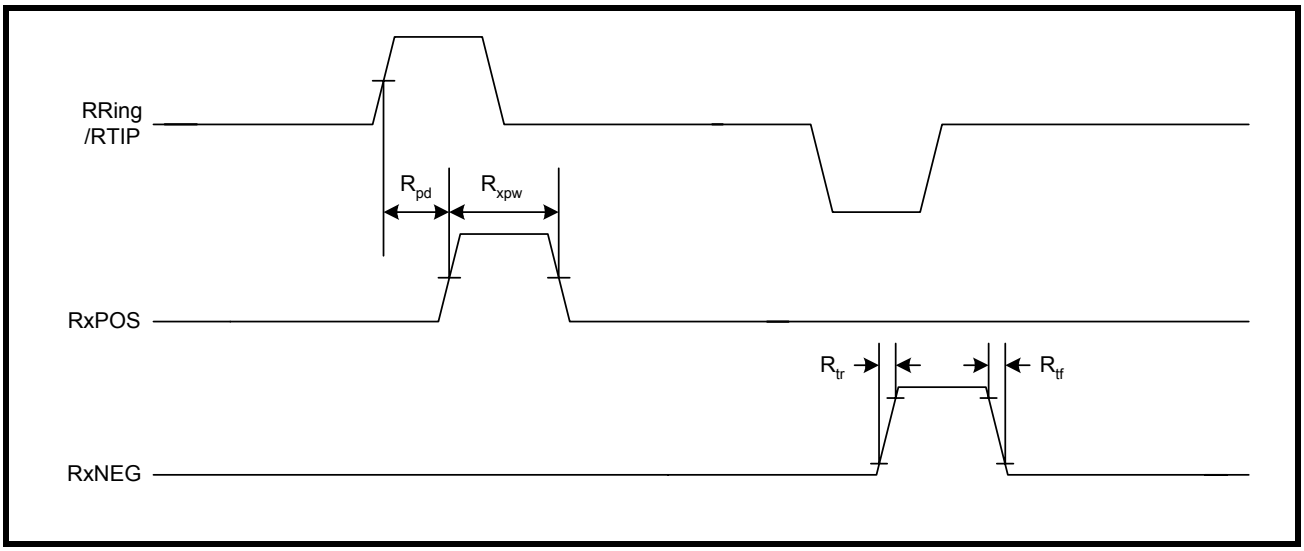


FIGURE 16. RECEIVE TIMING DIAGRAM



APPLICATION INFORMATION

Figure 17 and Figure 18, provide example schematics on how to interface Channel 1 of the XRT59L921 to the line, under the following conditions.

- Receiver is Transformer-coupled to a 75Ω unbalanced line.
- Receiver is Transformer-coupled to a 120Ω balanced line.

FIGURE 17. ILLUSTRATION ON HOW TO INTERFACE CHANNEL 1 (OF THE XRT59L921) TO THE LINE (RECEIVER IS TRANSFORMER-COUPLED TO A 75Ω UNBALANCED LINE)

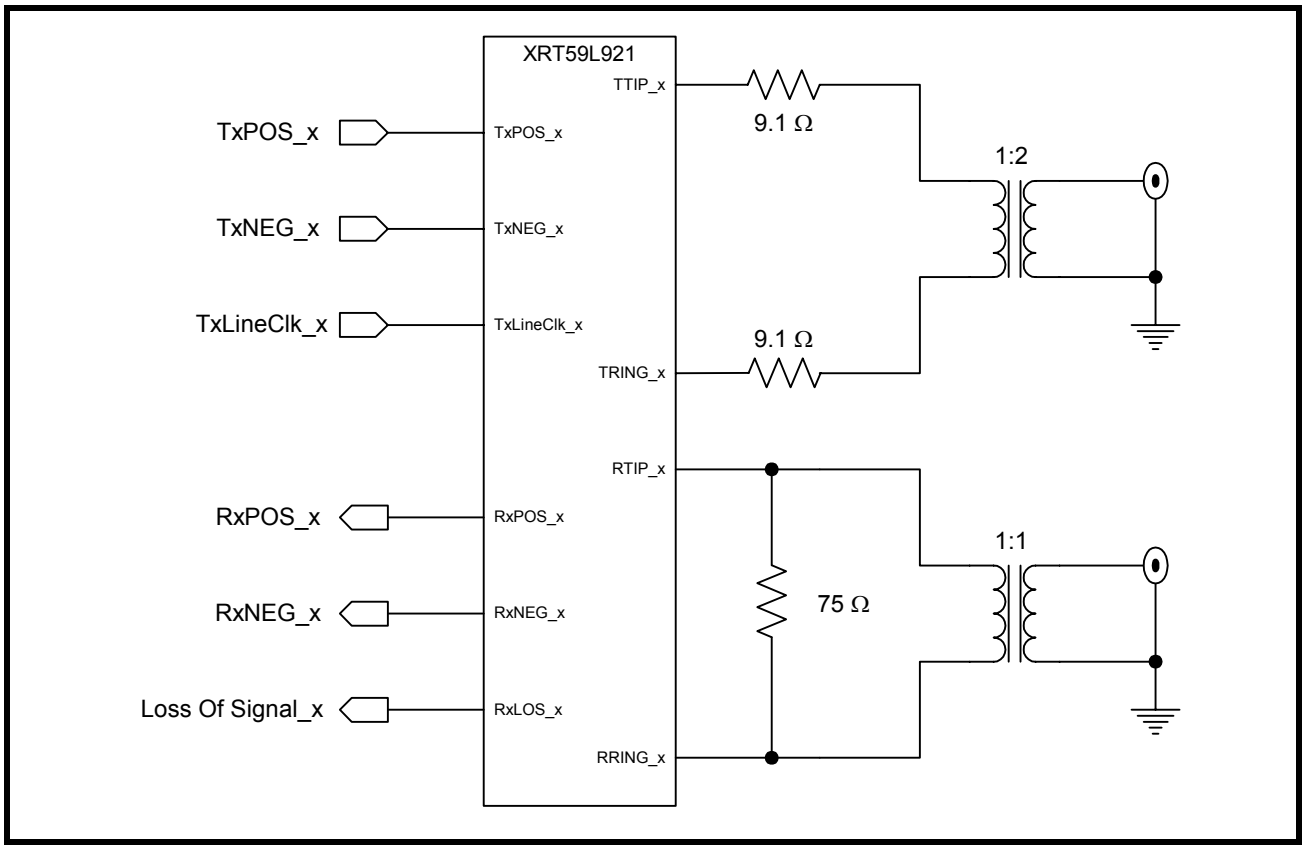
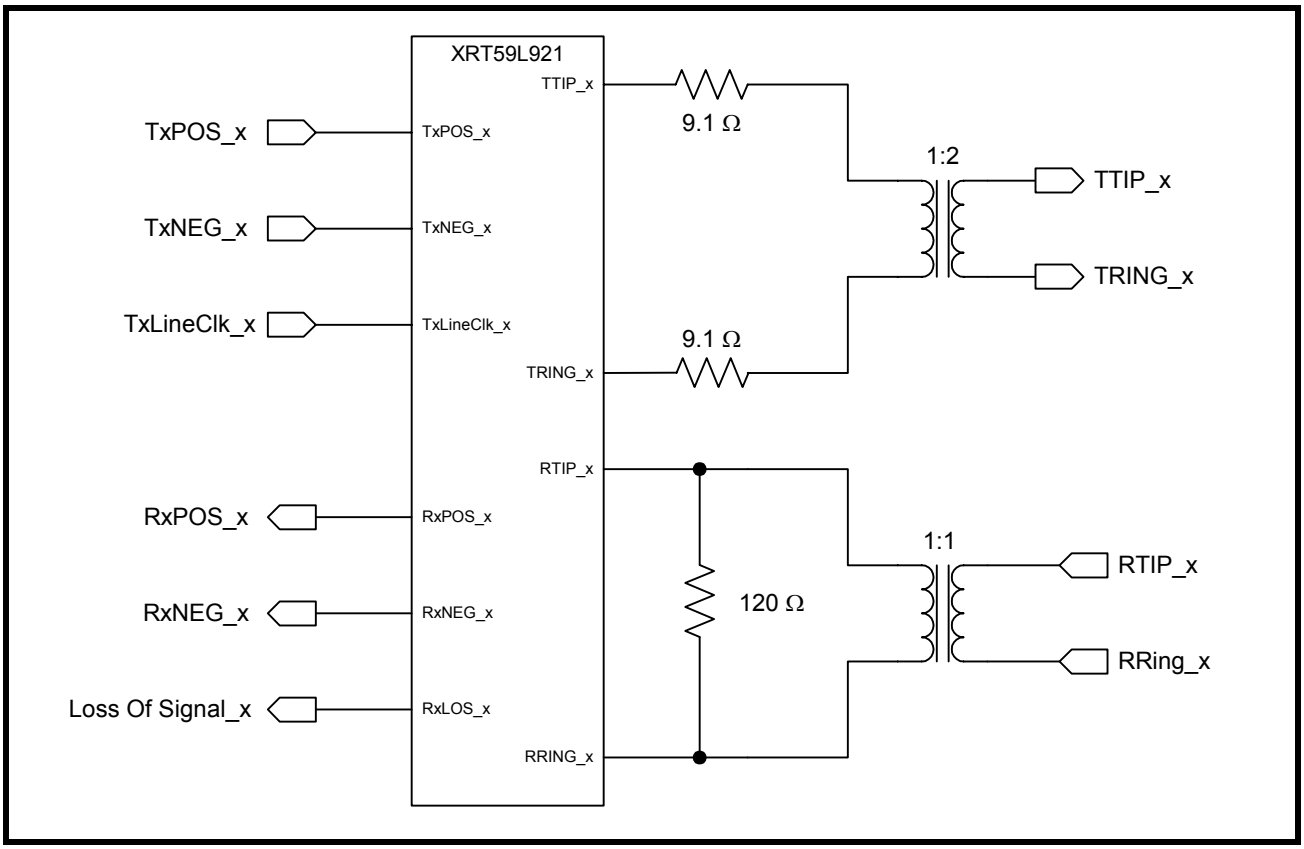


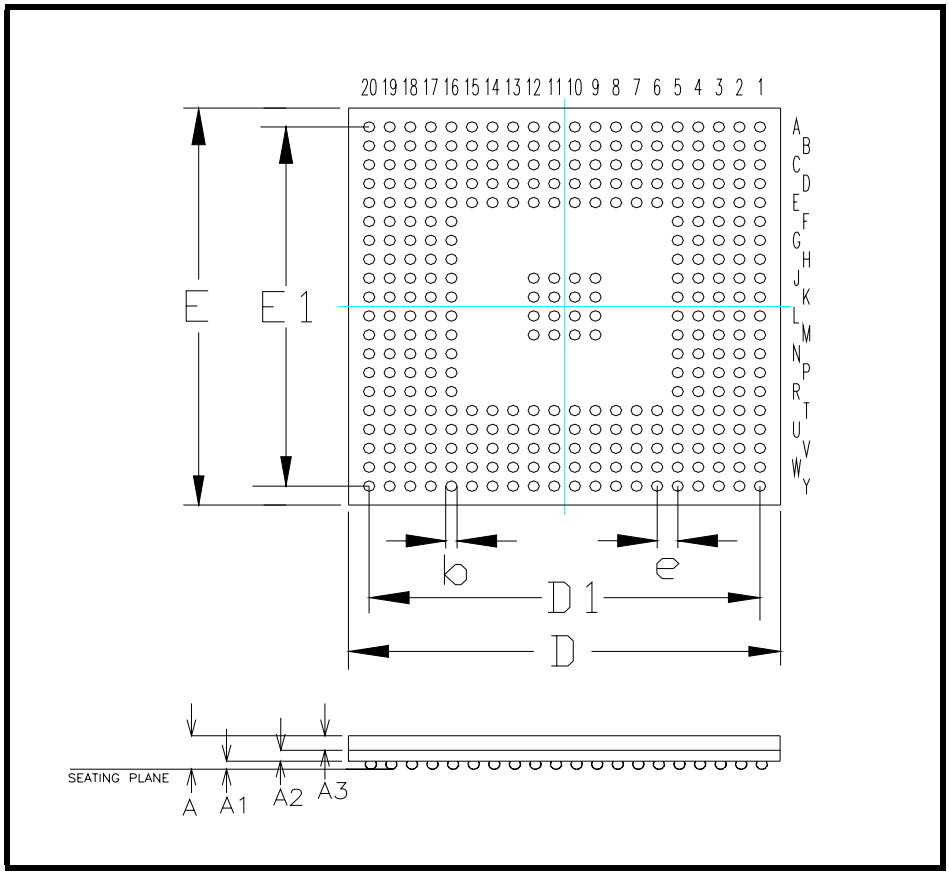
FIGURE 18. ILLUSTRATION ON HOW TO INTERFACE CHANNEL 1 (OF THE XRT59L921) TO THE LINE (RECEIVER IS TRANSFORMER-COUPLED TO A 120Ω BALANCED LINE)



ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT59L921IB	316 Shrink Thin Ball Grid Array (21.0 mm x 21.0 mm, STBGA)	-40^{0}C to +85^{0}C

PACKAGE DIMENSIONS



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.056	0.067	1.41	1.69
A1	0.011	0.015	0.28	0.38
A2	0.019	0.022	0.48	0.56
A3	0.026	0.030	0.65	0.75
D	0.819	0.835	20.80	21.20
D1	0.7480 BSC		19.00 BSC	
E	0.819	0.835	20.80	21.20
E1	0.7480 BSC		19.00 BSC	
b	0.018	0.022	0.45	0.55
e	0.0394 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	09/01/04	1st release of the XRT59L921 preliminary data sheet.
P1.0.1	10/28/04	CCorrected receive transformer turns ratio from 1:2 to 1:1. Added package outline drawing and pin numbers. Other minor edits
1.0.0	06/23/05	Replaced power supply current TBD's with actual. Release to production
1.1.0	09/07/05	Added comment to TxCLK pin description, added note to TxNEG pin description[, deleted "with -18db------" comment from electrical receiver sensitivity, minor edit to sect.1.2 and added sect. 1.2.2.
1.2.0	03/07/07	Added A2O, Y2, Y20 pins to positive supply. Added pins F1, F20, J1, J20, M1, M20, R1, R20 to digital ground. Added pins H16, P5, P16, P17 to AGND description.Added pin D15 to NC
1.2.1	03/12/07	Added pin V1 DGND in pin list.