T8533/34 Quad Programmable Line Card Signal Processor

Features

- Includes codec, termination impedance, and echo canceller in one device for line card applications
- Programmable μ-law, linear, or A-law PCM input and output (ITU-T G.712 compliant)
- Per-channel programmable gains
- Per-channel programmable internal termination impedance
- Per-channel 64-tap echo canceller (ITU-T G.168 compliant)
- Fully programmable time-slot assignment
- Analog and digital loopback test modes
- Serial microprocessor interface
- Sigma-delta converters with dither to reduce noise
- Six per-channel, bidirectional control pins for SLIC and line card function control (68-pin package)
- Quad design to minimize package count on dense line card applications
- Built-in level correction (transmit equalization) to accommodate current-sensing SLICs
- Single 5 V operation
- Available in 68-pin, 64-pin, and 44-pin packages

General Description

The quad programmable line card signal processor consists of four independent channels of codec and digital signal processing functions on one chip. In addition to the classic A-to-D and D-to-A conversion, the device includes termination impedance synthesis and a 64-tap echo canceller, functionally, on a per-channel basis. The device is capable of meeting all international standards for terminating impedance and digital encoding format. The processing circuitry for the adjustment of the transmit level (equalization) to accommodate current-sensing SLICs is also included.

The device is controlled by a serial microprocessor interface, and a set of bidirectional I/O pins are provided, on a per-channel basis, so that this control mechanism can be utilized to operate the battery feed device, ringing voltage switches, etc. Common data and clock paths can be shared over any number of devices. All the filter coefficients, signal processing, SLIC, and test features are accessible through this interface. This serial interface can be operated at speeds up to 4.096 Mbits/s.

The PCM bus is also programmable, with any channel capable of being assigned to any time slot. The PCM bus can be operated at speeds up to 16.384 Mbits/s, allowing for a maximum of 256 time slots. Separate transmit and receive interfaces are available for 4-wire bus designs, or they can be strapped together for a 2-wire PCM bus.

The device is available in 68-pin, 64-pin, and 44-pin surface-mount packages for economic use of board space.

Table of Contents

Functional Description

Refer to Figure 1 for the following discussion. (It should be noted that much of the processing is performed in a digital processor; thus, the actual data flow may be different than this functional, analog analogy based diagram shows.)
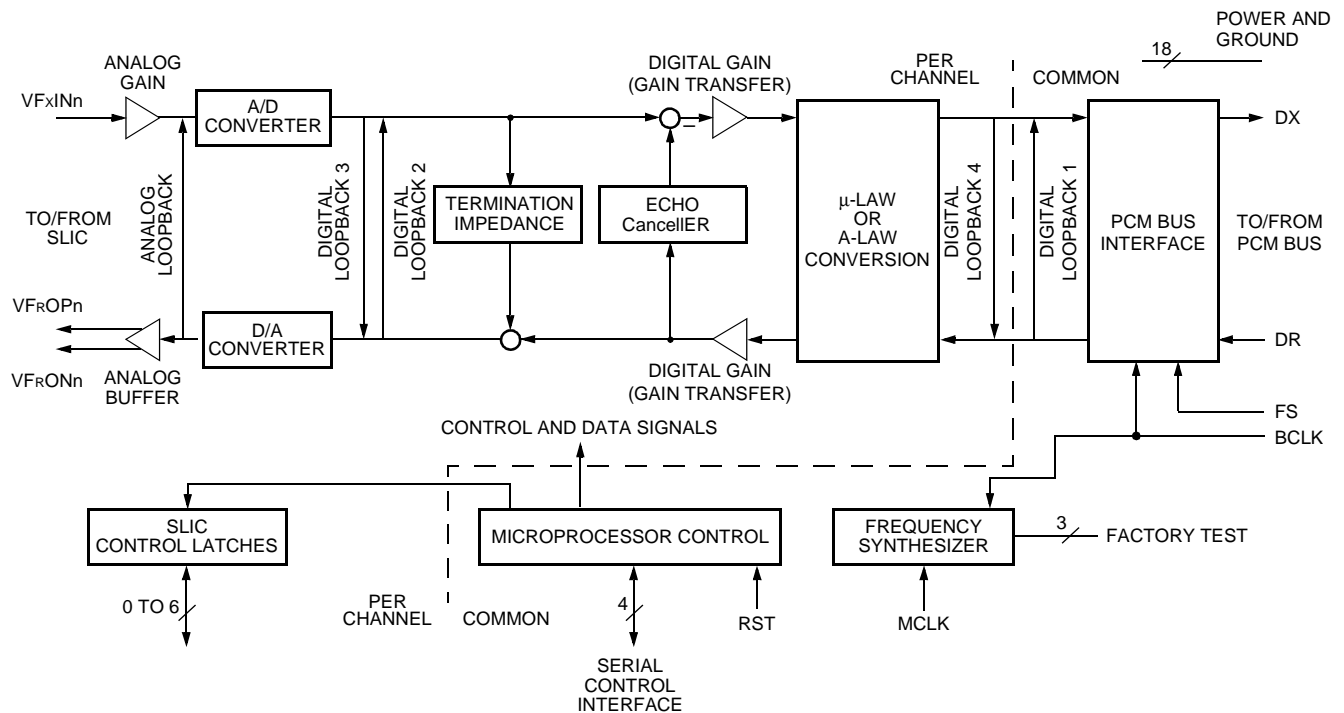
5-7172.ar5(F)

Figure 1. Functional Block Diagram, Each Section

This device performs virtually all the signal processing functions associated with a central office line termination. Functionality includes line termination impedance synthesis, adaptive or fixed hybrid balance (echo canceller), and level conversion both in the analog sense (transmit equalization), to accommodate various subscriber line interface circuits (SLICs), and in the digital sense, for adjustment of the levels on the PCM bus (gain transfer). In general, the termination impedance synthesis generates the equivalent of a circuit with the parallel combination of a capacitor and a resistor in series with a resistor or the parallel combination of a resistor and the series combination of a resistor and capacitor. These general forms of impedance characteristic will satisfy most of the requirements specified throughout the world. Programmable selection of either µ-law or A-law encoding further aids worldwide deployment. In addition to the programmable features for impedance and coding, the device also contains an echo canceller that meets international requirements for network echo cancellers. This includes the ability to automatically disable the adaptation in the presence of 2100 Hz modem tones. All coefficients used in the filtering algorithms can be computed off-line in advance and downloaded to the device at the time of powerup. All signal processing is contained within the device, and there are only three interfaces of consequence to the system designer: the SLIC interface, the PCM interface, and the control interface.

Functional Description (continued)

The SLIC interface is designed to be flexible and convenient to use with a variety of SLIC circuits. With an appropriate choice of SLIC, no external components are required in the interface, with the exception of a dc blocking capacitor in the transmit direction. In some cases, dc blocking capacitors in the receive direction may be necessary as well, since the device operates from a single 5 V supply.

The PCM bus interface is flexible in that it allows, independently, the transmit and receive data for any channel to be placed in any time slot. The bus can be operated at a maximum of a 16.384 Mbits/s rate to accommodate a maximum of 256 time slots. Separate pins are provided for each direction of transmission to allow 4-wire bus operation. The frame strobe signal is an 8 kHz signal that defines the beginning of the frame structure. The interface will count 8 bits per time slot and insert or read the data for each channel as programmed. Lower speeds of the PCM bus are allowed. The PCM clock must be synchronous with the master clock for the device (if present) and with the frame strobe signal.

The microprocessor control interface is a serial interface that uses the classic chip select type of operation. The interface controls the device by writing or reading various internal addresses. The command set comprises simple read and write operations, with the address determining the effect. All the memory locations, including the per-chip functions, are organized by channel, allowing a straightforward migration path to architectures other than quad.

There are several test modes included to facilitate confirmation of correct operation. In the signal path, both an analog and four digital loopback tests are available, while in the microprocessor interface, there is a write/read test mode that tests the operation of the memory. Use of external test access switches allows a complete test of the signal path through the line card so that correct operation of various operational modes can be verified.

Pin Information
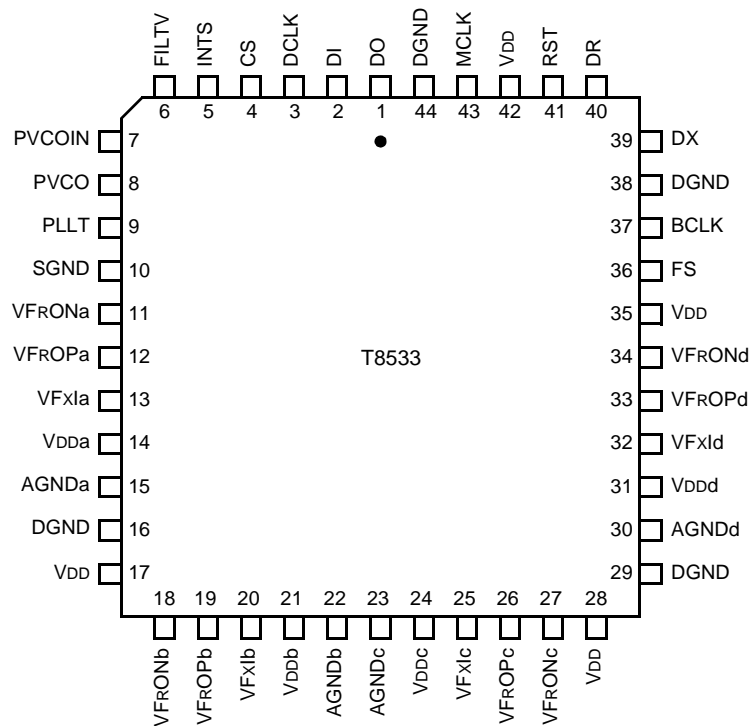
Figure 2. 44-Pin PLCC Pin Diagram

Table 1. Pin Assignments, 44-Pin PLCC, Per-Channel Functions

Ckt				Name	Type	Name/Description
a	b	c	d			
15	22	23	30	AGND	GND	**Analog Ground.** A common AGND, DGND, SGND plane is highly recommended.
14	21	24	31	V_{DD}	PWR	**5 V Analog Power Supply.**
13	20	25	32	VFxI	I	**Transmit Analog Input.** For complex terminations, this node requires a 10 MΩ or 20 MΩ resistance to AGND.
12	19	26	33	VFrOP	O	**Receive Analog Output, Positive Polarity.**
11	18	27	34	VFrON	O	**Receive Analog Output, Negative Polarity.**

Pin Information (continued)

Table 2. Pin Assignments, 44-Pin PLCC, Common Functions

Pin	Name	Type	Name/Description
1	DO	O	**Serial Data Output.** This is a 3-state output.
2	DI	I	**Serial Data Input.**
3	DCLK	I	**Serial Data Clock Input.**
4	CS	I	**Chip Select Input.** This pin determines the interval that the serial interface is active.
5	INTS	I	**Serial Interface Select.** Leaving this pin open places the serial interface in the normal mode; grounding it places the interface into the byte-by-byte mode. This pin has an internal pull-up.
6	FILTV	PWR	**Frequency Synthesizer Power (5 V).** This pin must be tied to V$_{DD}$.
7	PVCOIN	—	**Internal Test Point.** Do not connect to this pin.
8	PVCO	—	**Internal Test Point.** Do not connect to this pin.
9	PLLT	—	**Internal Test Point.** Do not connect to this pin.
10	SGND	GND	**Synthesizer Ground.** Connect to DGND. A common AGND, DGND, SGND plane is highly recommended.
16, 29, 38, 44	DGND	GND	**Digital Ground.** Logic ground and return for logic power supply. A common AGND, DGND, SGND plane is highly recommended.
17, 28, 35, 42	V$_{DD}$	PWR	**Digital Power Supply (5 V).**
36	FS	I	**PCM Frame Strobe Input.** This 8 kHz clock must be derived from the same source as BCLK. See the Clocking Considerations section.
37	BCLK	I	**PCM Clock Input.** This pin is used to develop internal clocks for certain clock rates. See the Clocking Considerations section.
39	DX	O	**PCM Bus Output Pin.** This is a 3-state output.
40	DR	I	**PCM Bus Input Pin.**
41	RST	I	**Power-On Reset.** A low causes a reset of the entire chip. This pin may be connected to DGND with a 0.1 µF capacitor for a power-on reset function, or it may be driven by external logic. This pin has an internal pull-up.
43	MCLK	I	**1.024 MHz Master Clock Input.** Internal timing is derived from this clock input for certain PCM bus rates. See Clocking Considerations. When unused, this pin may be left open. This pin has an internal pull-up.

Pin Information (continued)
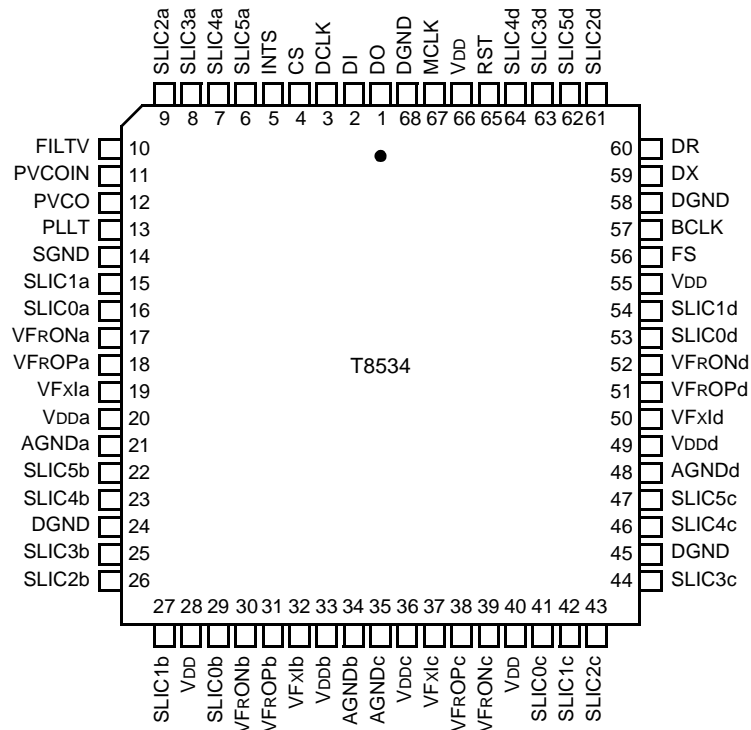
5-8194(F)

Figure 3. 68-Pin PLCC Pin Diagram

Table 3. Pin Assignments, 68-Pin PLCC, Per-Channel Functions

\multicolumn{4}{c}{Ckt}	Name	Type	Name/Description
a	b	c	d			
21	34	35	48	AGND	GND	**Analog Ground.** A common AGND, DGND, SGND plane is highly recommended.
20	33	36	49	V$_{DD}$	PWR	**5 V Analog Power Supply.**
19	32	37	50	VFxI	I	**Transmit Analog Input.** For complex terminations, this node requires a 10 MΩ or 20 MΩ resistance to AGND.
18	31	38	51	VF$_R$OP	O	**Receive Analog Output, Positive Polarity.**
17	30	39	52	VF$_R$ON	O	**Receive Analog Output, Negative Polarity.**
16	29	41	53	SLIC0	I/O	**SLIC Control Pin 0.**
15	27	42	54	SLIC1	I/O	**SLIC Control Pin 1.**
9	26	43	61	SLIC2	I/O	**SLIC Control Pin 2.**
8	25	44	63	SLIC3	I/O	**SLIC Control Pin 3.**
7	23	46	64	SLIC4	I/O	**SLIC Control Pin 4.**
6	22	47	62	SLIC5	I/O	**SLIC Control Pin 5.**

Pin Information (continued)

Table 4. Pin Assignments, 68-Pin PLCC, Common Functions

Pin	Name	Type	Name/Description
1	DO	O	**Serial Data Output.** This is a 3-state output.
2	DI	I	**Serial Data Input.**
3	DCLK	I	**Serial Data Clock Input.**
4	CS	I	**Chip Select Input.** This pin determines the interval that the serial interface is active.
5	INTS	I	**Serial Interface Select.** Leaving this pin open places the serial interface in the normal mode; grounding it places the interface into the byte-by-byte mode. This pin has an internal pull-up.
10	FILTV	PWR	**Frequency Synthesizer Power (5 V).** This pin must be tied to V_{DD}.
11	PVCOIN	—	**Internal Test Point.** Do not connect to this pin.
12	PVCO	—	**Internal Test Point.** Do not connect to this pin.
13	PLLT	—	**Internal Test Point.** Do not connect to this pin.
14	SGND	GND	**Synthesizer Ground.** Connect to DGND. A common AGND, DGND, SGND plane is highly recommended.
24, 45, 58, 68	DGND	GND	**Digital Ground.** Logic ground and return for logic power supply. A common AGND, DGND, SGND plane is highly recommended.
28, 40, 55, 66	V_{DD}	PWR	**Digital Power Supply (5 V).**
56	FS	I	**PCM Frame Strobe Input.** This 8 kHz clock must be derived from the same source as BCLK. See the Clocking Considerations section.
57	BCLK	I	**PCM Clock Input.** This pin is used to develop internal clocks for certain clock rates. See the Clocking Considerations section.
59	DX	O	**PCM Bus Output Pin.** This is a 3-state output.
60	DR	I	**PCM Bus Input Pin.**
65	RST	I	**Power-On Reset.** A low causes a reset of the entire chip. This pin may be connected to DGND with a 0.1 μF capacitor for a power-on reset function, or it may be driven by external logic. This pin has an internal pull-up.
67	MCLK	I	**1.024 MHz Master Clock Input.** Internal timing is derived from this clock input for certain PCM bus rates. See the Clocking Considerations section. When unused, this pin may be left open. This pin has an internal pull-up.

Pin Information (continued)

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Figure 4. 64-Pin TQFP Pin Diagram

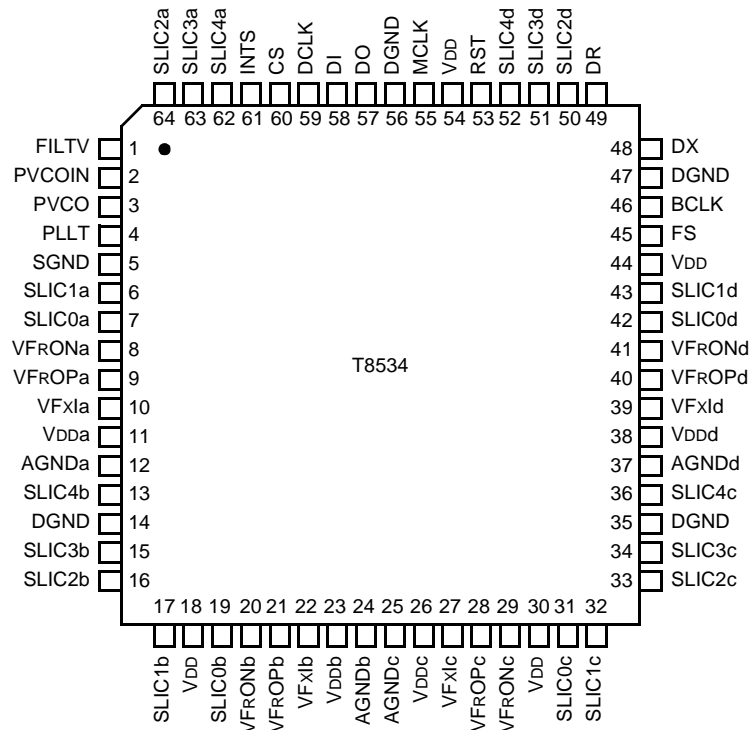**Table 5. Pin Assignments, 64-Pin TQFP, Per-Channel Functions**

Ckt				Name	Type	Name/Description
a	**b**	**c**	**d**			
12	24	25	37	AGND	GND	**Analog Ground.** A common AGND, DGND, SGND plane is highly recommended.
11	23	26	38	V$_{DD}$	PWR	**5 V Analog Power Supply.**
10	22	27	39	VF$_X$I	I	**Transmit Analog Input.** For complex terminations, this node requires a 10 MΩ or 20 MΩ resistance to AGND.
9	21	28	40	VF$_R$OP	O	**Receive Analog Output, Positive Polarity.**
8	20	29	41	VF$_R$ON	O	**Receive Analog Output, Negative Polarity.**
7	19	31	42	SLIC0	I/O	**SLIC Control Pin 0.**
6	17	32	43	SLIC1	I/O	**SLIC Control Pin 1.**
64	16	33	50	SLIC2	I/O	**SLIC Control Pin 2.**
63	15	34	51	SLIC3	I/O	**SLIC Control Pin 3.**
62	13	36	52	SLIC4	I/O	**SLIC Control Pin 4.**

Pin Information (continued)

Table 6. Pin Assignments, 64-Pin TQFP, Common Functions

Pin	Name	Type	Name/Description
1	FILTV	PWR	**Frequency Synthesizer Power (5 V).** This pin must be tied to V$_{DD}$.
2	PVCOIN	—	**Internal Test Point.** Do not connect to this pin.
3	PVCO	—	**Internal Test Point.** Do not connect to this pin.
4	PLLT	—	**Internal Test Point.** Do not connect to this pin.
5	SGND	GND	**Synthesizer Ground.** Connect to DGND. A common AGND, DGND, SGND plane is highly recommended.
14, 35, 47, 56	DGND	GND	**Digital Ground.** Logic ground and return for logic power supply. A common AGND, DGND, SGND plane is highly recommended.
18, 30, 44, 54	V$_{DD}$	PWR	**Digital Power Supply (5 V).**
45	FS	I	**PCM Frame Strobe Input.** This 8 kHz clock must be derived from the same source as BCLK. See the Clocking Considerations section.
46	BCLK	I	**PCM Clock Input.** This pin is used to develop internal clocks for certain clock rates. See the Clocking Considerations section.
48	DX	O	**PCM Bus Output Pin.** This is a 3-state output.
49	DR	I	**PCM Bus Input Pin.**
53	RST	I	**Power-On Reset.** A low causes a reset of the entire chip. This pin may be connected to DGND with a 0.1 µF capacitor for a power-on reset function, or it may be driven by external logic. This pin has an internal pull-up.
55	MCLK	I	**1.024 MHz Master Clock Input.** Internal timing is derived from this clock input for certain PCM bus rates. See the Clocking Considerations section. When unused, this pin may be left open. This pin has an internal pull-up.
57	DO	O	**Serial Data Output.** This is a 3-state output.
58	DI	I	**Serial Data Input.**
59	DCLK	I	**Serial Data Clock Input.**
60	CS	I	**Chip Select Input.** This pin determines the interval that the serial interface is active.
61	INTS	I	**Serial Interface Select.** Leaving this pin open places the serial interface in the normal mode; grounding it places the interface into the byte-by-byte mode. This pin has an internal pull-up.

Functional Description

Clocking Considerations

This device has several clock inputs for the various interfaces. The PCM bus uses BCLK as the bit clock and the one-going edge of FS to determine the location of the beginning of a frame. These two clocks must be derived from the same source. Internally, the device develops all the internal clocks with a phase-locked loop that uses BCLK as the timing source when BCLK is 16.384, 8.192, 4.096, 2.048, or 1.024 MHz. In these instances, MCLK is not used and may be left open since any signal driving MCLK is ignored. For BCLK rates of 256 kHz and 512 kHz, MCLK is used as a source for the PLL and must be 1.024 MHz. In this latter case, BCLK, MCLK, and FS must be derived from the same source and the rising edge of BCLK must be within 10 ns of the rising edge of MCLK. BCLK, FS, and MCLK (if required) must be continuously present and without gaps in order for the device to operate correctly. Note that the nominal values in Table 15 are the valid frequencies for BCLK.

DCLK is used to clock the internal serial interface and may be asynchronous to the other clocks. There is no need to derive this clock from the same source as the other clocks. The serial bus may be operated at any speed up to 4.096 Mbits/s. DCLK can be gapped, however additional clock cycles are required in and around the command frame to process data, and during and after a hardware or a software reset to ensure complete clearing of internal logic. There is no limit on the number of devices on the same serial bus.

The Control Interface

The device is controlled via a series of memory locations accessed by a serial data connection to the external master controller. This interface operates using the chip select lead to enable transmission of information. All chip functions are enabled or disabled by setting or clearing bits in the control memory. Filter coefficients and gain adjustments are also stored in this memory.

The codec has both a serial input lead and a serial output lead. These may be used individually for a 4-wire serial interface, or tied together for a 2-wire interface. The line driver circuitry is capable of driving relatively high currents so that in the event that the line is long enough to show significant transmission line effects, it can be terminated in the characteristic impedance at each end with resistors to Vcc and ground.

All data transfers on the serial bus are byte oriented with the least significant bit (shown in this data sheet as bit 0) transmitted first, followed by the more significant bits. For data fields, the least significant byte of the first data byte is transmitted first, followed by the more significant bytes, each byte transmitted LSB first. This format is compatible with the serial port on most microcontrollers.

Modes

There are two different modes of operation for the serial interface, the normal mode and the byte-by-byte mode. These two modes differ in the manner in which CS is used to control the transfer. Note that the CS lead is used to control the transfer of serial data from master controller to slave codec and in the reverse direction.

In normal mode, (INTS pin open) the CS lead must go low for the duration of the transfer. The only error check performed by the codec is to verify that CS is low for an integral number of bytes. Detection of an active (active-low) chip select for other than an integral multiple of 8 bits results in the operation being terminated. The next active excursion of chip select will be interpreted as a new command; hence, the serial I/O interface can always be initialized by asserting CS for a number of clock periods that is not an integral multiple of 8. CS is captured using DCLK, so DCLK must be transitioned to perform this initialization. Undefined command codes are reserved for future use and may cause unwanted operation of the device.

The byte-by-byte mode (INTS pin tied to ground) uses CS to control each byte of the transfer. In this mode, CS goes low for exactly 8 bits at a time, corresponding to a 1-byte transfer either to or from the codec chip. Repeated transitions of CS are used to control subsequent bytes of data to/from the codec. For a write command in this mode, CS must go low for each byte of the transfer until the transfer is complete. For a read command, CS will go low for each of the 3 bytes of the read command transferred to the device, then low again for each byte to be read. Notice that the total number of bytes transferred (and excursions on CS) is N + 3, where N is the number of bytes to be read in the command. This mode of operation is useful in cases where the master is a microprocessor with a built-in UART that transfers 1 byte at a time. Error detection is limited to detection of an active CS for other than an integral multiple of 8 bits. Recovery is the same as normal mode. Note that the clock phase is shifted in this mode.

Flow control can be accomplished by suspending the transitions on DCLK by holding either state. During the data transfer, CS must remain low while clock transitions are suspended with DCLK in either state.

Functional Description (continued)

The Control Interface (continued)

Protocol

The format of the command protocol is shown in Figures 5 and 6.

The control interface operates with one external master controller and multiple slave codec devices. Each transfer is initiated by the master, and the slave responds for either read operations or the fast scan mode. The slave does not check the bus for activity prior to transmitting; it only checks for an active CS. The master should allow for a wait between the end of a read command until CS becomes active for the read data. The master must refrain from sending additional commands to the slave chip until the response is received. On a 4-wire bus, commands to other devices may be initiated before the response is received, but care in generating the CS function is needed to ensure that the multiple responses do not interfere. It should be noted that multiple memory locations can be accessed in the same command by setting the data field length field to the desired number of bytes to be transferred. If flow control is desired, it must be performed by using separate commands, each transferring smaller blocks of information, or by controlling the serial clock (gapping the serial clock), or with CS in the case of byte-by-byte mode.

There is no response from the slave to the master for a write operation. The response to a read operation simply includes the data to be read in the data field. This data is sent least significant bit first, with the bytes sent in ascending sequence. Commands from the master controller include data for write operations, but not for read operations. Since the coefficients and gains are stored in volatile memory, all the coefficients and gains must be loaded after powerup. There is, however, no need to reload them when switching from active to standby modes, or vice versa. Great care should be exercised in loading memory when the codec channel is not in standby mode. Sudden changes in the termination or balance impedances can result in undesirable system operation.

All data is transmitted in a byte-oriented fashion with the least significant bit of each byte transferred first. Multibyte fields are transferred least significant byte first in both directions. The data field will contain the first addressed data location first, with subsequent data locations transmitted in ascending order.

Functional Description (continued)

The Control Interface (continued)

Protocol (continued)

LSB	MSB	LSB	MSB	LSB	MSB	LSB
COMMAND (8 bits)		START ADDRESS (8 bits)		DATA FIELD LENGTH (8 bits)		DATA FIELD (VARIABLE LENGTH) WRITE OPERATIONS ONLY

→ TIME

	7	6	5	4	3	2	1	0
	MSB							LSB
START ADDRESS:								

	7	6	5	4	3	2	1	0
	MSB							LSB
DATA FIELD LENGTH:								

	7	6	5	4	3	2	1	0
	MSB							LSB
COMMAND:	0*	0*	CKT SELECT		0	0	COMMAND	

CKT SELECT:		COMMANDS:	
CKT a:	00	FAST SCAN MODE:	10
CKT b:	01	WRITE MEMORY:	01
CKT c:	10	WRITE ALL CHANNELS:	11
CKT d:	11	READ MEMORY:	00

* Location of memory bank selection. All user controls are in memory bank 0; other memory banks contain internal state information for the device.

Note: Data field length is in bytes for all operations. All data is transmitted in bytes with the LSB for each byte transmitted first. For 16-bit memory operations, the least significant byte of the first memory location is transmitted first, followed by the most significant byte; each byte is transmitted LSB first. Additional memory locations are loaded in ascending sequence.

Figure 5. Command Frame Format, Master to Slave, Read or Write Commands

LSB

DATA FIELD (VARIABLE LENGTH) READ OPERATIONS ONLY

Note: All data is transmitted in bytes with the LSB for each byte transmitted first. For memory operations, the least significant byte of the first memory location is transmitted first, followed by the most significant byte, each byte transmitted LSB first. Additional memory locations are loaded in ascending sequence.

Figure 6. Command Frame Format, Slave to Master, Read Commands

Functional Description (continued)

The Control Interface (continued)

Write Command

A write command is used to write to the memory addresses. Figures 7—10 illustrate normal or byte-by-byte operation with continuous or gapped DCLKs. For gapped DCLK operation, transitions, not frequency, are critical (as long as transitions occur no faster than 122 ns apart).
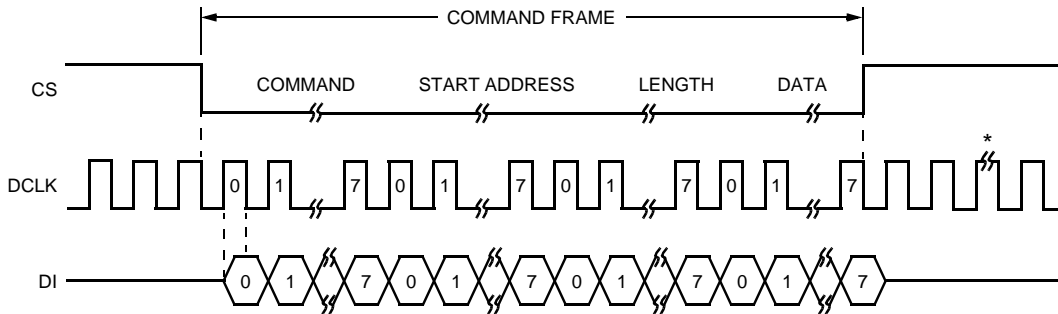
0078

* Two or more full DCLK cycles are required before the start of a new command frame.

Note: Data field length of 1 shown.

Figure 7. Write Operation, Normal Mode (Continuous DCLK)

0076

Notes:

Data field length of 1 shown.

CK1 through CK4 are additional DCLK pulses required to properly process the data.

CK3 and CK4 are not necessary if another command frame follows this sequence.

Figure 8. Write Operation, Normal Mode (Gapped DCLK)

Functional Description (continued)

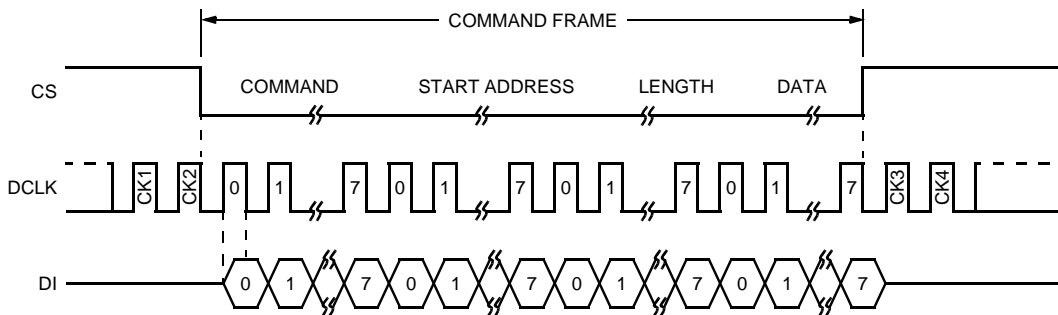## The Control Interface (continued)

Write Command (continued)

0074

* Two or more full DCLK cycles are required before the start of a new command frame.

Note: Data field length of 1 shown.

Figure 9. Write Operation, Byte-by-Byte Mode (Continuous DCLK)
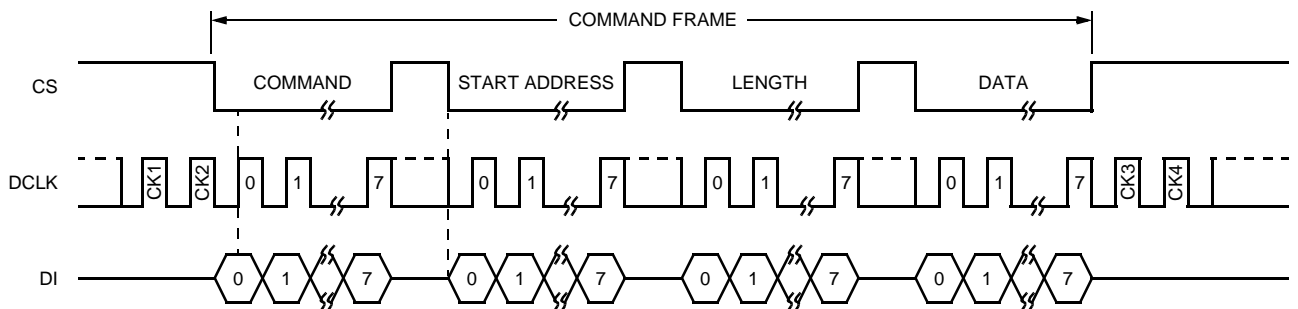
0072

Notes:

Data field length of 1 shown.

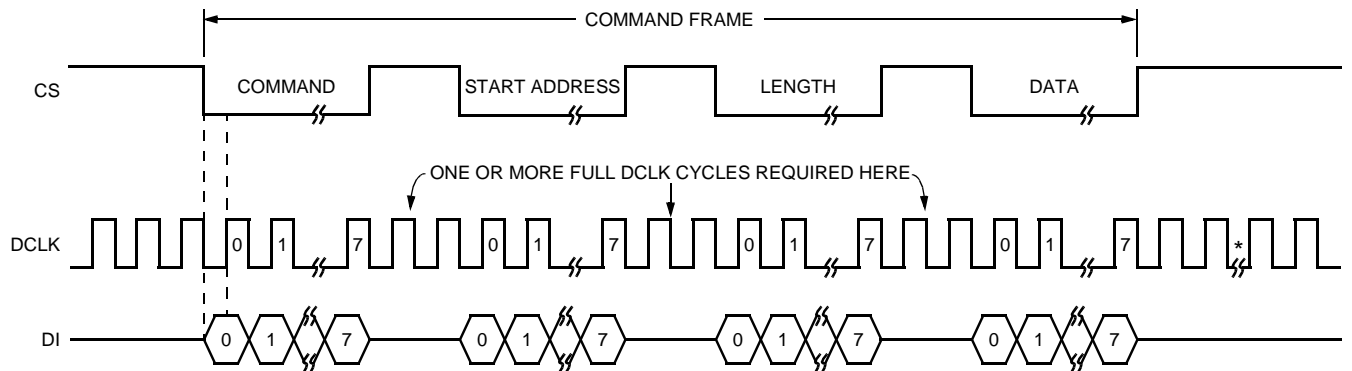CK1 through CK4 are additional DCLK pulses required to properly process the data.

CK3 and CK4 are not necessary if another command frame follows this sequence.

Figure 10. Write Operation, Byte-by-Byte Mode (Gapped DCLK)

Functional Description (continued)

The Control Interface (continued)

Read Command

The normal flow of information to the master controller is always in response to a read command. All control memory locations are accessed in 8-bit bytes. All read commands from the master controller require a response from the addressed codec. It is the responsibility of the master controller to ensure that only one device is transmitting on the serial interface line at any one time. The master controller also must ensure that the CS lead goes high after transferring the 3-byte sequence used to initiate the read, and then it goes low again for the response. In this case, it should be noted that the device expects the second time CS goes low that data is to be sent to the master; thus, it does not interpret the DI lead as containing a valid instruction during that CS excursion and a write during this time is not recommended. Note also that the CS lead must allow the number of bytes sent in a read command to be transferred before a subsequent command can be received by the codec. Figures 11—14 illustrate normal or byte-by-byte operation with continuous or gapped DCLKs. Like a write command, transitions, not frequency, are critical with regard to gapped DCLK operation.
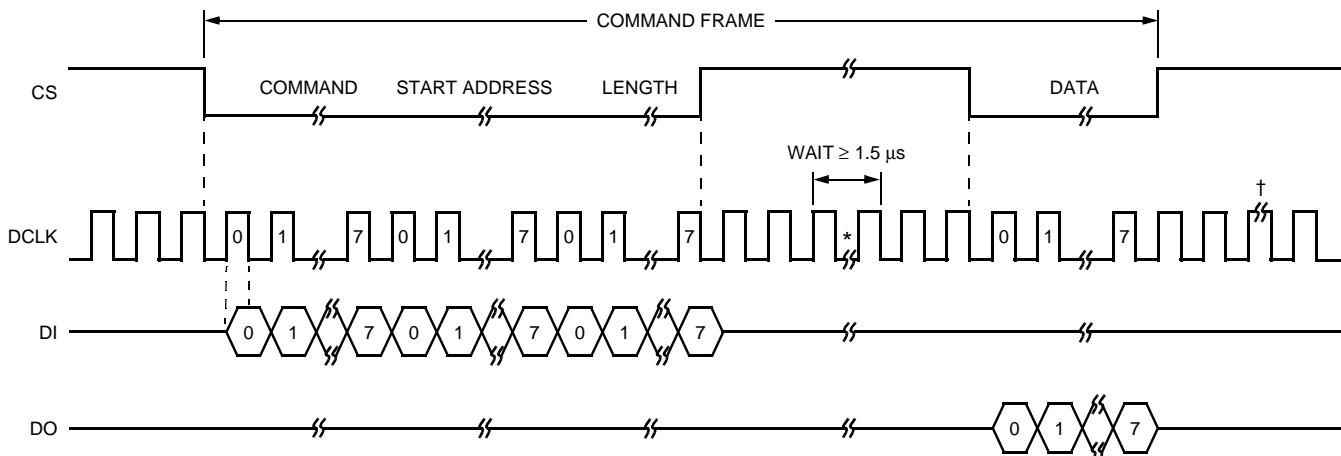
0079

* Provide sufficient wait time to access read data. Provide sufficient DCLK cycles to effectively wait ≥ 1.5 μs after the second full DCLK cycle and before the second to last full DCLK cycle. DCLK operation of 4.096 MHz would require 10 cycles of DCLK between LENGTH and DATA. The first two DCLK cycles, when CS goes high, processes the command. A wait is then required to access the read data. Two final DCLK cycles are required to process the read data.

† Two or more DCLK cycles are required before the start of a new command frame.

Note: Data field length of 1 shown.

Figure 11. Read Operation, Normal Mode (Continuous DCLK)

Functional Description (continued)

The Control Interface (continued)

Read Command (continued)
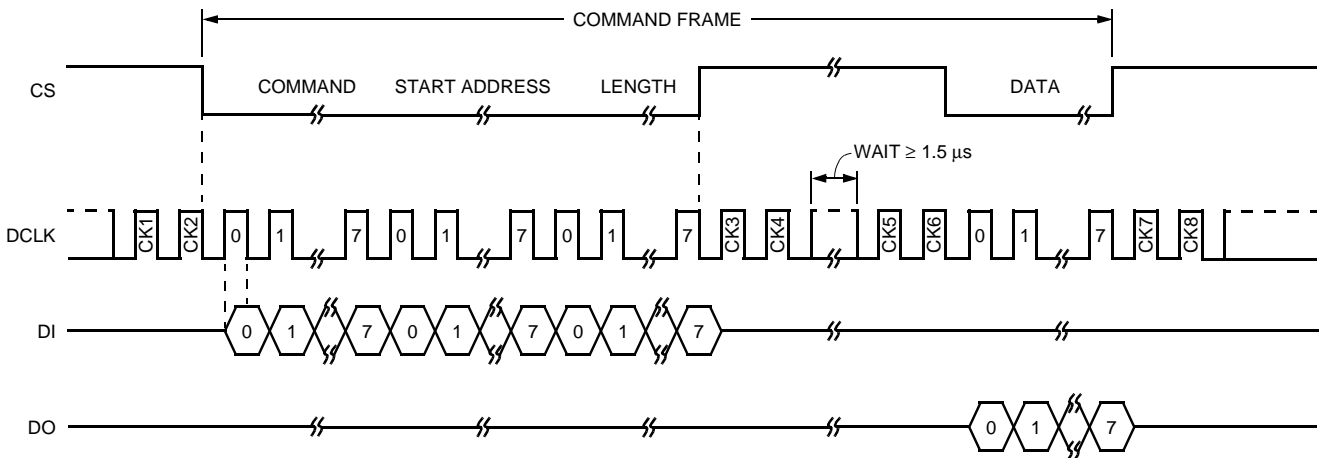
0077

Notes:

Data field length of 1 shown.

CK1 through CK8 are additional DCLK pulses required to properly process the data.

CK7 and CK8 are not necessary if another command frame follows this sequence.

Figure 12. Read Operation, Normal Mode (Gapped Clock)

Functional Description (continued)

The Control Interface (continued)

Read Command (continued)
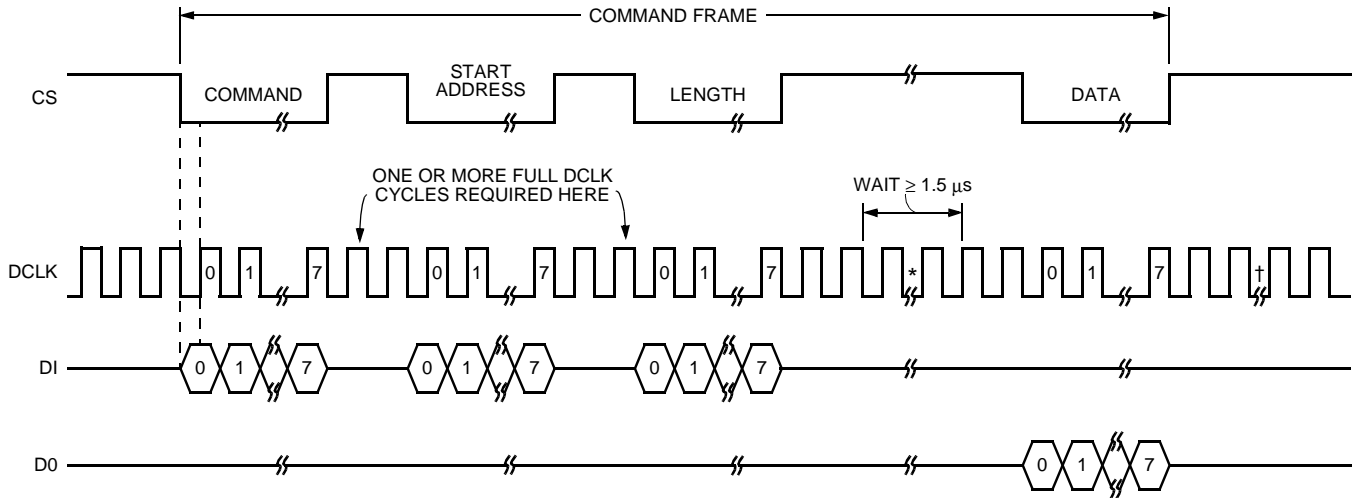
0075

* Provide sufficient wait time to access read data. Provide sufficient DCLK cycles to effectively wait $\geq$ 1.5 μs after the second full DCLK cycle and before the second to last full DCLK cycle. DCLK operation of 4.096 MHz would require 10 cycles of DCLK between LENGTH and DATA. The first two DCLK cycles, when CS goes high, processes the command. A wait is then required to access the read data. Two final DCLK cycles are required to process the read data.

† Two or more DCLK cycles are required before the start of a new command frame.

Note: Data field length of 1 shown.

Figure 13. Read Operation, Byte-by-Byte Mode (Continuous DCLK)

Functional Description (continued)

The Control Interface (continued)

Read Command (continued)
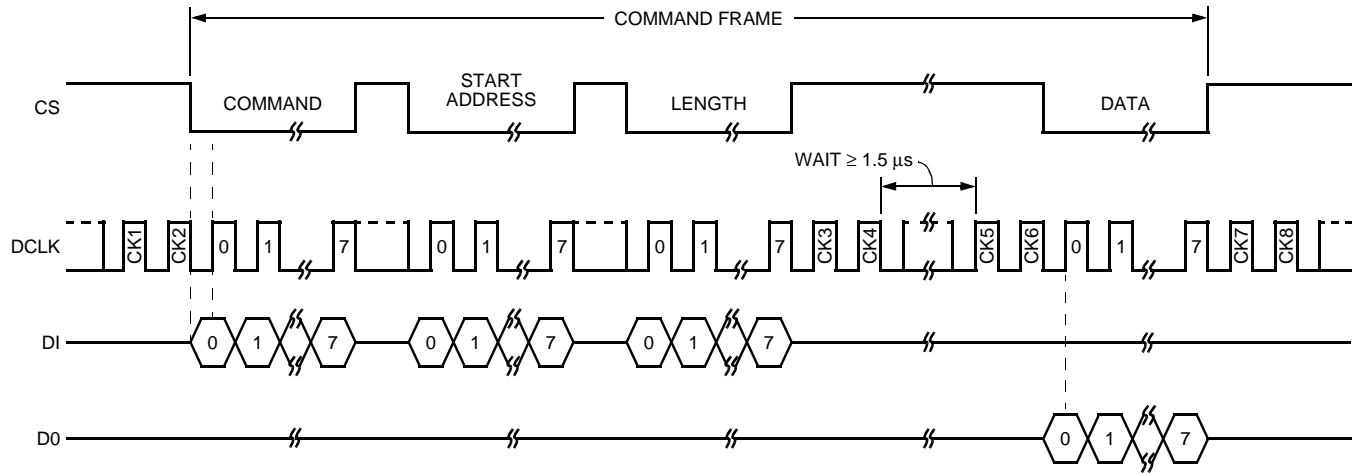
Notes:

Data field length of 1 shown.

CK1 through CK8 are additional DCLK pulses required to properly process the data.

CK7 and CK8 are not necessary if another command frame follows this sequence.

Figure 14. Read Operation, Byte-by-Byte Mode (Gapped DCLK)

Functional Description (continued)

The Control Interface (continued)

Fast Scan Mode

The fast scan mode allows a single byte command to read two SLIC control leads for all four channels with a 1-byte reply. This mode significantly speeds up the normal scanning for off-hook, ring trip, and ring ground detection. This special command sequence allows the controlling microprocessor to fast scan 2 bits in the SLIC control byte of each of the four channels. The command code is $(00000010)_2$, there are no start address or length fields. The command returns only a single byte of data, formatted as shown in Table 9.

Table 7. Bit Assignments for Fast Scan Mode

Bit	Reported Status
0 (LSB)	Channel 0, bit 0 (ckt a, address 160, bit 0)
1	Channel 0, bit 1 (ckt a, address 160, bit 1)
2	Channel 1, bit 0 (ckt b, address 160, bit 0)
3	Channel 1, bit 1 (ckt b, address 160, bit 1)
4	Channel 2, bit 0 (ckt c, address 160, bit 0)
5	Channel 2, bit 1 (ckt c, address 160, bit 1)
6	Channel 3, bit 0 (ckt d, address 160, bit 0)
7 (MSB)	Channel 3, bit 1 (ckt d, address 160, bit 1)

The circuit select in the command structure (Figure 5) is not used for this special single-byte command. The rules for toggling chip select apply as for the read command. Figures 15—18 illustrate normal or byte-by-byte operation with continuous or gapped DCLKs.

* Provide sufficient wait time to access read data. Provide sufficient DCLK cycles to effectively wait ≥ 1.5 µs after the second full DCLK cycle and before the second to last full DCLK cycle. DCLK operation of 4.096 MHz would require 10 cycles of DCLK between COMMAND and DATA. The first two DCLK cycles, when CS goes high, processes the command. A wait is then required to access the read data. Two final DCLK cycles are required to process the read data.

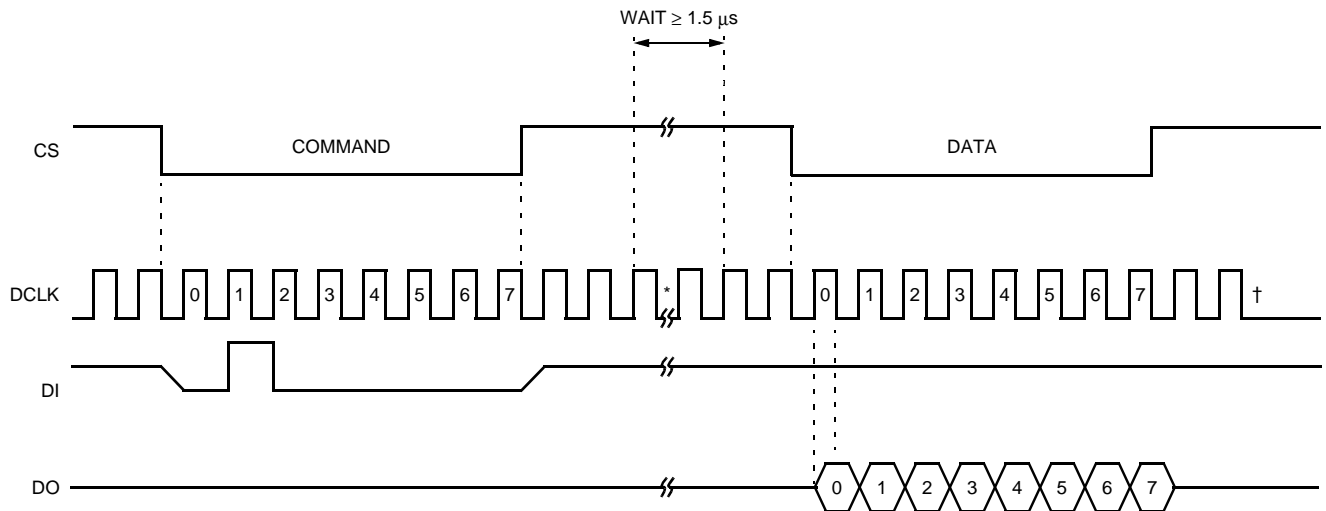† Two or more DCLK cycles are required before the start of a new command frame.

Figure 15. Fast Scan, Normal Mode (Continuous DCLK)

Functional Description (continued)

The Control Interface (continued)

Fast Scan Mode (continued)
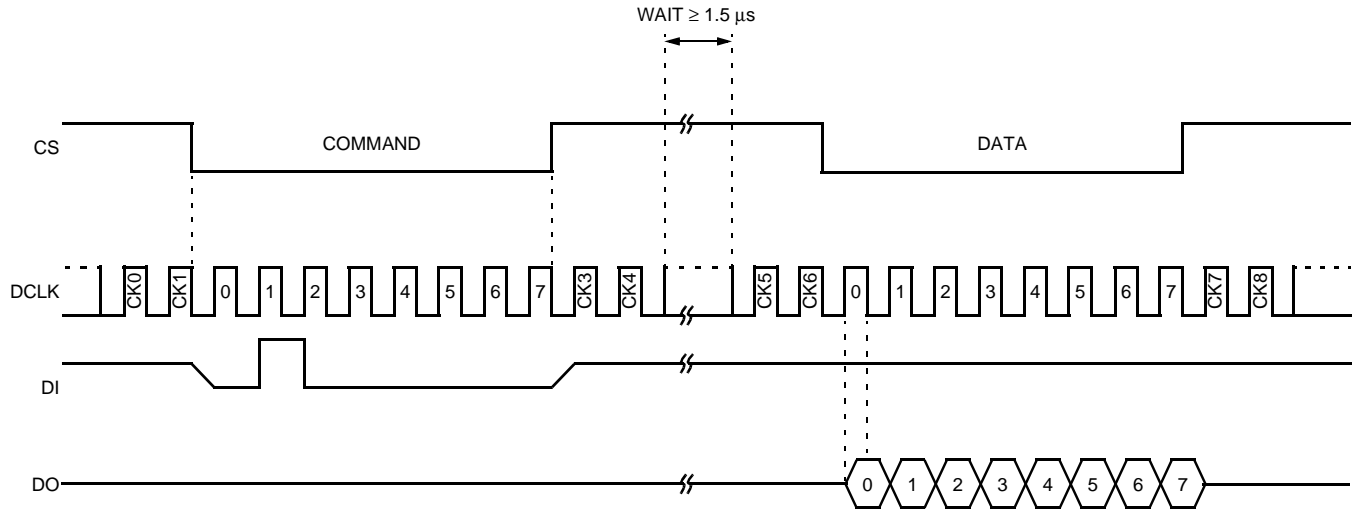
Note: CK1 through CK8 are additional DCLK pulses required to properly process the data.

Figure 16. Fast Scan, Normal Mode (Gapped DCLK)

Functional Description (continued)

The Control Interface (continued)

Fast Scan Mode (continued)

0124e

* Provide sufficient wait time to access read data. Provide sufficient DCLK cycles to effectively wait ≥ 1.5 μs after the second full DCLK cycle and before the second to last full DCLK cycle. DCLK operation of 4.096 MHz would require 10 cycles of DCLK between COMMAND and DATA. The first two DCLK cycles, when CS goes high, processes the command. A wait is then required to access the read data. Two final DCLK cycles are required to process the read data.

† Two or more DCLK cycles are required before the start of a new command frame.

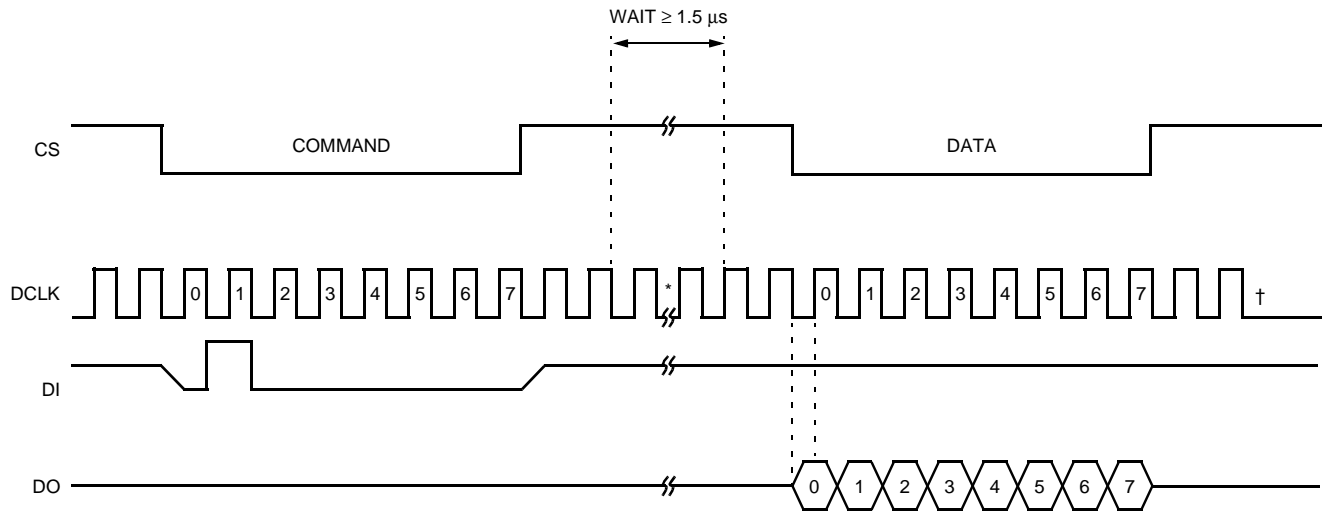**Figure 17. Fast Scan, Byte-by-Byte Mode (Continuous DCLK)**
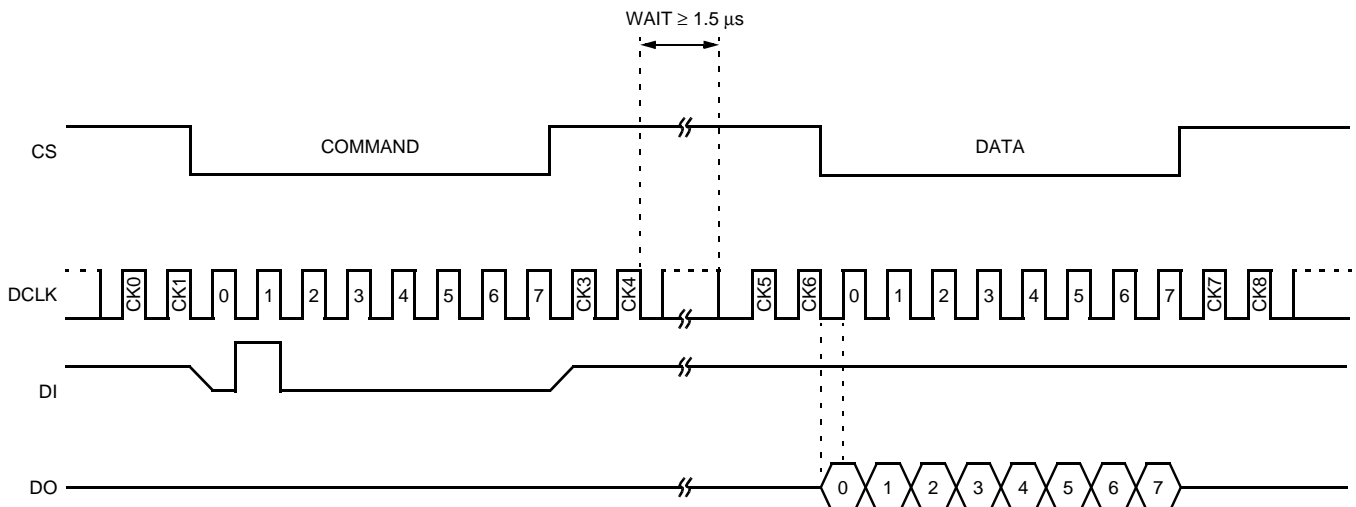
0126f

Note: CK1 through CK8 are additional DCLK pulses required to properly process the data.

Figure 18. Fast Scan, Byte-by-Byte Mode (Gapped DCLK)

Agere Systems Inc.

Functional Description (continued)

The Control Interface (continued)

Write All Channels

The write all channels command causes all four channels to be loaded with the same coefficients with a single data transfer from the master controller. This allows for a faster initialization of the device after a powerup. This command should be used with caution since it affects all four channels. The normal memory write and read commands affect only one channel.

Reset Functionality
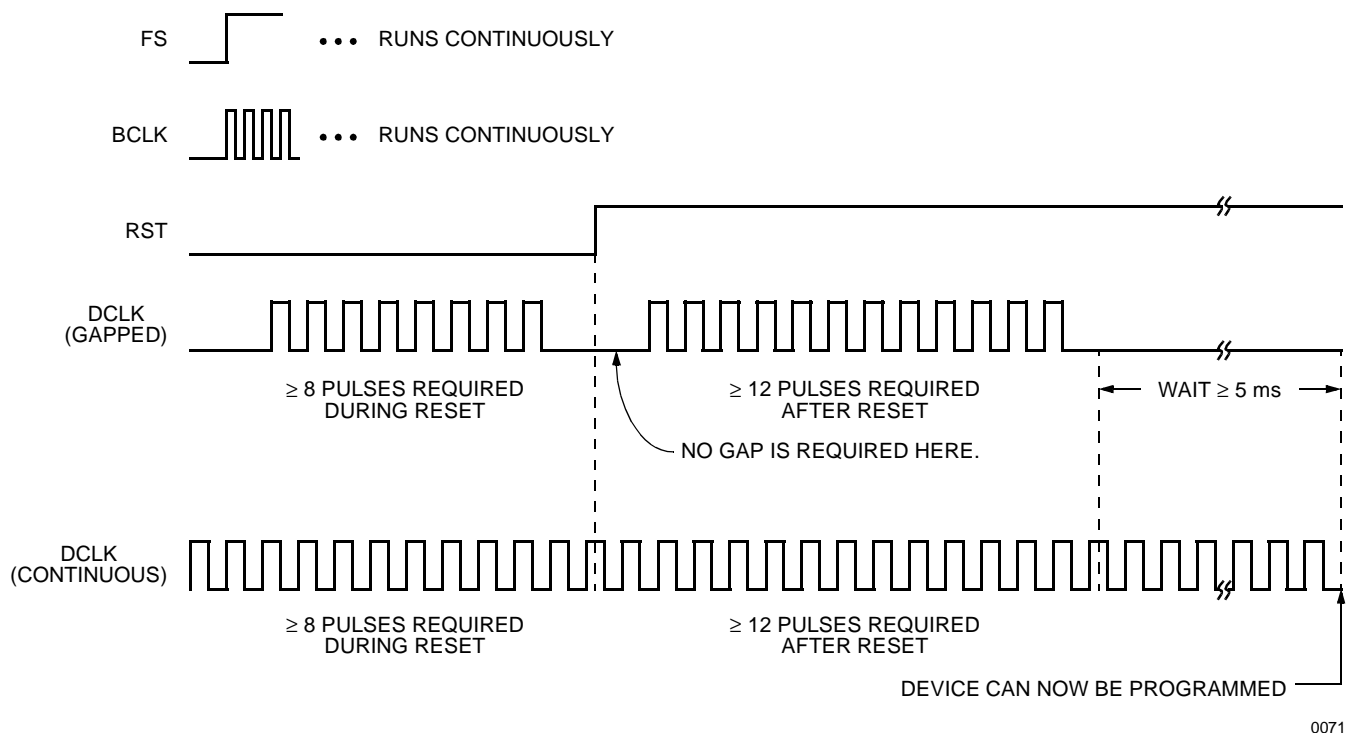
Figure 19. Hardware Reset Procedure

The reset function allows the internal logic of the device to be set to a known initial condition, either externally by activating the reset lead, or on a per-channel basis through the microprocessor interface by setting and then clearing bits, if required, in address RESCTRL (address 128). These two reset functions have different effects, and each of the software reset functions is a subset of the hardware reset functionality. The primary difference is in the treatment of the internal memory. The hardware reset is assumed to be a result of a catastrophic hardware event, such as a loss of power or an initial powerup. Accordingly, the assumption is made that the internal memory does not contain valid data, and default values for all memory locations are loaded. A software reset, however, can only be initiated if the device is operational (at least the microprocessor interface), so the contents of the memory may indeed be valid; thus, the resets may be more specific. Additionally, software resets only affect the selected channel.

Functional Description (continued)

Reset Functionality (continued)

A 0.1 µF capacitor between the RST lead and ground
will effectively hold the lead low long enough to reset
the device on powerup, allowing for a cost-effective
power-on reset function. Notice that the memory must
be reloaded through the serial interface after a hard-
ware reset function. For proper operation, it is neces-
sary for FS and BCLK to be present and stable during
a reset. DCLK transitions (frequency is not critical as
long as the maximum rate is not exceeded) are also
required in order for all internal logic to be properly
cleared as is a wait period for the internal PLL to stabi-
lize. See the timing diagram shown in Figure 19 for the
proper hardware or power-on reset procedure.

For a software reset, the control memory should not be
accessed for a minimum of 256 µs following the reset.

Memory Control Mapping

Several memory locations are used to control the
device. The Software Interface tables (Table 17, Mem-
ory Mapping and Table 18, Control Bit Definition) show
the memory assignments that are useful in call pro-
cessing and system testing. It should be noted that
other memory locations are used by the device to hold
intermediate results and other device state information.
Writing to these other locations can cause serious dis-
ruptions in the operation of the device and should be
avoided.

Standby Mode

The device enters a low-power standby mode with
powerup or software reset, or by programming the
CHACTIVE register 129, bit 0. In standby mode, the
control interface is active, capable of writing or reading
registers. SLIC read and write data latches are also
active. Analog signals at VFxI and PCM signals at DR
are ignored in this mode. BCLK must be present for
proper standby mode operation.

Test Capabilities

The device has several built-in test capabilities that can
be used to verify correct operation of the signal pro-
cessing of the line card. These test functions are
accessed in several different control addresses. Five
loopback modes are employed (the first four in the list
below are digital loopbacks):

Digital 1. Allows the digital signal from the PCM bus
to be looped back to the PCM bus. This
loopback facility can be used to verify cor-
rect operation of the PCM bus interface
logic, as well as operation of the PCM
bus.

Digital 2. Allows complete testing of the digital pro-
cessing capability of the codec by looping
the data back at the analog/digital conver-
sion interface.

Digital 3. This loopback function is at the digital side
of the sigma-delta mode converters and
loops analog transmit data back to the
analog receive path.

Digital 4. This loopback is at the PCM bus interface
and loops the transmit data from the line
back to the receive path.

Analog 5. The analog loopback facility can be used
to check the operation of all the signal
processing performed in the device,
including the conversions to/from analog.

Three of these loopback functions (digital 1 and 2, and
the analog loopback) can be used with tone generation
and reception via the PCM bus.

By assigning the transmit and receive time slots identi-
cally, a loopback arrangement at the PCM bus can be
effectively programmed for signals generated on the
line side of the codec. This mode is useful for testing
from the line side through the entire device.

An optional 16-bit encoding mode is included on a per-
channel basis for use in various test scenarios, or for
use by an external digital signal processor. This mode
of operation differs from the companded modes in both
the bit order and the use of multiple time slots on the
PCM bus.

Functional Description (continued)

Echo Canceller Functionality

The echo canceller has three sets of coefficient memory storage locations. One, called HPRE, contains the default balance coefficients and can be accessed as memory addresses 0—127. This serves as the coefficients for a fixed balance network (adaptation disabled), or as a starting point for echo cancelllation. The contents of these memory locations do not change with adaptation. The adaptation coefficients, which are added to the corresponding coefficients in HPRE, are stored in the HHAT area. Normally, the user has no need to access these coefficients; thus, these addresses are not described in this data sheet. The HHAT coefficients cover either the first 8, 16, 32, or the entire 64-tap length of the balance filter, depending on the settings in the LMSGAIN address. Note that all echo canceller length options in this control location may not be implemented, but are reserved for future use.

A third set of coefficients is contained in HDTA, which are used for special data call functions.

SLIC Control Capabilities

Memory locations 158, 159, and 160 are used to control six bidirectional latches that are intended to allow the serial interface to control other line card devices, such as ringing/test switches, telecom electromechanical relays, and SLIC devices. When the TTL latches are configured as outputs, external devices should be set up to sink current from the latch. Location 158 sets the operational mode of these latches as either inputs or outputs. Location 159 specifies what is to be written on the latch leads driven by the device. Location 160 reports the actual state of these leads. It should be noted that a channel control reset forces all of these external leads, except those corresponding to bits 2 and 3, to the high-impedance state, so any inputs connected to bits 0, 1, 4, and 5 should have appropriate pull-up or pull-down resistors (off-chip, if required) to force the external device into a known state at power-up or in the event of a reset. Bits 2 and 3 will reset to outputs with a value of zero.

The fast scan mode allows for a minimal data transfer on the serial bus to monitor bits 0 and 1 of the SLIC data memory location (159). If these 2 bits are wired as inputs to the off-hook and/or ring ground detection circuits, a convenient method of rapidly scanning for these two functions is obtained. Bits 2 and 3 default to outputs; thus, they are convenient to provide control of the SLIC state. In any event, all six leads are programmable for maximum flexibility.

Suggested Initialization Procedures

It is suggested that upon powerup, a hardware reset be used to set the device into a known state. The serial interface should then be used to load the memory addresses that differ from the default values (the write all channels command is convenient for this function). If other devices are controlled by the SLIC data memory location, then it also should be loaded with a known configuration. After the completion of this sequence, the device is ready to be activated. Depending on the application, the next step may either be normal operation or a set of test sequences. After the initialization of the memory, the device and associated line card devices can be controlled by using memory locations 130, 131, 145, 155, 156, 157, 158, 159, and 129; that is, by supplying the PCM bus time-slot addresses, switching the SLIC into the proper mode, and activating the codec. Within memory location 129, the codec would normally be placed into active mode, with both directions of the PCM bus enabled at the start of a call. At the completion of a call, the codec should be placed into standby mode and the PCM bus disabled. Great caution should be used when changing the memory while the codec is in active mode, since termination impedances, balance impedances, and gains may change. These changes are likely to yield undesirable system effects. It is safe to refresh coefficients that are known to be unchanging in the application. It is always possible to read the memory to verify its contents without deleterious effects on codec operation. Normal operation would load the memory and perform all gain adjustments while the codec is in standby mode. Under no circumstances should memory above address 162 be written, since this section of memory is used for state data and intermediate results. Also, all reserved addresses should not be written. Changing this information may have deleterious effects on system operation.

Functional Description (continued)

Signal Processing

Figure 20 details the signal processing functional blocks of one channel of the codec.
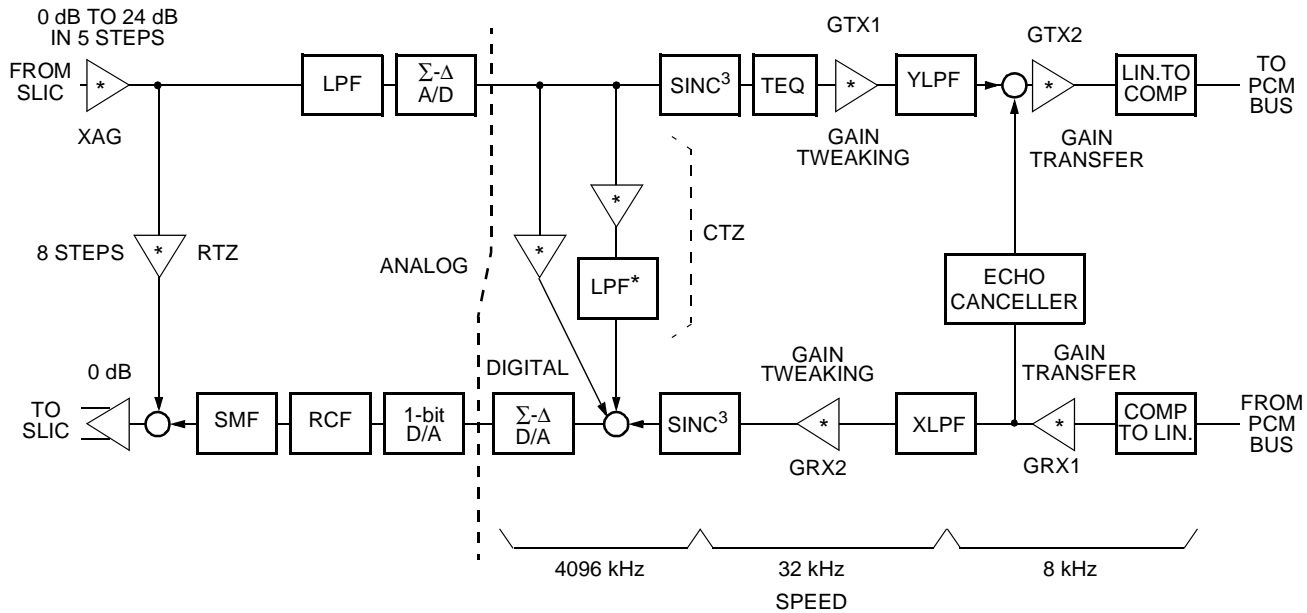
* Programmable blocks.

Figure 20. Internal Signal Processing

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational section of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature Range	T_{stg}	–55	150	°C
Power Supply Voltage (all pins designated power)	V_{DDX}	—	7	V
Negative Voltage on Any Pin with Respect to Ground	V_{SS}	–0.25	—	V
Thermal Resistance, Junction to Case (68-pin PLCC)	$R_{\Theta JC}$	—	43	°C/W
Package Power Dissipation (68-pin PLCC)	P_D	—	930	mW
Thermal Resistance, Junction to Case (64-pin MQFP)	$R_{\Theta JC}$	—	35	°C/W
Package Power Dissipation (64-pin MQFP)	P_D	—	1.14	W
Thermal Resistance, Junction to Case (44-pin PLCC)	$R_{\Theta JC}$	—	49	°C/W
Package Power Dissipation (44-pin PLCC)	P_D	—	815	mW

Operating Ranges

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	−40	85	°C
Operating Junction Temperature	T_J	−40	125	°C

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Agere Systems Inc. employs a human-body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. A standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely accepted and can be used for comparison. The HBM ESD threshold of >1000 V was obtained by using these circuit parameters:

HBM ESD Threshold Voltage	
Device	**Voltage**
T8533/T8534	>2000

Electrical Characteristics

For all specifications: T_A = −40 °C to +85 °C, V_{DD} = 5 V ± 5%, unless otherwise noted. Typical values are for T_A = 25 °C and V_{DD} = 5 V. Input signal frequency is 1004 Hz, unless otherwise noted.

dc Characteristics

Table 8. dc Characteristics
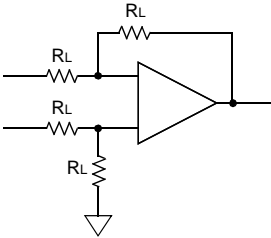
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Low	V_{IL}	All inputs	—	—	0.8	V
Input Voltage High	V_{IH}	All inputs	2.0	—	—	V
Input Current	I_{IL}	Digital, without pull-up, inputs, GND < V_{IN} < V_{DD}	−10	—	10	µA
		With internal pull-up, V_{IN} = GND (INTS, MCLK, and RST pins)	−240	—	10	µA
		With internal pull-up, V_{IN} = V_{DD} (INTS, MCLK, and RST pins)	−10	—	10	µA
Output Voltage Low	V_{OL}	I_L = 3.2 mA	—	—	0.4	V
Output Voltage High	V_{OH}	I_L = −320 µA	3.5	—	—	V
Output Current in High-impedance State	I_{OZ}	GND < V_{OUT} < V_{DD}	−30	—	30	µA
Line Driver (DX and DO pins) Output Voltage High	V_{OH}	I_L = −10 mA	V_{DD} − 0.5	—	—	V
Line Driver (DX and DO pins) Output Voltage Low	V_{OL}	I_L = 10 mA	—	—	0.5	V

Electrical Characteristics (continued)

Analog Interface

The following specifications pertain to the analog SLIC interface for each channel.

Table 9. Analog Interface

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Resistance	R_{VFXI}	$0.25 < V_{IN} < (V_{DDX} - 0.25)$ V	100	—	300	kΩ
Input Voltage	V_{IX}	Relative to ground. Signal should be capacitively coupled to VF$_X$I	1.8	2.0	2.2	V
Load Resistance at VF$_R$OP and VF$_R$ON (differential)	R_L		7.5	—	—	kΩ
Output Resistance	R_O	Digital input code corresponding to idle PCM code (μ-law)	—	2	10	Ω
Output Offset Voltage Between VF$_R$OP and VF$_R$ON	V_{OS}	Digital input code corresponding to idle PCM code (μ-law)	−100	0	100	mV
Output Offset Voltage Between VF$_R$OP and VF$_R$ON, Standby Mode	V_{OSS}	$R_L = 100$ kΩ	−20	0	20	mV
Common-mode Output Voltage, Active Mode	V_{OCM}	Digital input code corresponding to alternating ± zero μ-law PCM code	—	2.0	—	V
Common-mode Output Voltage, Standby Mode	V_{OCMS}	—	1.7	2.0	2.3	V

Electrical Characteristics (continued)

Analog Interface (continued)

Table 10. Power Requirements

Parameter	Min	Typ	Max	Unit
Operating Voltage:				
V_{DD}	4.75	—	5.25	V
V_{DDX}	4.75	—	5.25	V
Power Supply Current, V_{DD} + V_{DDX}:				
All Channels in Standby Mode	—	—	35	mA
All Channels Active	—	—	110	mA

Transmission Characteristics

Table 11. Transmission Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Absolute Levels	GAL	Maximum 0 dBm0 levels (1004 Hz): VF$_X$I (encoder milliwatt), all programmable transmit gains set to 0 dB	—	2.80	—	Vp-p
		RCV (decoder milliwatt), termination impedance off, all programmable receive gains set to 0 dB	—	5.29	—	Vp-p
		Minimum 0 dBm0 levels (1004 Hz): VF$_X$I (encoder milliwatt) XAG = 24 dB GTX1 = 6 dB GTX2 = 0 dB	—	87.5	—	mVp-p
		RCV (decoder milliwatt), termination impedance off GRX1 = 0 dB GRX2 = −6 dB	—	2.63	—	Vp-p
Absolute Maximum Voltage Swings	GAL	VF$_X$I	—	—	3.2	Vp-p
		VF$_R$OP to VF$_R$ON (differential)	—	—	5.28	Vp-p
Transmit Gain Absolute Accuracy	GXA	Transmit gain programmed for maximum 0 dBm0 test level, measured deviation of digital code from ideal 0 dBm0 level at DX digital outputs, with transmit gain set to 0 dB:				
		20 °C to 70 °C	—	±0.15	—	dB
		0 °C to 85 °C	−0.25	—	0.25	dB
		−40 °C to +85 °C	−0.35	—	0.35	dB
Transmit Gain Variation with Programmed Gain	GXAG	Measured transmit gain over the range from maximum to minimum, calculated deviation from the programmed gain relative to GXA at 0 dB, V_{DD} = 5 V	−0.1	—	0.1	dB

Electrical Characteristics (continued)

Transmission Characteristics (continued)

Table 11. Transmission Characteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Gain Variation with Frequency, 600 Ω Resistive Source Impedance and Synthesized Termination Impedance	GXAF	Relative to 1004 Hz, minimum gain < GX < maximum gain, VF_XI = 0 dBm0 signal, path gain set to 0 dB:				
		f = 16.67 Hz	—	−50	−30	dB
		f = 40 Hz	—	−40	−26	dB
		f = 50 Hz	—	−40	−30	dB
		f = 60 Hz	—	−55	−30	dB
		f = 200 Hz	—	−3.5	0	dB
		f = 300 Hz to 3000 Hz	−0.125	±0.04	0.135	dB
		f = 3140 Hz	−0.57	0.01	0.125	dB
		f = 3380 Hz	−0.735	−0.03	0.015	dB
		f = 3860 Hz	—	−9.0	−8.98	dB
		f = 4600 Hz and above	—	—	−32	dB
Transmit Gain Variation with Signal Level	GXAL	Sinusoidal test method*, reference level = 0 dBm0:				
		VF_XI = −40 dBm0 to +3 dBm0	−0.25	—	0.25	dB
		VF_XI = −50 dBm0 to −40 dBm0	−0.50	—	0.50	dB
		VF_XI = −55 dBm0 to −50 dBm0	−1.40	—	1.40	dB
Receive Gain Absolute Accuracy	GRA	Receive gain programmed to −6 dB, apply 0 dBm0 signal to DR, measure V_{RCV}, R_L = 100 kΩ differential:				
		20 °C to 70 °C	—	±0.15	—	dB
		0 °C to 85 °C	−0.25	—	0.25	dB
		−40 °C to +85 °C	−0.30	—	0.30	dB
Relative Gain, VF_ROP to VF_RON	—	Digital input 0 dBm0 signal, f = 300 Hz to 3400 Hz	−0.01	—	0.01	dB
Relative Phase, VF_ROP to VF_RON	—	Digital input 0 dBm0 signal, f = 300 Hz to 3400 Hz	−0.25	—	0.25	Degrees
Receive Gain Variation with Programmed Gain	GRAG	Measure receive gain over the range from maximum to minimum setting, calculated deviation from the programmed gain relative to GRA at 0 dB, V_{DD} = 5 V	−0.1	—	−0.1	dB
Receive Gain Variation with Frequency, 600 Ω Resistive Termination	GRAF	Relative to 1004 Hz, digital input = 0 dBm0 code, minimum gain < GR < maximum gain, 0 dB path gain:				
		f = below 3000 Hz	−0.125	±0.04	0.125	dB
		f = 3140 Hz	−0.57	±0.04	0.125	dB
		f = 3380 Hz	−0.735	−0.550	0.015	dB
		f = 3860 Hz	—	−10.7	−8.98	dB
		f = 4600 Hz and above	—	—	−28	dB
Receive Gain Variation with Signal Level	GRAL	Sinusoidal test method*, reference level = 0 dBm0:				
		IPCM digital level = −40 dBm0 to +3 dBm0	−0.25	—	0.25	dB
		IPCM digital level = −50 dBm0 to −40 dBm0	−0.50	—	0.50	dB
		IPCM digital level = −55 dBm0 to −50 dBm0	−1.40	—	1.40	dB

* Applied to all four channels.

Electrical Characteristics (continued)

Noise Characteristics

Table 12. Per-Channel Noise Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit Noise, C-Message Weighted	N_{XC}	0 dB transmit gain*	—	—	18	dBrnC0
Transmit Noise, P-Message Weighted	N_{XP}	0 dB transmit gain*	—	—	−68	dBm0p
Receive Noise, C-Message Weighted	N_{RC}	0 dB receive gain, digital pattern corresponding to idle PCM code, μ-law	—	—	13	dBrnC0
Receive Noise, P-Message Weighted	N_{RP}	0 dB receive gain, digital pattern corresponding to idle PCM code, A-law	—	—	−75	dBm0p
Noise, Single Frequency	N_{RS}	f = 0 kHz to 100 kHz, loop around measurement, V_{VFxI} = 0 Vrms	—	—	−53	dBm0
Power Supply Rejection, Transmit	PSR_X	V_{DD} = 5.0 V_{DC} + 100 mVrms f = 0 kHz to 4 kHz f = 4 kHz to 50 kHz C-message weighted	36 30	— —	— —	dBC dBC
Power Supply Rejection, Receive	PSR_R	Measured on VF_ROP, V_{DD} = 5.0 V_{DC} + 100 mVrms: f = 0 kHz to 4 kHz f = 4 kHz to 25 kHz f = 25 kHz to 50 kHz	36 40 36	— — —	— — —	dBC dBC dBC
Spurious Out-of-Band Signals at the Channel Outputs	SOS	0 dBm0, 300 Hz to 3400 Hz signal applied to V_{VFxI}, transmit gain set to 0 dB: 4600 Hz to 7600 Hz 7600 Hz to 8400 Hz 8.4 kHz to 50 kHz	— — —	— — —	−30 −40 −30	dB dB dB

* RTZ and CTZ paths open. All channels active.

Electrical Characteristics (continued)

Distortion and Group Delay

Table 13. Distortion and Group Delay

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Signal to Total Distortion, Transmit or Receive, C-Message Weighted	STD_X STD_R	Sinusoidal test method level: 3.0 dBm0 0 dBm0	33 36	— —	— —	dB dB
Single Frequency Distortion, Transmit	SFD_X	0 dBm0 single frequency input, 200 Hz $\leq$ f_{IN} $\leq$ 3400 Hz; measured at any other single frequency	—	—	−46	dB
Single Frequency Distortion, Receive	SFD_R	0 dBm0 single frequency input, 200 Hz $\leq$ f_{IN} $\leq$ 3400 Hz; measured at any other single frequency	—	—	−46	dB
Intermodulation Distortion	IMD	Transmit or receive, two frequencies in the range of 300 Hz to 3400 Hz	—	—	−50	dB
TX Group Delay, Absolute*	D_{XA}	f = 1600 Hz, 600 Ω resistive termination	—	—	370	µs
RX Group Delay, Absolute*	D_{RX}	f = 1600 Hz, 600 Ω resistive termination	—	—	220	µs

* Absolute group delay is a function of time-slot assignment, and the maximum in this table refers to the (optimal minimum group delay) time-slot assignment.

Electrical Characteristics (continued)

Crosstalk

Table 14. Crosstalk

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transmit to Transmit Crosstalk, 0 dBm0 Level	CT_{X-X}	f = 300 Hz to 3400 Hz, any channel to any channel	—	—	−80	dB
Transmit to Receive Crosstalk, 0 dBm0 Level	CT_{X-R}	f = 300 Hz to 3400 Hz, any channel to any other channel	—	—	−80	dB
		In-channel	—	—	−50	dB
Receive to Transmit Crosstalk, 0 dBm0 Level	CT_{R-X}	f = 300 Hz to 3400 Hz, any channel to any other channel	—	—	−80	dB
		In-channel	—	—	−50	dB
Receive to Receive Crosstalk, 0 dBm0 Level	CT_{R-R}	f = 300 Hz to 3400 Hz, any channel to any channel	—	—	−80	dB

Timing Characteristics

Table 15. Timing Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{DCLK}	Serial Bus Clock Frequency	—	—	—	4096	kHz
f_{BCLK}	Allowable PCM Bus Clock Frequencies* (512 kHz minimum if linear encoding is selected.)	—	— — — — — — —	256 512 1024 2048 4096 8192 16384	— — — — — — —	kHz kHz kHz kHz kHz kHz kHz
—	Jitter of BCLK	—	—	—	100 ns in 100 ms = 1 ppm	—
—	Serial Bus Clock Duty Cycle	—	40	50	60	%
—	PCM Bus Clock Duty Cycle	—	40	50	60	%
$t_{CSSETUP}$	Chip Select Setup Time, Normal Mode	Serial clock frequency = 4.096 MHz	7	—	—	ns
t_{CSHOLD}	Chip Select Hold Time, Normal Mode	Serial clock frequency = 4.096 MHz	4	—	—	ns
t_{SXDLY}	Serial Bus Output Data Delay, Normal Mode	Serial clock frequency = 4.096 MHz	—	—	9	ns
t_{SDHOLD}	Serial Bus Input Data Hold Time, Normal Mode	Serial clock frequency = 4.096 MHz	4	—	—	ns
$t_{SDSETUP}$	Serial Bus Input Data Setup Time, Normal Mode	Serial clock frequency = 4.096 MHz	7	—	—	ns
$t_{FSSETUP}$	Frame Strobe Setup Time	PCM clock frequency = 16.384 MHz	7	—	—	ns
t_{FSHOLD}	Frame Strobe Hold Time	PCM clock frequency = 16.384 MHz	4	—	—	ns
$t_{FSWIDTH}$	Frame Strobe Width	FS synchronous with BCLK	t_{BCLK}	—	125 μs − t_{BCLK}	ns
t_{XDLY}	PCM Bus Output Data Delay	PCM clock frequency = 16.384 MHz	—	—	9	ns

* PCM clock (BCLK) must be synchronous with both FS and MCLK, if used. If MCLK is used, then the rising edge of MCLK must coincide with the rising edge of BCLK within 10 ns.

† The t_{SXBDLY} delay is from either DCLK or CS, whichever transition is later, for the first bit of the byte.

Timing Characteristics (continued)

Table 15. Timing Characteristics (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{IDHOLD}	PCM Bus Input Data Hold Time	PCM clock frequency = 16.384 MHz	4	—	—	ns
$t_{IDSETUP}$	PCM Bus Input Data Setup Time	PCM clock frequency = 16.384 MHz	7	—	—	ns
t_{RISE}	Clock Edge Rise Time	Serial clock frequency = 4.096 MHz, PCM clock frequency = 16.384 MHz	—	—	8	ns
t_{FALL}	Clock Edge Fall Time	Serial clock frequency = 4.096 MHz, PCM clock frequency = 16.384 MHz	—	—	8	ns
t_{RISE}, t_{FALL}	Line Driver Rise/Fall Time (DO and DX outputs)	I_L = 15 mA, C_{LOAD} = 100 pF	—	—	30	ns
$t_{CSBHOLD}$	Chip Select Hold Time, Byte-by-Byte Mode	Serial clock frequency = 4.096 MHz	4	—	—	ns
t_{SXBDLY}	Serial Bus Output Data Delay, Byte-by-Byte Mode	Serial clock frequency = 4.096 MHz[†]	—	—	9	ns
$t_{CSBSETUP}$	Chip Select Setup Time, Byte-by-Byte Mode	Serial clock frequency = 4.096 MHz	7	—	—	ns
$t_{SDBHOLD}$	Serial Bus Data Hold Time, Byte-by-Byte Mode	Serial clock frequency = 4.096 MHz	4	—	—	ns
$t_{SDBSETUP}$	Serial Bus Data Setup Time, Byte-by-Byte Mode	Serial clock frequency = 4.096 MHz	7	—	—	ns
$t_{CSBHOLD}$	Chip Select Hold Time, Byte-by-Byte Mode	Serial clock frequency = 4.096 MHz	4	—	—	ns

* PCM clock (BCLK) must be synchronous with both FS and MCLK, if used. If MCLK is used, then the rising edge of MCLK must coincide with the rising edge of BCLK within 10 ns.
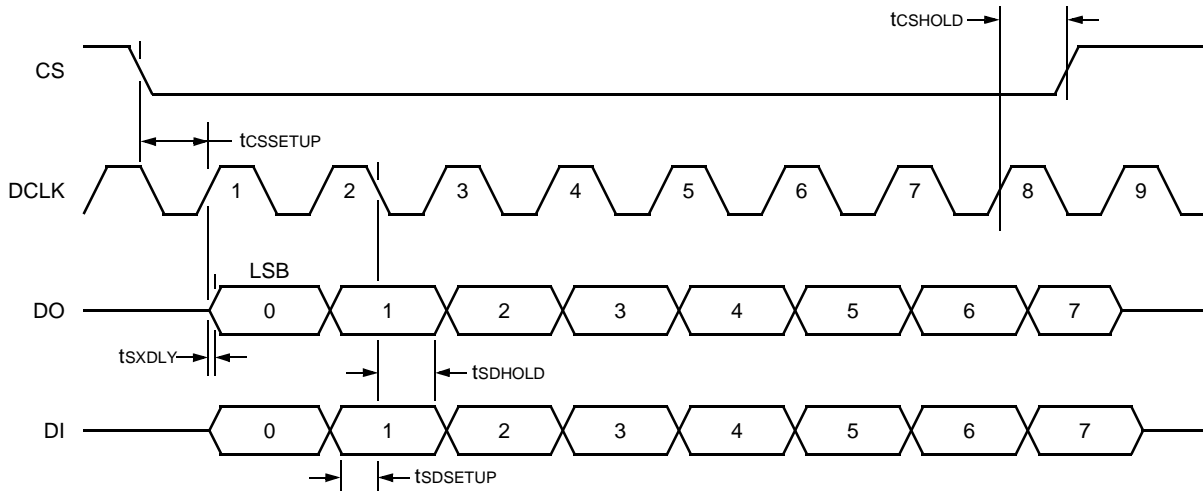† The t_{SXBDLY} delay is from either DCLK or CS, whichever transition is later, for the first bit of the byte.

Table 16. Echo Canceller Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Echo Return Loss	—	—	—	45	—	dB
Convergence Time	—	—	—	100+	—	dB/s

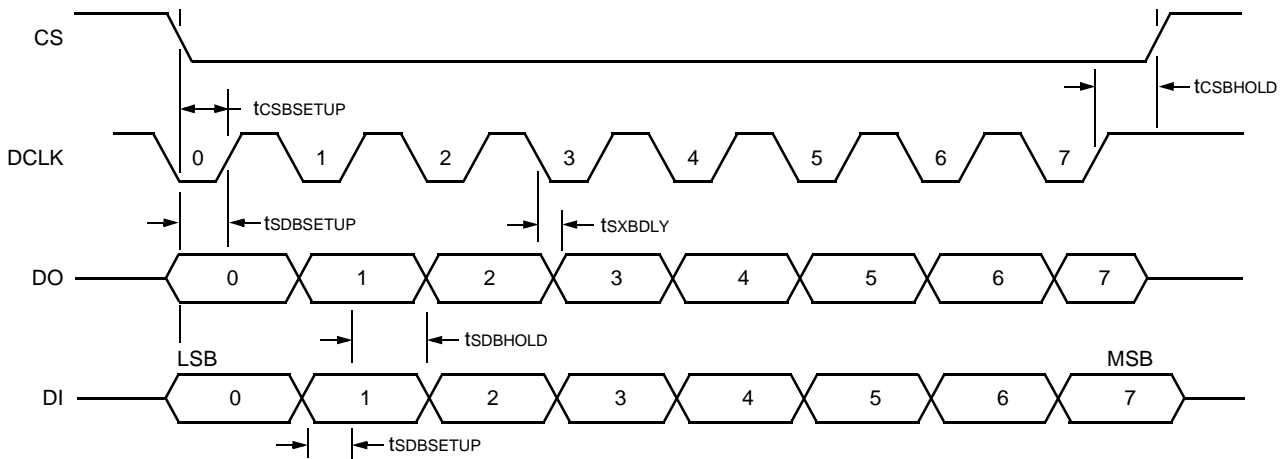## Bus Timing Diagrams

Normal Mode

5-7185.MOD(F)

Figure 21. Serial Interface Timing, Normal Mode (One Byte Transfer Shown)

Byte-by-Byte Mode

5-7186e (F)

Figure 22. Serial Interface Timing, Byte-by-Byte Mode (One Byte Transfer and Gapped DCLK Shown)

Bus Timing Diagrams (continued)

PCM Interface

Only the first time slot is shown, and the bit offset is assumed to be zero. Notice that the PCM bus transfers the most significant bit of the time slot first, consistent with normal telephony practice. The diagram shows a bit offset of zero from frame strobe, and for nonzero values of RXBITOFF and TXBITOFF, the relationship between FS and DX or DR will be shifted by the programmed number of cycles of BCLK. BCLK can be any value from 256 kHz (four time slots) to 16.384 MHz (256 time slots). The frame strobe signal is at a rate of 8 kHz and **must** be synchronous with the PCM bus clock (BCLK). Sixteen-bit linear code uses two consecutive time slots with LSB transmitted/received first. See the Clocking Considerations section for the relationship between BCLK and MCLK, if used.
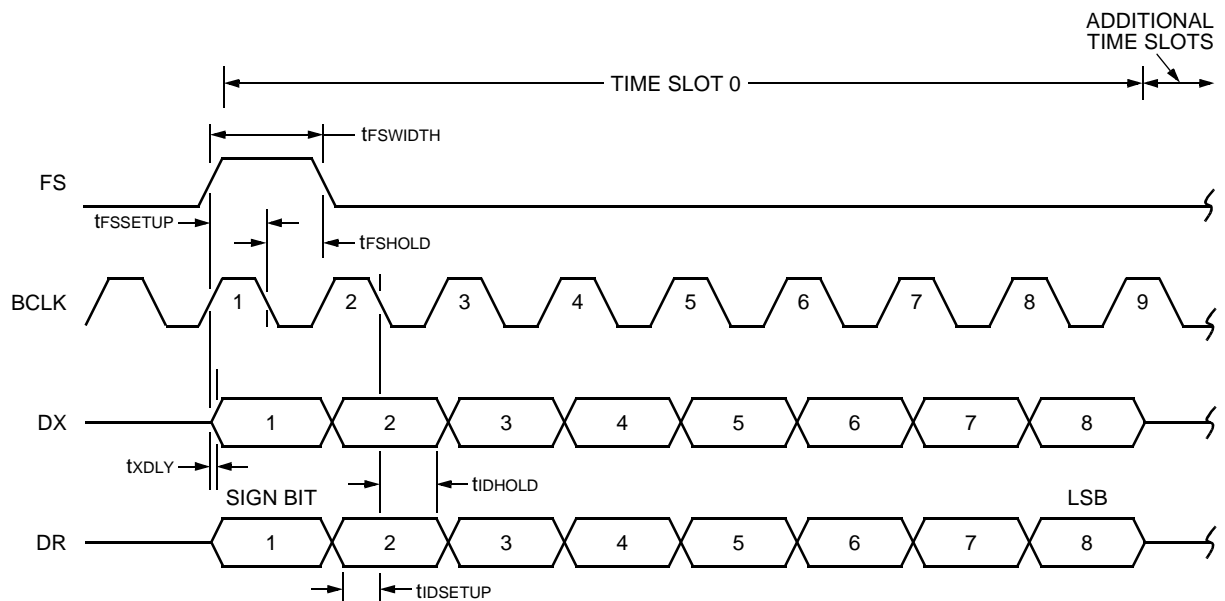
5-7188.e(F)

Figure 23. PCM Bus Timing (Diagram Shown has Bit Offset of Zero and Minimum Width of FS)

Software Interface

Table 17. Memory Mapping

With the exceptions noted, all of these memory locations may be read to determine the state of the controls contained therein. In the following table, bit 0 is the LSB (transmitted first on the serial interface) and bit 7 is the most significant bit of the byte. Unused bits in an address or multibyte address should be loaded as zero. All of the memory locations can be programmed on a per-channel basis.

Note that the entire coefficient set for a channel (or all four channels) may be loaded with one command.

Control Name	Address (decimal)	Number of Bits Used	Default Value	Name/Description
HBALTAPS*	0—127	1024	See Table 18	Balance impedance tap coefficients.
RESCTRL	128	4	0x00	Reset address. Writing a 1 in the used positions causes a reset as defined by the bit definition. This reset remains in force until the bit is written as a 0.
CHACTIVE	129	1	0x00	Standby/active control.
RXBITOFF	130	3	0x00	Bit offset for receive direction.
RXOFF	131	8	(16* channel #)	Time-slot offset for receive direction.
GRX1*	132—133	11	0x0400	Control of gain affecting receive direction gain transfer.
GRX2*	134—135	11	0x01ac	Control of gain sensitive to impedance and SLIC parameter choices, receive direction.
NORMCTRL*	136	6	0x25	Peak and far-end speech detector control.
NESCTRL*	137	3	0x06	Near-end speech detector control.
LMSGAIN*	138	8	0xee	Adaptation control address.
TDETCTRL*	139	6	0x00	Data call control address.
CTZCTRL*	140—143	31	0x07ed0000	CTZ bleed coefficients.
LMSCTRL*	144	3	0x01	Adaptation leak values.
RECCTRL*	145	5	0x00	Residual echo control.
SDCTRL*	146	7	0x19	RTZ, transmit analog gain (XAG), and analog loopback controls.
SDTSI	147	7	(17* channel #)	Internal time-slot interchanger. Default sets external pins to state referenced in this data sheet.
GTX2*	148—149	12	0x0400	Control of gain affecting transmit direction gain transfer.
ZEQCTRL*	150—152	21	0x000000	Coefficients for the equalization stage that accommodates current-sensing SLICs.
GTX1*	153—154	12	0x051a	Control of gain sensitive to impedance and SLIC parameter choices, transmit direction.
TXBITOFF	155	3	0x00	Bit offset for transmit direction.
TXOFF	156	8	(16* channel #)	Time-slot offset for transmit direction.
PCMCTRL	157	7	0x00	PCM control address.
SLICTS	158	6	0x0c	SLIC 3-state control address. A 1 enables the corresponding SLIC pin to operate as an output pin.

* The coefficients to be entered can be obtained from the Aquarium coefficient software.

Software Interface (continued)

Table 17. Memory Mapping (continued)

Control Name	Address (decimal)	Number of Bits Used	Default Value	Name/Description
SLICWR	159	6	0x00	Data to be written to the SLIC latches if the corresponding bit is set in the SLICTS control word.
SLICRD	160	6	—	Current actual state of the SLIC pins. This will be the same as SLICWR for those pins configured as outputs. All other positions will reflect the actual state of the external pin. A write operation to this word will be ignored, and within one PCM frame (125 μs), the data will be overwritten.
VERIFY	162	8	—	Test address for serial interface verification.
DATACALL	167	1	—	Read-only indicator of a data call in progress. Do not write this register.
—	254—255	16	—	Factory test only, do not access.

Table 18. Control Bit Definition

The following table shows the control bit assignments in the memory control addresses. In all control bit cases, the bit being set places the function into the active mode as defined in the function column.

Control Name (Address, Decimal) [Address, Hex]	Bit Assignment(s)	Function
HBALTAPS (0—127) [0x00—0x7f]	0—1023	Balance impedance coefficients. Default value is 0x00 for all bytes except for addresses 3 and 5, which are 0x80, and address 69, which is 0x88.
RESCTRL (128) [0x80]	4—7	Not used, load as 0s.
	3	A one resets the state associated with special data call processing.
	2	A one resets the echo canceller coefficients to 0 when channel is active.
	1	A one resets all other internal states. Does not affect programmed registers.
	0	Reset all control addresses to default values. Note that setting this bit will result in it and all others of this word becoming cleared on the next PCM frame as a normal part of this control reset functionality. Also, the state reset bits (1—3) are cleared before they are acted upon if this bit is raised; hence, it is not possible to reset both state and control by writing 0x0F to RESCTRL. If such an action is desired, it is necessary to first reset control by writing 0x01 and then, in a subsequent frame, write first 0x0E and then 0x00. Alternatively, hardware reset can be used to reset all control and state. It is necessary to wait at least 256 μs after asserting this bit before initiating any other serial I/O transactions.
CHACTIVE (129) [0x81]	1—7	Load as 0s.
	0	Active/Standby mode. A 0 causes the channel to enter standby (low power) mode and disables the PCM interface for this channel. A 1 activates the channel and the corresponding PCM bus interface. Default is 0.

Software Interface (continued)

Table 18. Control Bit Definitions (continued)

Control Name (Address, Decimal) [Address, Hex]	Bit Assignments	Function				
RXBITOFF (130) [0x82]	5—7	Receive direction bit offset for the FS signal. Defaults to 0. These 3 bits can be thought of as the least significant bits (RXOFF contains the more significant bits) of a bit counter that determines the location of the first bit of the PCM data from FS.				
	0—4	Load as 0.				
RXOFF (131) [0x83]	0—7	Receive time-slot assignment. Defaults to (16 * channel number). Each time slot represents 8 bits, allow for two time slots when using linear mode.				
GRX1 (132—133) [0x84—0x85]	0—10	Gain adjustment for gain transfer stage in receive direction. Defaults to 0x0400 (0 dB). This is an 11-bit multiply operation with a maximum gain of 2 (6 dB). 0 dB is the maximum recommended setting.				
GRX2 (134—135) [0x86—0x87]	0—10	Gain adjustment for tweak gain stage in receive direction. Defaults to 0x01ac (−7.58 dB). This is an 11-bit multiply operation with a maximum gain of 2 (6 dB). 0 dB is the maximum recommended setting.				
NORMCTRL (136) [0x88]	6—7	Load as 0s.				

	3—5	Peak detector tweaking control. Use default of 4.	Bit Number			Function (dB)
			5	4	3	
			0	0	0	0.0
			0	0	1	−3.01
			0	1	0	−6.02
			0	1	1	−9.03
			1	0	0	−12.04
			1	0	1	−15.05
			1	1	0	−18.06
			1	1	1	−21.07

	0—2	Far-end speech detector threshold. Use default of 5.	Bit Number			Function (dBm0)
			2	1	0	
			0	0	0	−57
			0	0	1	−54
			0	1	0	−51
			0	1	1	−48
			1	0	0	−45
			1	0	1	−42
			1	1	0	−39
			1	1	1	−36

Software Interface (continued)

Table 18. Control Bit Definitions (continued)

Control Name (Address, Decimal) [Address, Hex]	Bit Assignments	Function		
NESCTRL (137) [0x89]	3—7	Load as 0s.		
	2	Enable near-end speech detector. Defaults to 1 (active).		
	0—1	Threshold for the near-end speech detector. Default is 2 (–6 dB).	**Bit Number**	**Function (dB) (Threshold =)**
			1 **0**	
			0 0	0.0
			0 1	–3.5
			1 0	–6.0
			1 1	–9.5
LMSGAIN (138) [0x8a]	6—7	Length of echo canceller (8, 16, 32, 64 taps). Defaults to 3 (64 taps).	**Bit Number**	**Function**
			7 **6**	
			0 0	8 taps
			0 1	16 taps
			1 0	32 taps
			1 1	64 taps
	3—5	Relative adaptive gain of the two IIR taps in the echo canceller. Defaults to 5. A setting of 0 provides no adaptive loop gain.		
	0—2	Loop gain for adaptation algorithm. Default is 6.	**Bit Number**	**Function (Gain =)**
			2 **1** **0**	
			0 0 0	0.0078
			0 0 1	0.0156
			0 1 0	0.0313
			0 1 1	0.0625
			1 0 0	0.1250
			1 0 1	0.2500
			1 1 0	0.5000
			1 1 1	1.000
TDETCTRL (139) [0x8b]	6—7	Load as 0.		
	5	This bit being set allows the echo canceller coefficients developed off-line during a data call to be captured and saved for potential use during the next data call. Default is 0 (do not capture).		
	4	This bit enables the echo canceller to continue to adapt during a data call. Default is 0 (do not adapt during a data call).		
	3	This bit, when set, enables the use of the internal logic to determine the proper time for the off-line adaptation during a data call. Default is 0.		
	2	Selects the internal set of hybrid balance network coefficients to use on a data call. Default is 0.		
	1	This bit, when set to a 1, clears the H register at the start of a data call. Default is 0.		
	0	This bit being set freezes the echo canceller. Default is 0.		

Software Interface (continued)

Table 18. Control Bit Definitions (continued)

Control Name (Address, Decimal) [Address, Hex]	Bit Assignments	Function		
CTZCTRL (140—143) [0x8c—0x8f]	0—30	Coefficients for the CTZ termination bleed. Defaults to 0x07ed0000.		
LMSCTRL (144) [0x90]	3—7	Load as 0s.		
	0—2	Leak coefficient for LMS adaptation algorithm. Defaults to 1.		
RECCTRL (145) [0x91]	5—7	Load as 0s.		
	4	Noise match enable (comfort noise). Defaults to 0 (disabled).		
	3	Enable residual echo control. Defaults to 0 (disabled).		
	0—2	Residual echo control sensitivity factor. Defaults to 0.	**Bit Number**	**Function (dB) (Threshold =)**

			2	1	0	
			0	0	0	0.0
			0	0	1	−3.5
			0	1	0	−6.0
			0	1	1	−9.5
			1	0	0	−12.0
			1	0	1	−15.5
			1	1	0	−18.0
			1	1	1	−21.6

Control Name (Address, Decimal) [Address, Hex]	Bit Assignments	Function		
SDCTRL (146) [0x92]	7	Load as 0.		
	6	Enable **analog loopback**. Defaults to 0 (no loopback).		
	3—5	RTZ gain. Defaults to 3 (equal level point value of 3 * 0.075 = 0.225).		
	0—2	Transmit analog gain (XAG). Defaults to 1 (6 dB) gain.	**Bit Number**	**Function (dB)**

			2	1	0	
			0	0	0	0.0
			0	0	1	6.02
			0	1	0	12.04
			0	1	1	18.06
			1	0	0	24.08

| Control Name (Address, Decimal) [Address, Hex]	Bit Assignments	Function
SDTSI (147) [0x93]	7	Load as 0.
	6	Digital loopback, loopback from receive to transmit at the sigma-delta converters (**digital loopback 2**). Defaults to 0 (no loopback).
	4—5	Digital channel feeding this analog receive channel. Defaults to channel number.
	3	Send idle channel code (alternating bits) to this analog receive path. Defaults to 0 (do not send idle channel code).
	2	Loopback from transmit to receive at the sigma-delta converters (**digital loopback 3**). Defaults to 0 (no loopback).
	0—1	Analog channel feeding this digital channel in the transmit direction. Defaults to channel number.
GTX2 (148—149) [0x94—0x95]	0—11	Gain control for gain transfer stage in transmit direction. Defaults to 0x0400 (0 dB). This is a 12-bit multiply operation with a maximum gain of 4 (12 dB).

Software Interface (continued)

Table 18. Control Bit Definitions (continued)

Control Name (Address, Decimal) [Address, Hex]	Bit Assignments	Function
ZEQCTRL (150—152) [0x96—0x98]	0—20	Coefficients for the equalization stage that accommodates current-sensing SLICs. Defaults to 0x000000.
GTX1 (153—154) [0x99—0x9a]	0—11	Gain control for tweak gain stage in transmit direction. Defaults to 0x051a (2.11 dB). This is a 12-bit multiply operation with a maximum gain of 4 (12 dB).
TXBITOFF (155) [0x9b]	5—7	Transmit direction bit offset for the FS signal. Defaults to 0. These 3 bits can be thought of as the least significant bits (TXOFF contains the more significant bits) of a bit counter that determines the location of the first bit of the PCM data from FS.
	0—4	Load as 0.
TXOFF (156) [0x9c]	0—7	Transmit time-slot assignment. Defaults to (16 * channel number). Each time slot represents 8 bits, allow for two time slots when using linear mode.
PCMCTRL (157) [0x9d]	7	3-state transmit PCM interface. Defaults to 0. A 1 forces the PCM interface into a high-impedance state during its assigned time slot on the PCM bus. Placing the channel in standby mode also forces a high-impedance condition on the transmit interface.
	6	Transmit zeroes instead of data. Defaults to 0 (off).
	5	Load as 0.
	4	Place idle channel code on receive path. Defaults to 0 (off).
	3	Loopback receive to transmit at PCM conversion interface (**digital loopback 1**). Defaults to 0 (no loopback).
	2	Loopback transmit to receive at PCM conversion interface (**digital loopback 4**). Defaults to 0 (no loopback).
	1	Linear/companded. A 1 sets 16-bit linear mode with two adjacent time slots used, LSB transmitted first. Linear data is in two's complement form. A 0 sets companded mode with only one time slot used, and MSB transmitted first. Defaults to 0.
	0	µ-law or A-law. A 0 sets µ-law mode, and a 1 sets A-law mode. This bit has no effect if bit 1 of this address is set to 1. Defaults to 0 (µ-law).
SLICTS (158) [0x9e]	6—7	Load as 0.
	0—5	Controls the drivers for the corresponding SLIC latches. A 1 enables the pin as an output. Defaults to 0x0c (bits 2 and 3 set, the rest cleared).
SLICWR (159) [0x9f]	6—7	Load as 0.
	0—5	SLIC data latches. If the corresponding bit in the SLICTS address is set for an output, the device will drive the corresponding bit according to the contents of this address. Writes are performed within 125 µs. Wait 125 µs before a subsequent write to the same channel or between **write all channel** commands. Default is 0.
SLICRD (160) [0xa0]	6—7	Not used, ignore on a codec read command addressing this location.
	0—5	Reports the actual state of the SLIC pins. Anything written to this address is ignored. Updates within 125 µs.
VERIFY (162) [0xa2]	0—7	Test location for serial interface. This location has no internal use, but merely latches write data for the purpose of testing the serial interface. This register does not clear with reset.
DATACALL (167) [0xa7]	5	This bit is set to a 1 if a data call is in progress. Do not attempt to write this register.
	0—4, 6, 7	Internal state control bits; do not write and ignore on read.

Applications

The following reference circuit shows a complete schematic for interfacing to the Agere L9215G SLIC. All ac parameters are programmed by the T8534. Note that this implementation differentiates itself in that no external components are required in the ac interface to provide a dc termination impedance or for stability. For illustration purposes, 0.5 Vrms PPM injection was assumed in this example and no meter pulse rejection is used. Also, this example illustrates the device using programmable overhead and current limit.
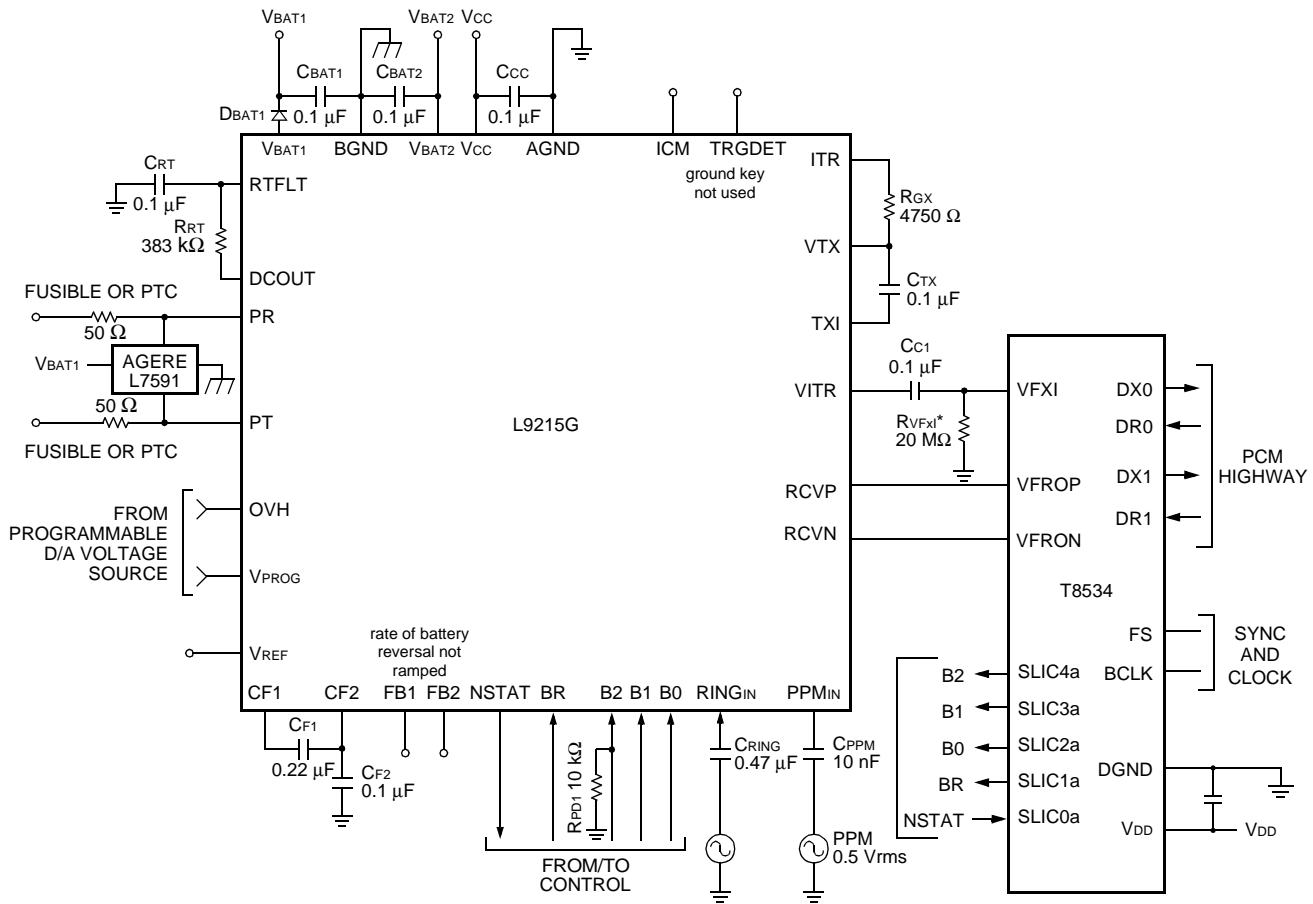
12-3534.z (F)

*R_{VFxI} is required for complex terminations. Optional for resistive terminations.

Figure 24. POTS Interface

Outline Diagrams

68-Pin PLCC

Dimensions are in millimeters.

Note: The dimensions in this outline diagram are intended for informational purposes only.
For detailed footprint drawings to assist your design efforts, please contact your Agere Sales Representative.
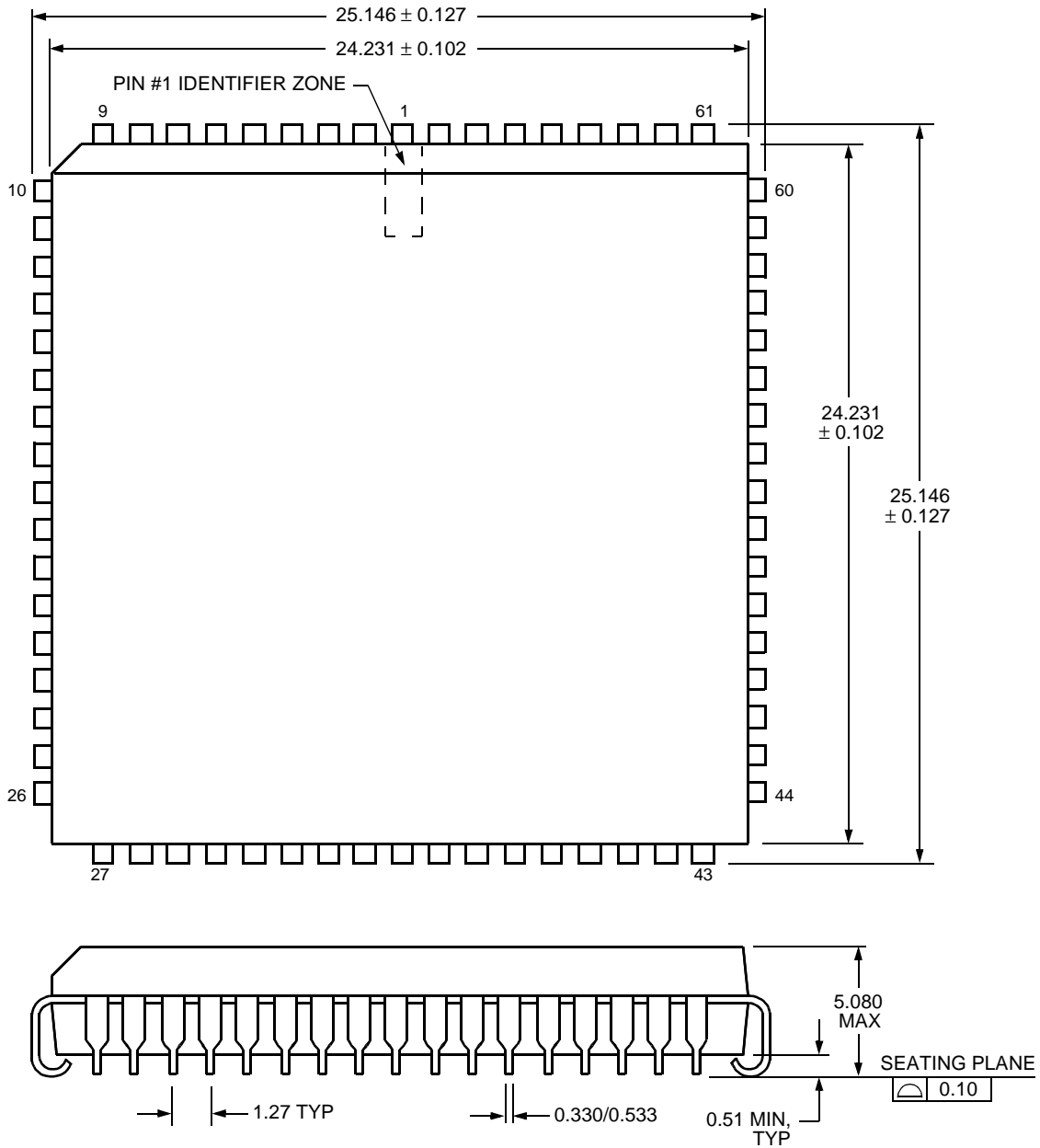
5-2139(F)

Outline Diagrams (continued)

64-Pin TQFP

Dimensions are in millimeters.

Note: The dimensions in this outline diagram are intended for informational purposes only.
For detailed footprint drawings to assist your design efforts, please contact your Agere Sales Representative.

DETAIL A

DETAIL B

5-3080(F)
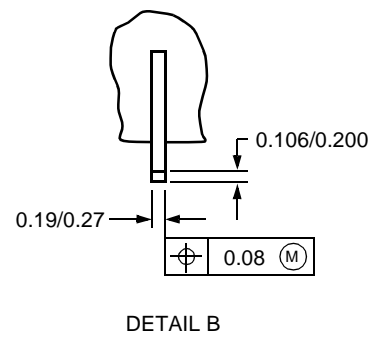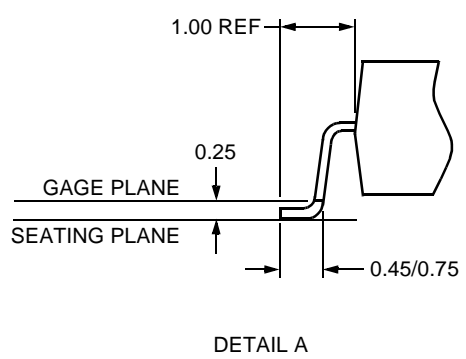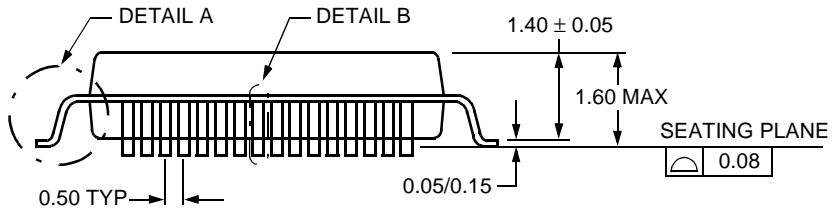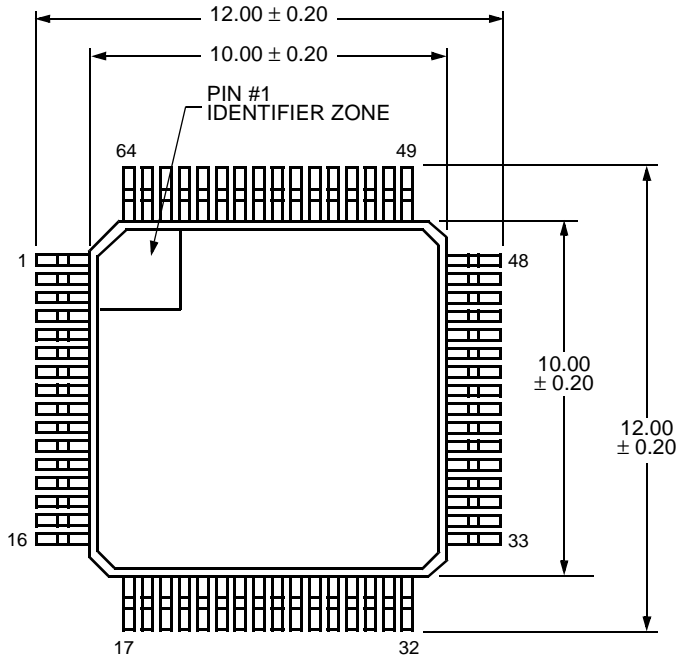
Outline Diagrams (continued)

44-Pin PLCC

Dimensions are in millimeters.

Note: The dimensions in this outline diagram are intended for informational purposes only.
For detailed footprint drawings to assist your design efforts, please contact your Agere Sales Representative.
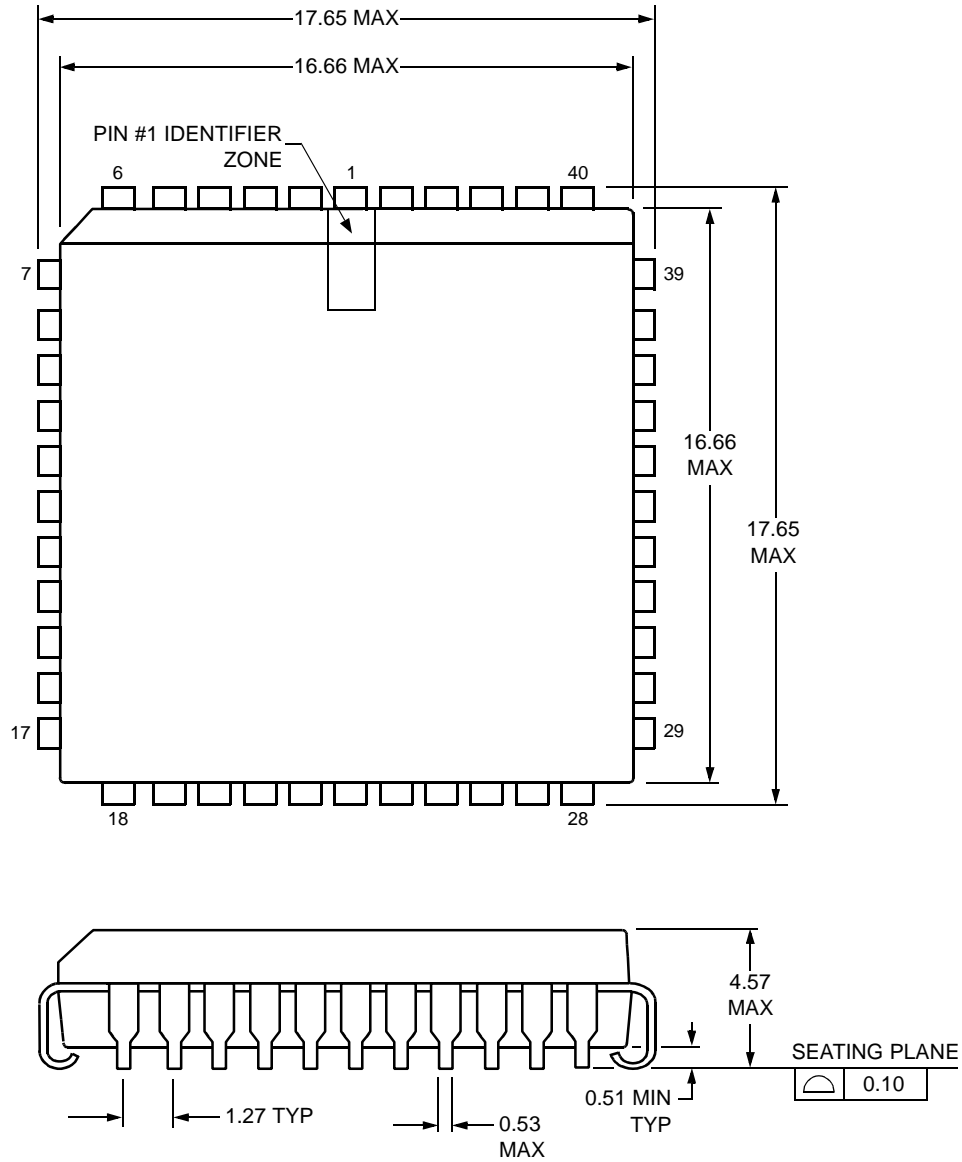
5-2506(F)

Ordering Information

Device Code	Package	Comcode
T-8533 - - - ML - D	44-Pin PLCC, Dry-bagged	108269408
T-8534 - - - TL - DB	64-Pin TQFP, Dry pack tray	108420217
T-8534 - - - ML - D	68-Pin PLCC, Dry-bagged	108269424

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