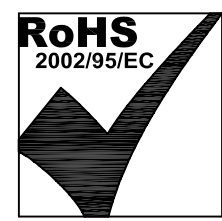


ELECTRICAL SPECIFICATIONS:

- 1.0 TURNS RATIO: (P6-P5-P4) : (J6-J3) : 1CT : 1CT ± 3%  
 (P3-P2-P1) : (J2-J1) : 1CT : 1CT ± 3%
- 2.0 INDUCTANCE: (P6-P4) : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias  
 (P3-P1) : 350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias
- 3.0 LEAKAGE INDUCTANCE: P6-P4 (WITH J6 AND J3 SHORT) : 0.3 MAX. @ 1MHz  
 P3-P1 (WITH J2 AND J1 SHORT) : 0.3 MAX. @ 1MHz
- 4.0 INTERWINDING CAPACITANCE: (P6,P5,P4) TO (J6,J3) : 30pf MAX @ 1MHz  
 (P3,P2,P1) TO (J2,J1) : 30pf MAX. @ 1MHz
- 5.0 DC RESISTANCE: (J6-J3)=(J2-J1) : 1.2 ohms Max.

NOTES

1.0 PINS WITHOUT ELECTRICAL CONNECTION ARE OMITTED.



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RECEIVE

6.0 RETURN LOSS: 1MHz TO 30MHz : 18dB MIN.  
60MHz TO 80MHz : 12dB MIN.

NOTE: 100 OHMS CONNECTED TO (J2-J1) OR (J6-J3).

7.0 DIELECTRIC WITHSTAND: (J1, J2) TO (P1, P3) : 1500 VAC  
(J3, J6) TO (P4,P6) : 1500 VAC

8.0 INSERTION LOSS: RS=RL=100 ohms : 1.1 dB TYP  
100kHz TO 100MHz

9.0 RISE TIME: RS=100 OHMS AND RL = 100 OHMS : 3.0 nS MAX  
OUTPUT VOLTAGE = 1 V peak : 3.0 nS MAX  
PULSE WIDTH= 112nS

10.0 CROSS TALK: 1MHz TO 100MHz : 40 dB TYP

11.0 COMMON TO COMMON MODE ATTENUATION: 30MHz TO 100MHz : 35dB TYP

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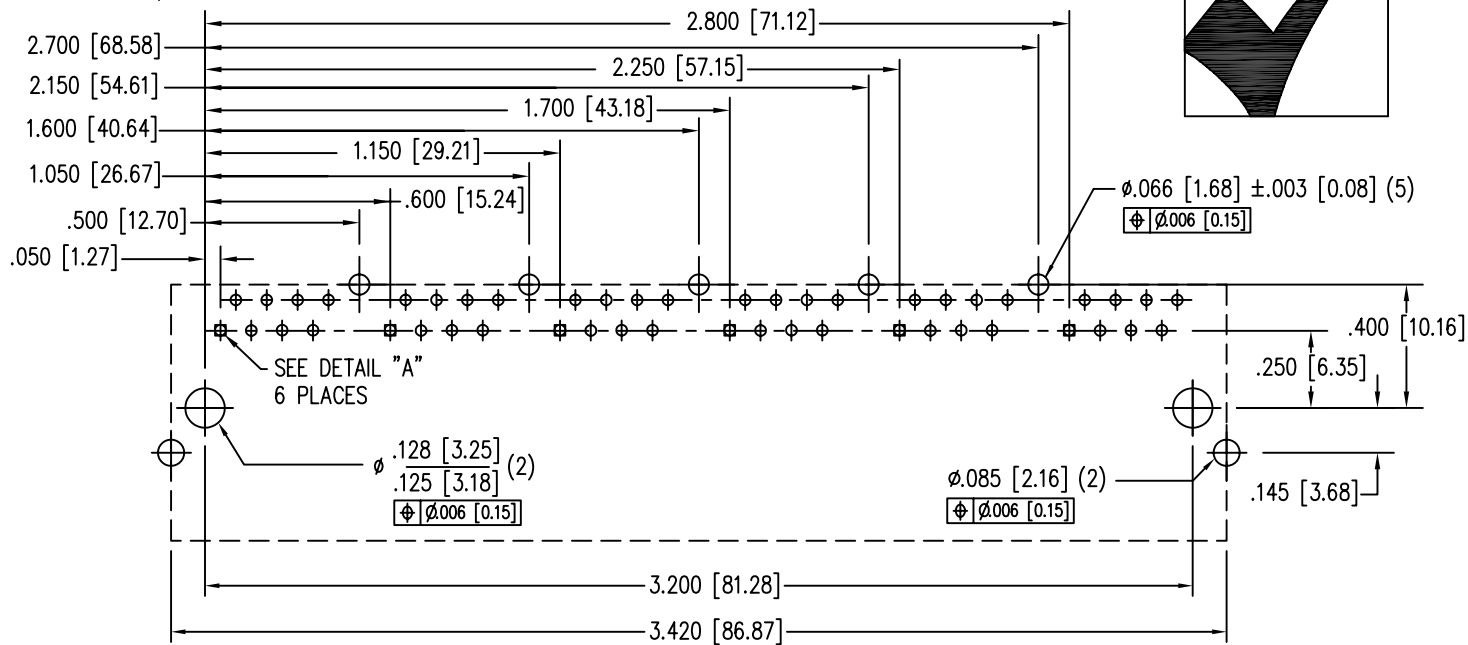
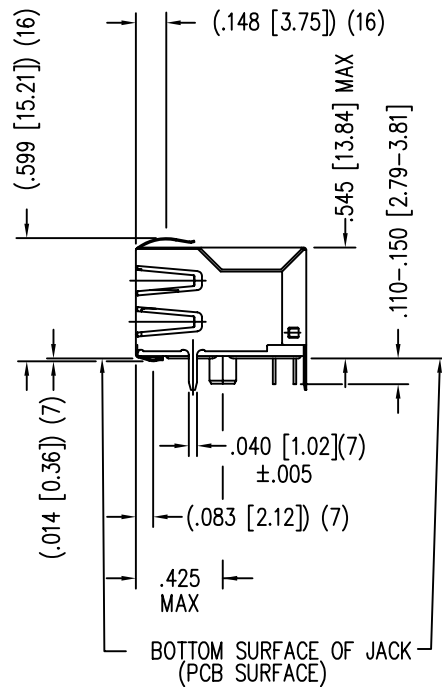
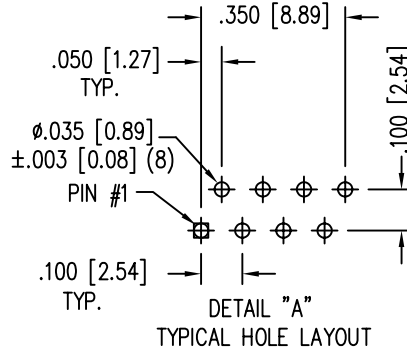
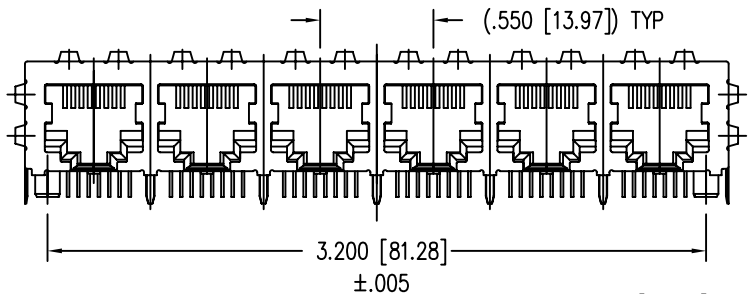
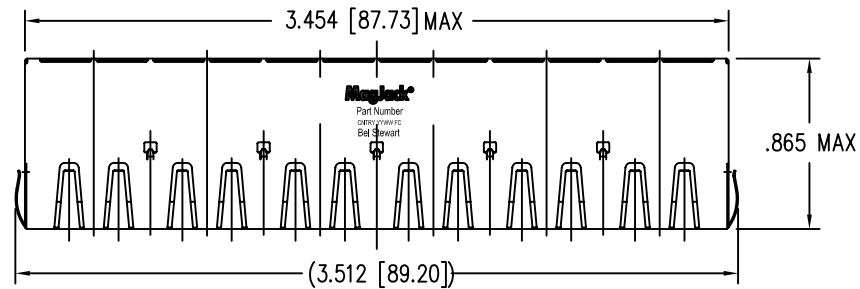
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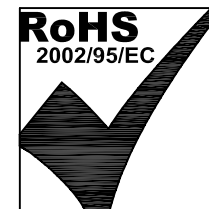
REV.  
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P.C.B. RECOMMENDED HOLE LAYOUT  
SEEN FROM COMPONENT SIDE  
ALL CENTERLINE DIMENSIONS ARE BASIC

NOTES:

- CONNECTOR MATERIALS:  
HOUSING: THERMOPLASTIC UL94 V-0  
CONTACT/SHIELD: COPPER ALLOY  
SHIELD PLATING: NICKEL OR TIN  
CONTACT PLATING: SELECTIVE GOLD,  
50 MICRO-INCHES MIN. IN CONTACT AREA.
- PIN NOT ELECTRICALLY CONNECTED MAYBE OMITTED.  
SEE ELECTRICAL DRAWING FOR OMITTED PINS.
- TOLERANCES COMPLY WITH F.C.C. DIMENSION REQUIREMENTS.
- ALL TOLERANCES NOT OTHERWISE SPECIFIED TO BE  $\pm .005 [0.13]$
- WAVE SOLDER COMPATIBLE - PREHEAT 125°C/90SECS.



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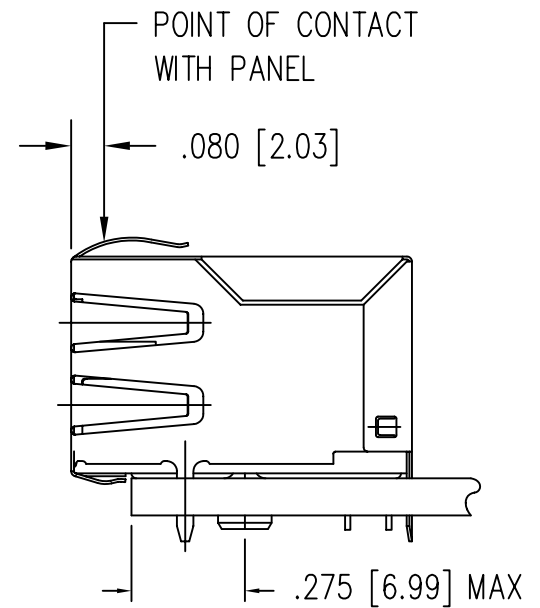
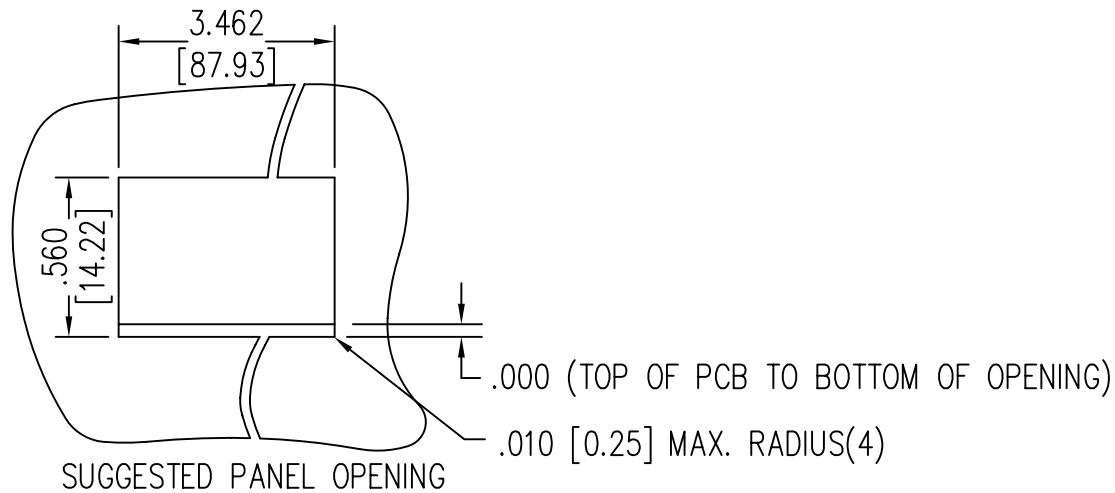
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REV. 02



THE SUGGESTED PANEL OPENING IS INTENDED TO GIVE THE USER THE ABILITY TO HAVE REASONABLE JACK / PANEL CLEARANCES YET MAINTAIN RELIABLE GROUNDING CAPABILITY.

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