



Solid State Devices, Inc.

14830 Valley View Blvd * La Mirada, Ca 90638

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DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF140 **J** — —
 + Screening ^{2/} — = Not Screen
 TX = TX Level
 TXV = TXV Level
 S = S Level
 + Lead Option ^{3/} — = Cooper Core Alloy Leads
 BW = Welded Copper Leads
 + Package: TO-257

**SFF140J
SFF140JBW**

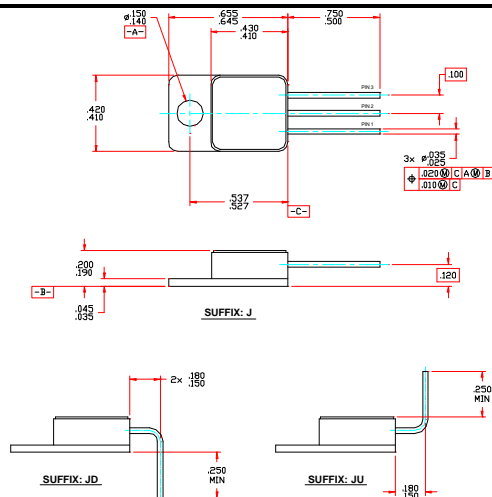
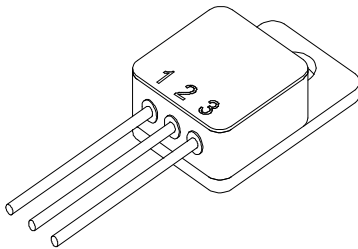
**28 AMP / 100 Volts
0.077 W
N-Channel
POWER MOSFET**

Features:

- Rugged Construction with Polysilicon Gate Cell
- Low R_{DS(ON)} and High Transconductance
- Excellent High Temperature Stability
- Very Fast Switching Speed
- Fast Recovery and Superior dV/dt Performance
- Increased Reverse Energy Capability
- Low Input and Transfer Capacitance for Easy Paralleling
- Ceramic Seals for Improved Hermeticity
- Hermetically Sealed Surface Mount Power Package
- TX, TXV, Space Level Screening Available
- Replacement for IRF140/540 Types
- Available with enhanced flexibility Cu pins: SFF140JBW

Maximum Ratings		Symbol	Value	Units
Drain – Source Voltage		V _{DS}	100	Volts
Gate – Source Voltage		V _{GS}	±20	Volts
Continuous Collector Current		I _D	28	Amps
Power Dissipation	T _C = 25°C T _C = 55°C	P _D	62.5 47.5	W
Operating & Storage Temperature		Top & Tstg	-55 to +150	°C
Maximum Thermal Resistance Junction to Case		R _{qJC}	2	°C/W

**TO-257
Pin Out:
Pin1: Drain
Pin2: Source
Pin3: Gate**



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

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SFF140J
SFF140JBW

Electrical Characteristics @ T _J = 25°C (Unless Otherwise Specified)		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage (V _{GS} =0 V, I _D =250 μA)		BV _{DSS}	100	—	—	Volts
Drain to Source On State Resistance (V _{GS} =10 V, I _D =50% Rated ID)		R _{DS(on)1}	—	0.067	0.077	W
On State Drain Current (V _{DS} >I _{D(on)} X R _{DS(on)} Max, V _{GS} =10V, I _D = rated ID)		R _{AS(on)2}	—	—	0.125	A
Gate Threshold Voltage (V _{DS} =V _{GS} , I _D = 250μA)		V _{GS(th)}	2.0	2.4	4.0	V
Forward Transconductance (V _{DS} >I _{D(on)} X R _{DS(on)} Max, I _{DS} = 60% Rated ID)		g _{fs}	8.7	13	—	S(mho)
Zero Gate Voltage Drain Current (V _{DS} =max rated voltage, V _{GS} =0 V) (V _{DS} =80% rated V _{DS} , V _{GS} =0 V, T _A =150°C)		I _{DSS}	—	—	25 250	mA
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V _{GS}	I _{GSS}	— —	— —	+100 -100	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	V _{GS} =10 Volts 60% rated V _{DS} 60% Rated ID	Q _g Q _{gs} Q _{gd}	— — —	40 8 19	75 12 35	nC
Turn on Delay Time Rise Time Turn on Delay Time Fall Time	V _{DD} =50% Rated V _{DS} 60% Rated ID R _G = 6.2Ω V _{GS} =10 Volts	t _{d(on)} t _r t _{d(off)} t _f	— — — —	15 72 40 50	23 110 60 75	nsec
Diode Forward Voltage (I _S = Rated I _D , V _{GS} =0 V, T _J =25°C)		V _{SD}	—	1.3	2.5	V
Diode Reverse Recovery Time Reverse Recovery Charge	T _J =25°C I _F =10A Di/dt=100A/μsec	t _{rr} Q _{RR}	— 0.44	150 0.91	400 1.9	nsec nC
Input Capacitance Input Capacitance Reverse Transfer Capacitance	V _{GS} =0 Volts V _{DS} =25 Volts f=1 MHz	C _{iss} C _{oss} C _{rss}	— — —	1750 575 125	— — —	pF

For thermal derating curves and other characteristics please contact SSDI Marketing Department.

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