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NTE6508
Integrated Circuit
CMOS, 1K Static RAM (SRAM)

Description:

The NTE6508 is a 1024 x 1 fully static CMOS RAM in a 16–Lead DIP type package fabricated using self–aligned silicon gate technology. Synchronous circuit design techniques are employed to acheive high performance and low power operation. On chip latches are provided for address allowing effecient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

Features:

- Low Power Standby: 50μW Max
- Low Power Operation: 20mW/MHz Max
- Fast Access Time: 300ns Max
- Data Retention: 2V Min
- TTL Compatible Input/Output
- High Output Drive: 2 TTL Loads
- On–Chip Address Register

Absolute Maximum Ratings: (Note 1)

Supply Voltage . . . . . +7V
Input, Output or I/O Voltage . . . . . GND –0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 1.5mA/MHz increase in $I_{CC(OP)}$
Gate Count . . . . . 1925 Gates
Operating Junction Temperature . . . . . +175°C
Storage Temperature Range . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10s max) . . . . . +300°C

Note 1. Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. This device is sensitive to electrostatic discharge, users should follow proper IC handling procedures.

Recommended Operating Conditions:

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . –40° to +85°C

DC Electrical Characteristics: V_{CC} = 5V ±10%, T_A = –40° to +85°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Standby Supply Current	$I_{CC(SB)}$	I_O = 0, V_I = V_{CC} or GND, V_{CC} = 5V	–	–	10	µA
Operating Supply Current	$I_{CC(OP)}$	$\overline{E}$ = 1MHz, I_O = 0, V_I = V_{CC} or GND, V_{CC} = 5.5V, Note 2	–	–	4	mA
Data Retention Supply Current	$I_{CC(DR)}$	V_{CC} = 2V, I_O = 0, V_I = V_{CC} or GND, $\overline{E}$ = V_{CC}	–	–	10	µA
Data Retention Supply Voltage	$V_{CC(DR)}$		2.0	–	–	V
Input Leakage Current	I_I	V_I = V_{CC} or GND, V_{CC} = 5.5V	–1.0	–	+1.0	µA
Output Leakage Current	I_{OZ}	V_O = V_{CC} or GND, V_{CC} = 5.5V	–1.0	–	+1.0	µA
Input Voltage, LOW	V_{IL}	V_{CC} = 4.5V	–0.3	–	+0.8	V
Input Voltage, HIGH	V_{IH}	V_{CC} = 5.5V	V_{CC}–2	–	V_{CC}+0.3	V
Output Voltage, LOW	V_{OL}	I_O = 3.2mA, V_{CC} = 4.5V	–	–	0.4	V
Output Voltage, HIGH	V_{OH}	I_O = –0.4mA, V_{CC} = 4.5V	2.4	–	–	V

Note 2. Typical derating 1.5mA/MHz increase in $I_{CC(OP)}$.

Capacitance: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	C_I	f = 1MHz, All measurements are referenced to device GND	–	–	6	pF
Output Capacitance	C_O		–	–	10	pF

AC Electrical Characteristics: V_{CC} = 5V ±10%, T_A = –40° to +85°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Chip Enable Access Time	TELQV	Note 3, Note 5	–	–	300	ns
Address Access Time	TAVQV	Note 3, Note 5, & Note 6	–	–	300	ns
Chip Enable Output Enable Time	TELQX	Note 4, Note 5	5	–	160	ns
Write Enable Output Disable Time	TWLQZ	Note 4, Note 5	–	–	160	ns
Chip Enable Output Disable Time	TEHQZ	Note 4, Note 5	–	–	160	ns
Chip Enable Pulse Negative Width	TELEH	Note 3, Note 5	300	–	–	ns
Chip Enable Pulse Positive Width	TEHEL	Note 3, Note 5	100	–	–	ns
Address Setup Time	TAVEL	Note 3, Note 5	0	–	–	ns
Address Hold Time	TELAX	Note 3, Note 5	50	–	–	ns
Data Setup Time	TDVWH	Note 3, Note 5	110	–	–	ns
Data Hold Time	TWHDX	Note 3, Note 5	0	–	–	ns
Chip Enable Write Pulse Setup Time	TWLEH	Note 3, Note 5	130	–	–	ns
Chip Enable Write Pulse Hold Time	TELWH	Note 3, Note 5	130	–	–	ns
Write Enable Pulse Width	TWLWH	Note 3, Note 5	130	–	–	ns
Read or Write Cycle Time	TELEL	Note 3, Note 5	350	–	–	ns

Note 3. Input pulse levels: 0.8V to V_{CC} –2V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) – for C_L greater than 50pF, access time is derated by 0.15ns per pF.

Note 4. Tested at initial design and after major design changes.

Note 5. V_{CC} = 4.5V and 5.5V.

Note 6. TAVQV = TELQV + TAVEL.

Read Cycle Truth Table:

Time Reference	Inputs				Outputs	Function
	$\overline{E}$	$\overline{W}$	A	D	Q	
–1	H	X	X	X	Z	Memory Disabled
0	↓	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	X	Output Enables
2	L	H	X	X	V	Output Valid
3	↑	H	X	X	V	Read Accomplished
4	H	X	X	X	Z	Prepare for Next Cycle (Same as –1)
5	↓	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the NTE6508 Read Cycle, the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Write Cycle Truth Table:

Time Reference	Inputs				Outputs	Function
	$\overline{E}$	$\overline{W}$	A	D	Q	
–1	H	X	X	X	Z	Memory Disabled
0	↓	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↓	X	X	Z	Write Period Begins
2	L	↑	X	V	Z	Data is Written
3	↑	H	X	X	Z	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as –1)
5	↓	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

Pin Connection Diagram